FAIRCHILD

SEMICONDUCTOR®

February 2008

MM74HCT04
Hex Inverter

Features

■ TTL, LS pin-out and threshold compatible
■ Fast switching: t_{PLH}, t_{PHL}=12 ns (typ)
■ Low power: 10 µW at DC, 3.7 mW at 5 MHz
■ High fanout: ≥ 10 LS loads
■ Inverting, triple buffered

General Description

The MM74HCT04 is a logic function fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. This device is input and output characteristic as well as pin-out compatible with standard 74LS logic families. The MM74HCT04, triple buffered, hex inverters, features low power dissipation and fast switching times. All inputs are protected from static discharge by internal diodes to V_{CC} and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Ordering Information

Order Number	Package Number	Package Description
MM74HCT04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HCT04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP

Top View

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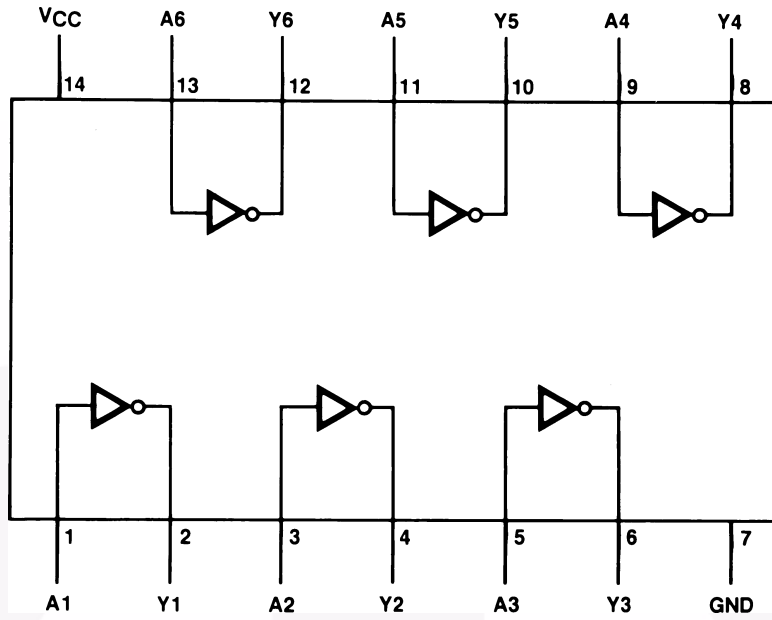
Absolute Maximum Ratings[1]

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +7.0V
V_{IN}	DC Input Voltage	–1.5 to V_{CC}+1.5V
V_{OUT}	DC Output Voltage	–0.5 to V_{CC}+0.5V
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.

2. Power Dissipation temperature derating — plastic "N" package: –12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C
t_r, t_f	Input Rise or Fall Times		500	ns

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DC Electrical Characteristics

V_{CC} = 5V ± 10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C Typ.	T_A = 25°C Guaranteed Limits	T_A = –40°C to 85°C	T_A = –55°C to 125°C	Units
V_{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $|I_{OUT}| = 20\mu A$	V_{CC}	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
		$V_{IN} = V_{IH}$ or V_{IL}, $|I_{OUT}| = 4.0mA$, $V_{CC} = 4.5V$	4.2	3.98	3.84	3.7	
		$V_{IN} = V_{IH}$ or V_{IL}, $|I_{OUT}| = 4.8mA$, $V_{CC} = 5.5V$	5.2	4.98	4.84	4.7	
V_{OL}	Maximum LOW Level Voltage	$V_{IN} = V_{IH}$, $|I_{OUT}| = 20\mu A$	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$, $|I_{OUT}| = 4.0mA$, $V_{CC} = 4.5V$	0.2	0.26	0.33	0.4	
		$V_{IN} = V_{IH}$, $|I_{OUT}| = 4.8mA$, $V_{CC} = 5.5V$	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		2.0	20	40	µA
		$V_{IN} = 2.4V$ or $0.5V$ [3]		0.3	0.4	0.5	mA

Note:

3. This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics

V_{CC} = 5.0V, t_r = t_r = 6ns, C_L = 15pF, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics

V_{CC} = 5.0V ±10%, t_r = t_f = 6ns, C_L = 50pF (unless otherwise noted)

Symbol	Parameter	Conditions	T_A = 25°C Typ.	T_A = −40°C to 85°C	T_A = −55°C to 125°C	Units
				Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay		14	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(4)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note:

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions

LAND PATTERN RECOMMENDATION
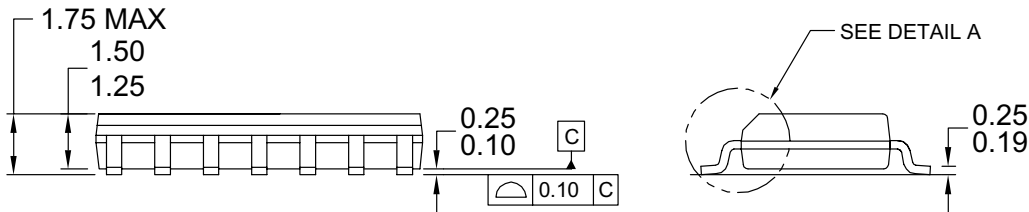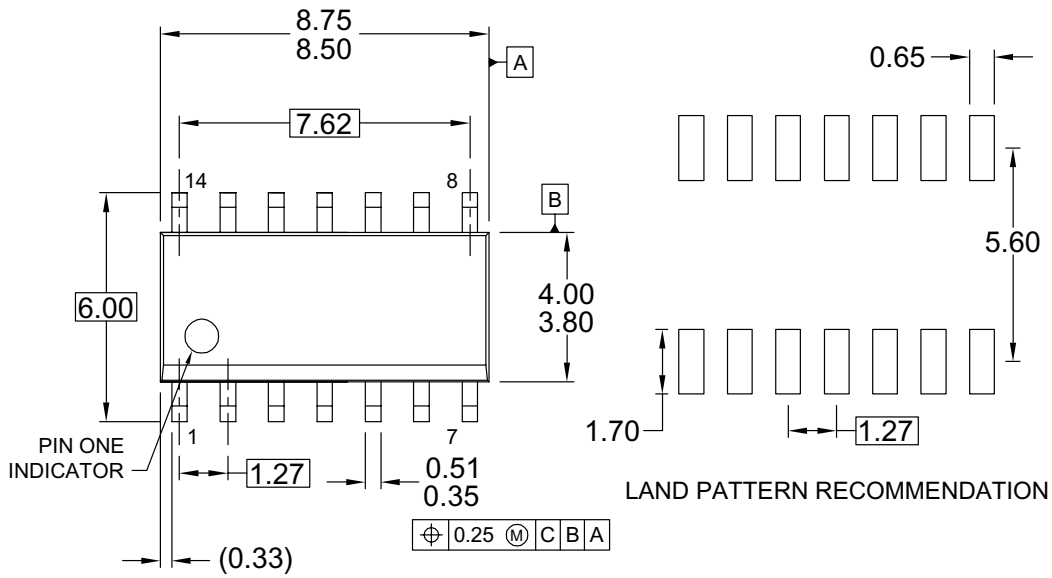
NOTES: UNLESS OTHERWISE SPECIFIED
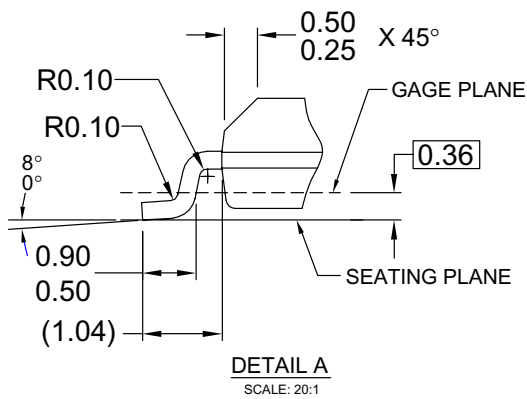
A) THIS PACKAGE CONFORMS TO JEDEC
   MS-012, VARIATION AB, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD
   FLASH OR BURRS.
D) LANDPATTERN STANDARD:
   SOIC127P600X145-14M
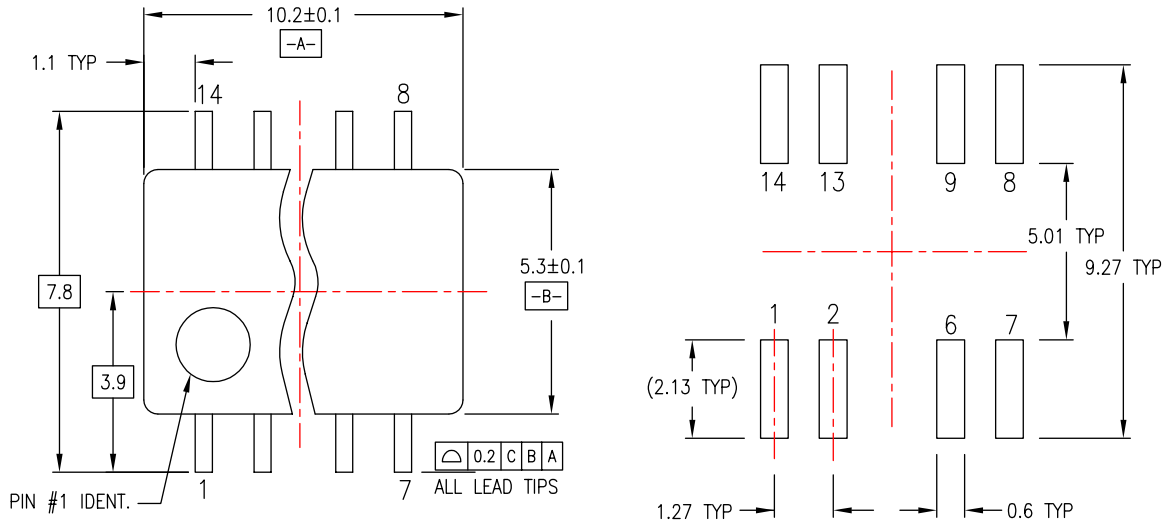E) DRAWING CONFORMS TO ASME Y14.5M-1994
F) DRAWING FILE NAME: M14AREV13

DETAIL A
SCALE: 20:1

Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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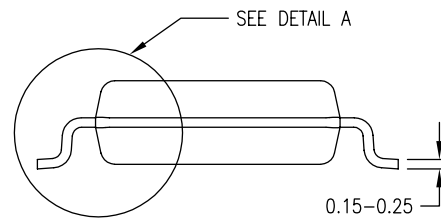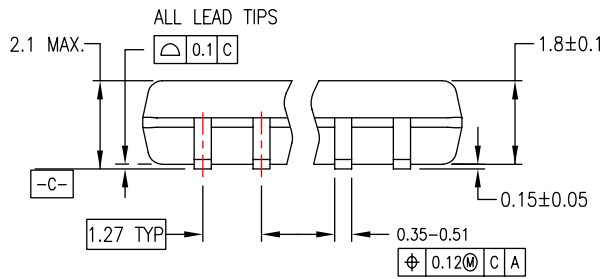
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Physical Dimensions (Continued)

10.2±0.1
−A−

1.1 TYP

14   8

7.8

3.9

5.3±0.1
−B−

PIN #1 IDENT.   1   7

△ 0.2 C B A
ALL LEAD TIPS

Land Pattern Recommendation

14   13   9   8

5.01 TYP

9.27 TYP

1   2   6   7

(2.13 TYP)

1.27 TYP   0.6 TYP

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS

2.1 MAX.

△ 0.1 C

1.8±0.1

−C−

1.27 TYP   0.35−0.51

0.15±0.05

⊕ 0.12Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO EIAJ EDR−7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

SEE DETAIL A

0.15−0.25

7° TYP

GAGE PLANE

0°−8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE
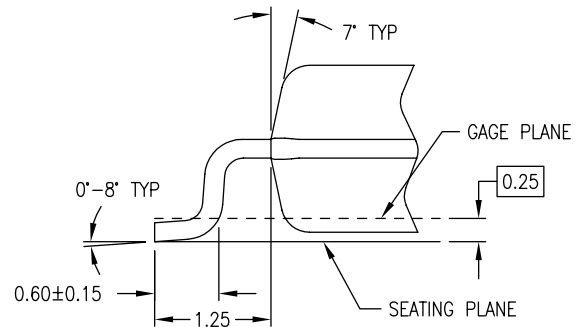
DETAIL A

M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
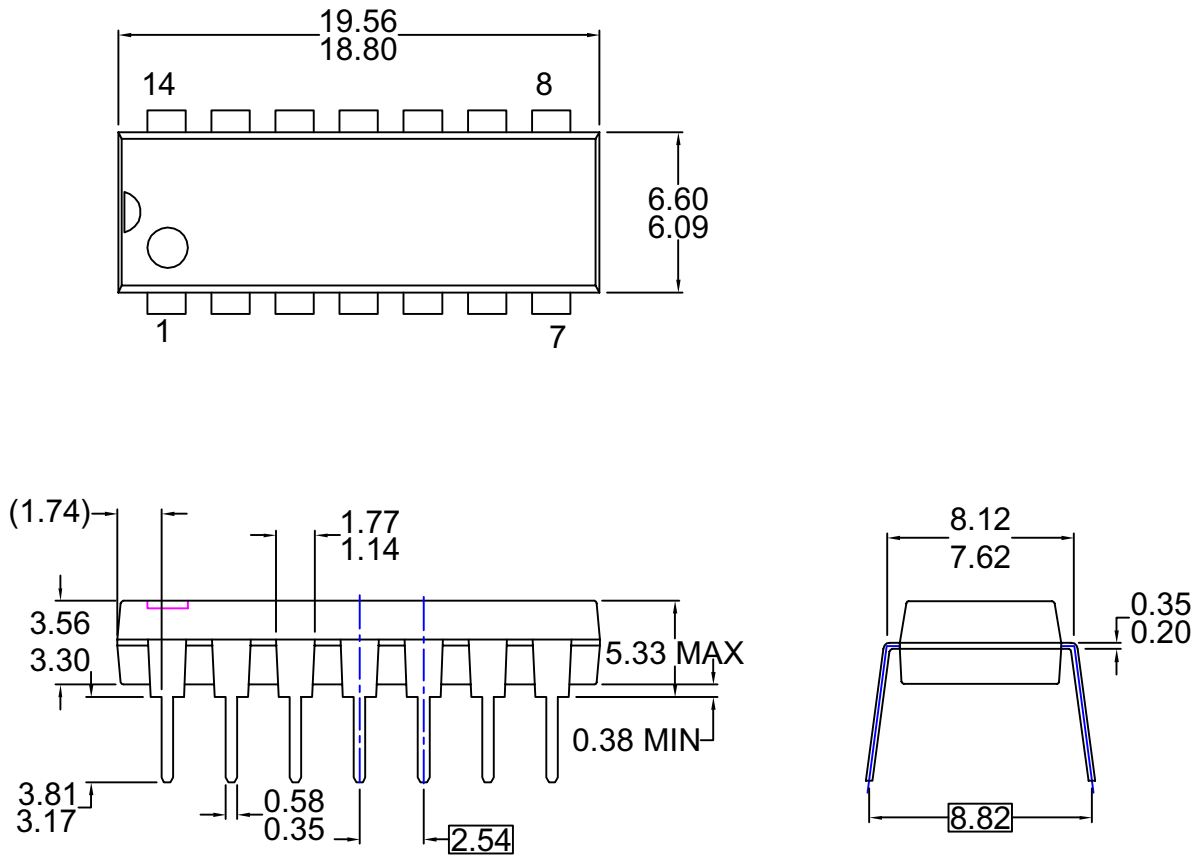
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Physical Dimensions (Continued)
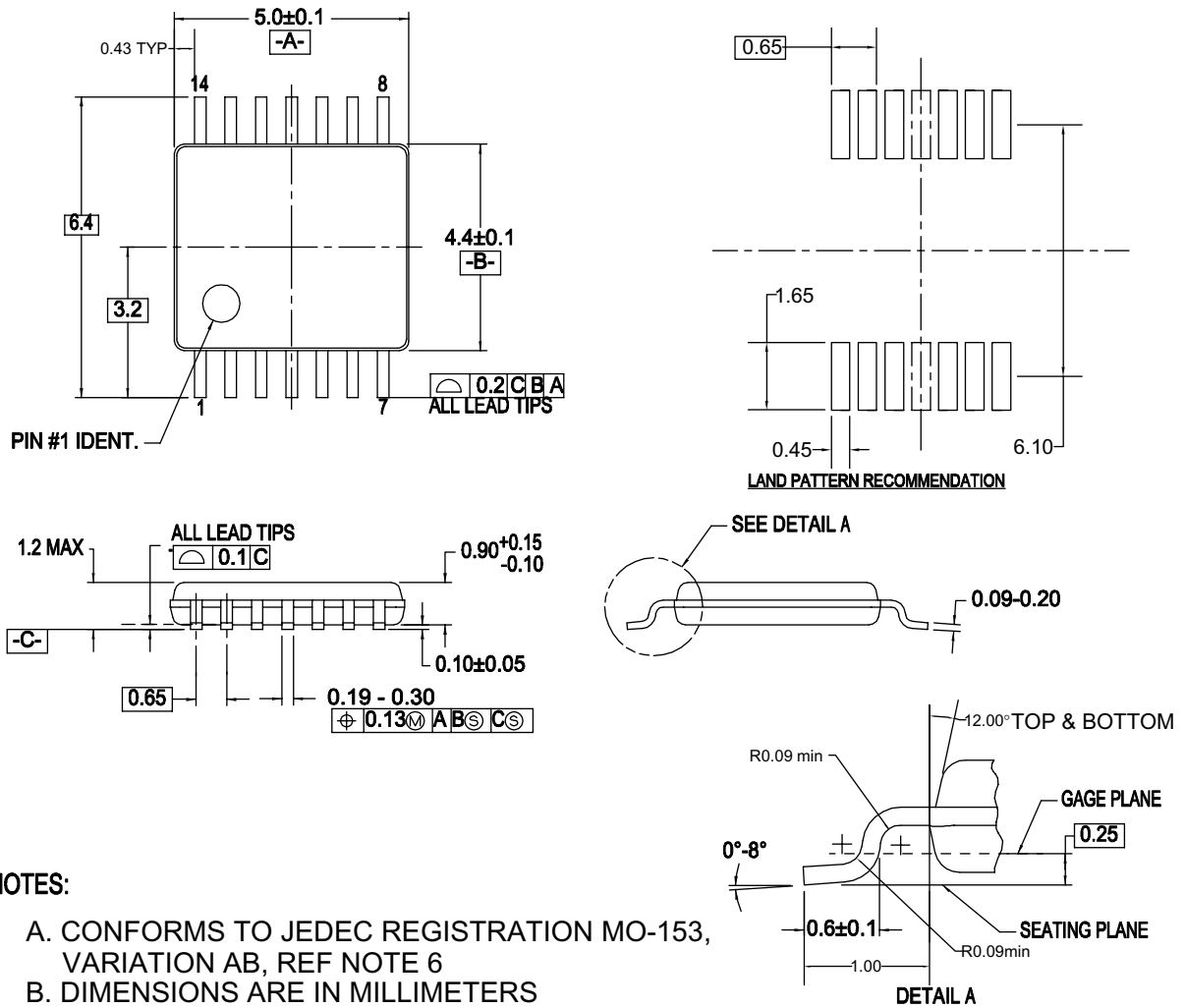
NOTES:

    A. CONFORMS TO JEDEC REGISTRATION MO-153,
       VARIATION AB, REF NOTE 6
    B. DIMENSIONS ARE IN MILLIMETERS
    C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
       AND TIE BAR EXTRUSIONS
    D. DIMENSIONING AND TOLERANCES PER ANSI
       Y14.5M, 1982
    E. LANDPATTERN STANDARD: SOP65P640X110-14M
    F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)

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  B) ALL DIMENSIONS ARE IN MILLIMETERS.
    DIMENSIONS ARE EXCLUSIVE OF BURRS,
  C) MOLD FLASH, AND TIE BAR EXTRUSIONS.
  D) DIMENSIONS AND TOLERANCES PER
    ASME Y14.5-1994
  E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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