PI74FCT273T
(25Ω Series) PI74FCT2273T

Fast CMOS Octal D Flip-Flop with Master Reset

Product Features

- PI74FCT273/2273T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: –40°C to +85°C
- Packages available:
  – 20-pin 173 mil wide plastic TSSOP (L)
  – 20-pin 300 mil wide plastic DIP (P)
  – 20-pin 150 mil wide plastic QSOP (Q)
  – 20-pin 150 mil wide plastic TQSOP (R)
  – 20-pin 300 mil wide plastic SOIC (S)

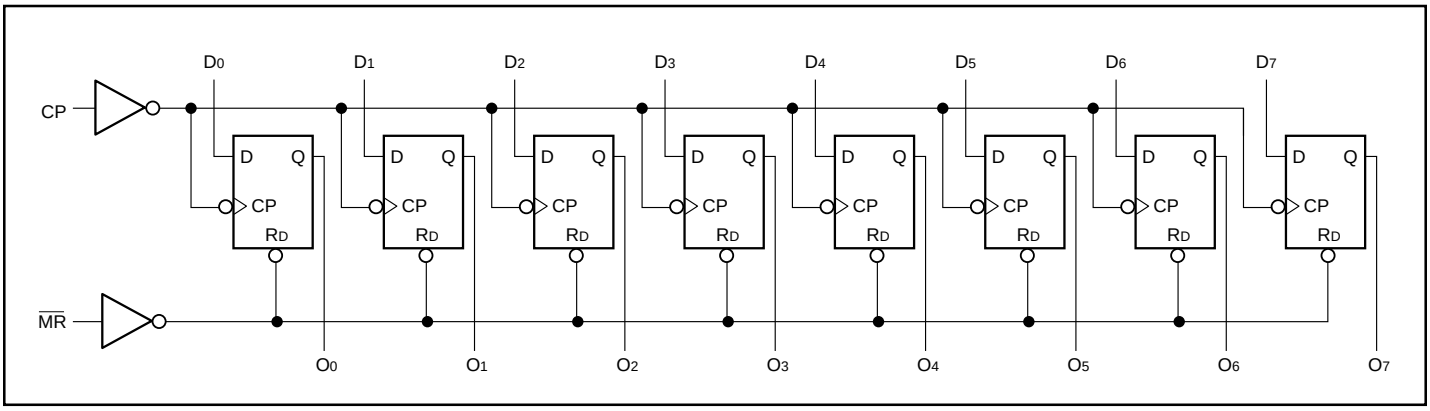
Product Description

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6/0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25-ohm series resistor on all outputs to reduce noise because of reflections, thus eliminating the need for an external terminating resistor.

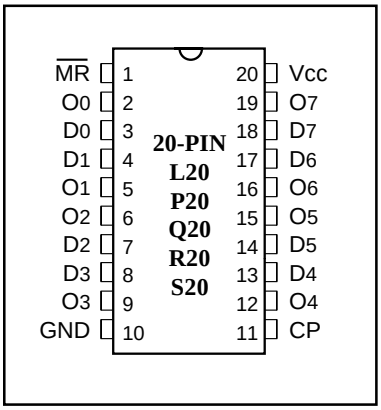
The PI74FCT273T and PI74FCT2273T is an 8-bit wide octal designed with eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) load and resets (clear) all flip-flops simultaneously. The register is fully edge-triggered. The D input state, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input.

Device models available upon request.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
D0-D7	Data Inputs
O0-O7	Data Outputs
GND	Ground
VCC	Power

Truth Table[1]

	Inputs			Outputs
Mode	**$\overline{MR}$**	**CP**	**DN**	**ON**
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

1. H = High Voltage Level
   h = High Voltage Level one setup time prior to the LOW-to-HIGH Clock transition
   L = Low Voltage Level
   l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15.0mA	2.4	3.0		V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA		0.3	0.55	V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω Series)		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			–1	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current		V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA			–0.7	–1.2	V
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5V		—	—	100	µA
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120		mA
V_H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	2.0	mA
I_{CCD}	Supply Current per Input per MHx[4]	V_{CC} = Max., Outputs Open $\overline{MR}$ = Vcc, One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		1.5	3.5[5]	mA
		$\overline{MR}$ = Vcc, 50% Duty Cycle One Bit toggling at f_i = 5 MHz	V_{IN} = 3.4V V_{IN} = GND		2.0	3.5[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		3.8	7.3[5]	
		$\overline{MR}$ = V_{CC}, 50% Duty Cycle Eight Bits toggling at f_i = 2.5 MHz, 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND		6.0	16.3[5]	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	273T/2273T Com. Min	273T/2273T Com. Max	273AT/2273AT Com. Min	273AT/2273AT Com. Max	273CT/2273CT Com. Min	273CT/2273CT Com. Max	273DT Com. Min	273DT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to On	C_L = 50pF R_L = 500Ω	2.0	13.0	2.0	7.2	2.0	5.8	2.0	4.4	ns
t_{PHL} t_{PLH}	Propagation Delay $\overline{MR}$ to On		2.0	13.0	2.0	7.2	2.0	6.1	2.0	5.0	ns
t_{SU}	Setup Time, HIGH or LOW Dn to CP		3.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time, HIGH or LOW Dn to CP		2.0	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width[3] HIGH or LOW		7.0	—	6.0	—	6.0	—	3.0	—	ns
t_W	$\overline{MR}$ Pulse Width[3] LOW		7.0	—	6.0	—	6.0	—	3.0	—	ns
t_{REM}	Recovery Time MR to CP[3]		4.0	—	2.0	—	2.0	—	2.0	—	ns

Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.