74ACT18823 18-Bit D-Type Flip-Flop with 3-STATE Outputs

General Description

FAIRCHILD

SEMICONDUCTOR

The ACT18823 contains eighteen non-inverting D-type flipflops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP), Clear (CLR), Clock Enable (EN) and Output Enable (OE) are common to each byte and can be shorted together for full 18-bit operation.

Features

- Broadside pinout allows for easy board layout
- Separate control logic for each byte
- Extra data width for wider address/data paths or buses carrying parity

August 1999

Revised October 1999

Outputs source/sink 24 mA

Connection Diagram

TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description			
74ACT18823SSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide			
74ACT18823MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide			
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.					

Jevice also available in Tape and Reel. Specify by appending sum letter "X" to the order

Logic Symbol



Pin Descriptions

Pin Names	Description
OEn	Output Enable Input (Active LOW)
CLR _n	Clear (Active LOW)
ENn	Clock Enable (Active LOW)
CPn	Clock Pulse Input
I ₀ —I ₁₇	Inputs
O ₀ -O ₁₇	Outputs

CLR.	1	\bigcirc	56	_ ср.
OE	2		55	
00 —	3		54	- 6
GND -	4		53	- GND
0, -	5		52	L 1,
o, —	6		51	- 12
V.c	7		50	- v _{cc}
0 ₃ —	8		49	- 13
۰ <u>،</u> –	9		48	L,
o ₅ —	10		47	- 1 ₅
GND -	11		46	- GNE
o ₆ —	12		45	- 1 ₆
0 ₇ —	13		44	- 17
°8 —	14		43	- 1 ₈
0 ₉ —	15		42	- Ig
٥ ₁₀ —	16		41	- 40
° ₁₁ —	17		40	- 41
GND —	18		39	- GNE
0 ₁₂ —	19		38	- 1 ₁₂
0 ₁₃ —	20		37	- 43
0 ₁₄ —	21		36	- 1 ₁₄
V _{cc} —	22		35	– v _{cc}
0 ₁₅ —	23		34	- 45
0 ₁₆ —	24		33	- 1 ₁₆
GND —	25		32	— GNE
0 ₁₇ —	26		31	- h7
0E2 -	27		30	- EN2
CLR ₂	28		29	- CP2
1				

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Functional Description

The ACT18823 consists of eighteen D-type edge-triggered flip-flops. These have 3-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. The buffered clock (CP_n) and buffered Output Enable (\overline{OE}_n) are common to all flip-flops within that byte. The flip-flops will store the state of their individual D inputs that meet set-up and hold time requirements on the LOW-to-HIGH CPn transition. With \overline{OE}_n LOW, the contents of the flip-flops are available at the outputs. When \overline{OE}_n is HIGH, the outputs go to the impedance state. Operation of the $\overline{\text{OE}}_n$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear (\overline{CLR}_n) and Clock Enable (ENn) pins. These devices are ideal for parity bus interfacing in high performance systems.

When $\overline{\text{CLR}}_n$ is LOW and $\overline{\text{OE}}_n$ is LOW, the outputs are LOW. When $\overline{\text{CLR}}_n$ is HIGH, data can be entered into the flip-flops. When $\overline{\text{EN}}_n$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{\text{EN}}_n$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

(Note 1)

	Inputs					Output	F unction
OE	CLR	EN	СР	I _n	Q	0 _n	Function
Н	Х	L	~	L	L	Z	High Z
н	х	L	~	н	н	Z	High Z
н	L	х	х	Х	L	Z	Clear
L	L	х	х	х	L	L	Clear
н	н	н	х	Х	NC	Z	Hold
L	н	н	х	х	NC	NC	Hold
н	н	L	~	L	L	Z	Load
н	н	L	~	н	н	Z	Load
L	н	L	~	L	L	L	Load
L	н	L	~	Н	Н	Н	Load

H= HIGH Voltage Level

L= LOW Voltage Level X= Immaterial

Z= High Impedance

NC= No Change

Note 1: The table represents the logic for one byte. The two bytes are independent of each other and function identically.



Logic Diagrams

Absolute Maximum Ratings(Note 2)

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Diode Current (I _{IK})	
$V_{I} = -0.5V$	–20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I _{OK})	
$V_{O} = -0.5V$	–20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V _O)	–0.5V to $V_{CC}^{} + 0.5 \text{V}$
DC Output Source/Sink Current (I _O)	± 50 mA
DC V _{CC} or Ground Current	
Per Output Pin	± 50 mA
Junction Temperature	
PDIP/SOIC	+140°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V _{CC})	4.5V to 5.5V
Input Voltage (V _I)	0V to V _{CC}
Output Voltage (V _O)	0V to V _{CC}
Operating Temperature (T _A)	$-40^{\circ}C$ to $+85^{\circ}C$
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V _{IN} from 0.8V to 2.0V	
V _{CC} @ 4.5V, 5.5V	

74ACT18823

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-out exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Sumbol	Parameter	Vcc	T _A = -	+ 25°C	$T_A = -40^{\circ}C$ to $+85^{\circ}C$	Unito	Conditions
Symbol		(V)	Тур	Gu	aranteed Limits	Units	Conditions
VIH	Minimum HIGH	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$
	Input Voltage	5.5	1.5	2.0	2.0	v	or V _{CC} –0.1V
VIL	Maximum LOW	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$
	Input Voltage	5.5	1.5	0.8	0.8	v	or V _{CC} –0.1V
V _{OH}	Minimum HIGH	4.5	4.49	4.4	4.4	V	L
	Output Voltage	5.5	5.49	5.4	5.4	v	100120 mA
							$V_{IN} = V_{IL} \text{ or } V_{IH}$
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$
		5.5		4.86	4.76		$I_{OH} = -24 \text{ mA}$ (Note 3)
V _{OL}	Maximum LOW	4.5	0.001	0.1	0.1	V	L
	Output Voltage	5.5	0.001	0.1	0.1	, v	10UT - 30 mA
							$V_{IN} = V_{IL} \text{ or } V_{IH}$
		4.5		0.36	0.44	V	$I_{OL} = 24 \text{ mA}$
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 3)
I _{OZ}	Maximum 3-STATE	5.5		+0.5	+5.0		$V_I = V_{IL}, V_{IH}$
	Leakage Current	0.0		±0.5	±0.0	μΑ	$V_{O} = V_{CC}, GND$
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μΑ	$V_I = V_{CC}, GND$
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
ICC	Maximum Quiescent Supply Current	5.5		8.0	80.0	μΑ	$V_{IN} = V_{CC}$ or GND
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 4)	0.0			-75	mA	V _{OHD} = 3.85V Min

Note 3: All outputs loaded; thresholds associated with output under test. Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

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3

74ACT18823

AC Electrical Characteristics

		V _{cc}	T _A = +25°C C _L = 50 pF		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ $C_L = 50 \text{ pF}$		Units
Symbol	Parameter	(V)					
		(Note 5)	Min	Max	Min	Max	
f _{MAX}	Maximum Clock	5.0	400				N411-
	Frequency	5.0	100		90		MHZ
t _{PHL}	Propagation Delay	5.0	2.0	9.0	2.0	9.5	
t _{PLH}	CP _n to O _n	5.0	2.0	9.0	2.0	9.5	ns
t _{PHL}	Propagation Delay	5.0	2.0	0.0	2.0	0.5	
	CLR _n to O _n	5.0	2.0	9.0	2.0	9.5	ns
t _{PZL}	Output Enable Time	5.0	2.0	9.0	2.0	10.0	
t _{PZH}		5.0	2.0	9.0	2.0	10.0	ns
t _{PLZ}	Output Disable Time	5.0	1.5	7.0	1.5	7.5	
t _{PHZ}		5.0	1.5	8.0	1.5	8.5	ns

Note 5: Voltage Range 5.0 is 5.0V \pm 0.5V.

AC Operating Requirements

		Vcc	$T_A = +25^{\circ}C$	$\textbf{T}_{\textbf{A}}=-40^{\circ}\textbf{C} \text{ to } +85^{\circ}\textbf{C}$	
Symbol	Parameter	(V)	$\mathbf{C}_{\mathbf{L}} = 50 \ \mathbf{pF}$	$\mathbf{C}_{\mathbf{L}} = 50 \ \mathbf{pF}$	Units
		(Note 6)	Guarantee	ed Minimum	
t _S	Setup Time, HIGH or LOW,	5.0	3.0	3.0	25
	Input to Clock	5.0	5.0	5.0	ns
t _H	Hold Time, HIGH or LOW,	5.0	1 5	15	20
	Input to Clock	5.0	1.5	1.5	115
t _S	Setup Time, HIGH or LOW,	5.0	3.0	3.0	25
	Enable to Clock	5.0	3.0	5.0	115
t _H	Hold Time, HIGH or LOW,	5.0	1.5	15	25
	Enable to Clock	5.0	1.5	1.5	ns
t _W	CP _n Pulse Width,	5.0	10	10	
	HIGH or LOW	5.0	4.0	4.0	ns
t _W	CLR _n Pulse Width,	5.0	1.0	1.0	
	HIGH or LOW	5.0	4.0	4.0	ns
t _{rec}	Recovery Time,	5.0		6.0	
	CLR _n to CP _n	5.0	0.0	0.0	115

Note 6: Voltage Range 5.0 is 5.0V \pm 0.5V.

Capacitance

Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Pin Capacitance	4.5	pF	$V_{CC} = 5.0V$
C _{PD}	Power Dissipation Capacitance	95	pF	$V_{CC} = 5.0V$

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