DATA SHEET

74ABT16374B

16-bit D-type flip-flop;
positive-edge trigger (3-State)

Product data
Supersedes data of 2004 Mar 01

2004 Mar 08

Philips
Semiconductors

16-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT16374B

DESCRIPTION

The 74ABT16374B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16374B has two 8-bit, edge triggered registers, with each register coupled to eight 3-State output buffers. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-LOW Output Enable ($n\overline{OE}$) controls all eight 3-State buffers for its register independent of the clock operation.

When $n\overline{OE}$ is LOW, the stored data appears at the outputs for that register. When $n\overline{OE}$ is HIGH, the outputs for that register are in the high-impedance "OFF" state, which means they will neither drive nor load the bus.

FEATURES

- Two 8-bit positive edge triggered registers
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State output buffers
- Output capability: +64 mA/–32 mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50 pF; V_{CC} = 5 V	2.6 2.2	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5 V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5 V	8	mA

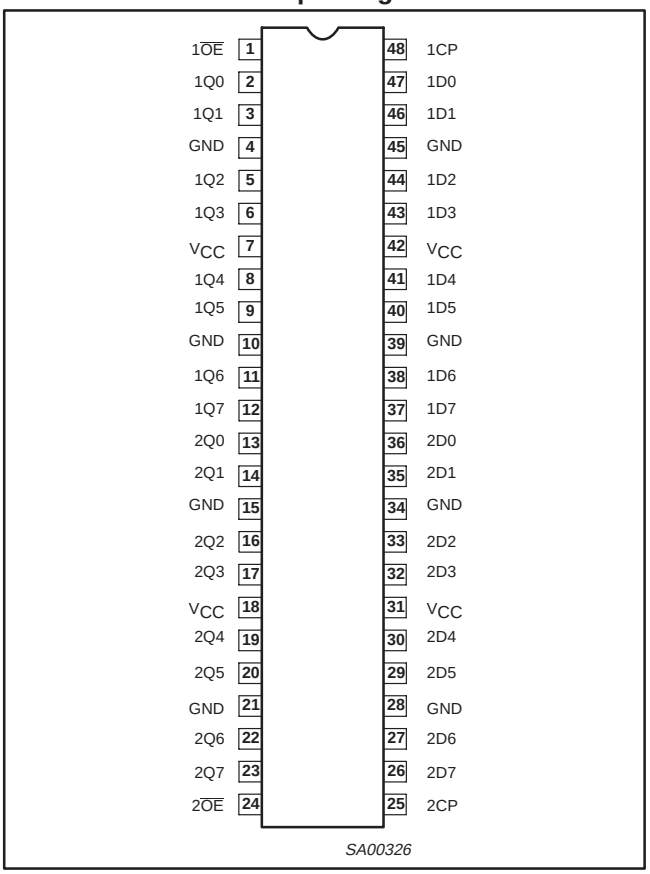
ORDERING INFORMATION

T_{amb} = –40 °C to +85 °C

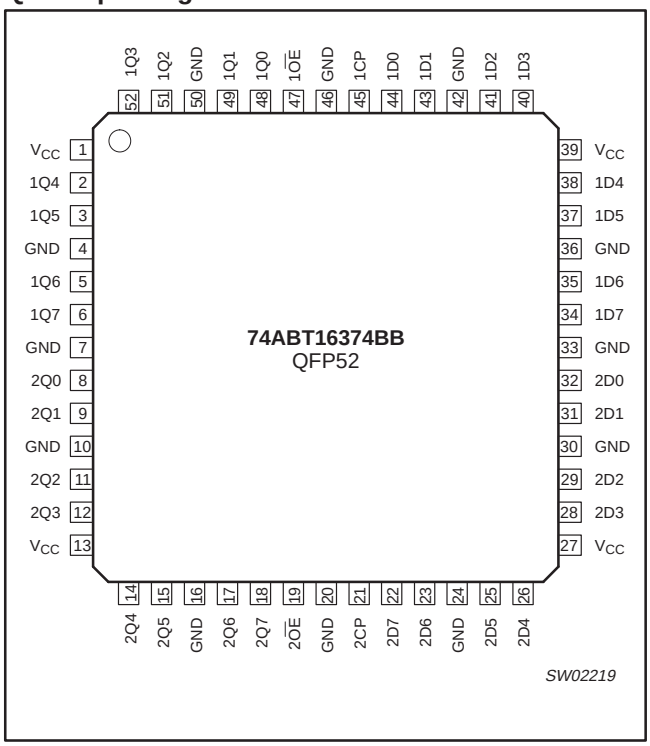
Type number	Package		
	Name	Description	Version
74ABT16374BB	QFP52	plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 × 10 × 2.0 mm	SOT379-1
74ABT16374BDGG	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ABT16374BDL	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

PIN CONFIGURATION

TSSOP48 and SSOP48 pinning



QFP52 pinning



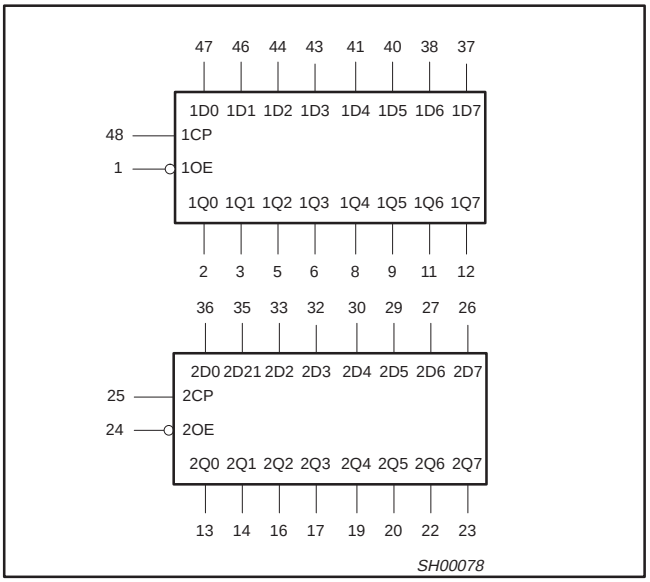
PIN DESCRIPTION

PIN NUMBER		SYMBOL	FUNCTION
TSSOP and SSOP	QFP52		
47, 46, 44, 43, 41, 40, 38, 37 36, 35, 33, 32, 30, 29, 27, 26	44, 43, 41, 40, 38, 37, 35, 34 32, 31, 29, 28, 26, 25, 23, 22	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12 13, 14, 16, 17, 19, 20, 22, 23	48, 49, 51, 52, 2, 3, 5, 6 8, 9, 11, 12, 14, 15, 17, 18	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	47, 19	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-LOW)
48, 25	45, 21	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0 V)
7, 18, 31, 42	1, 13, 27, 39	V_{CC}	Positive supply voltage

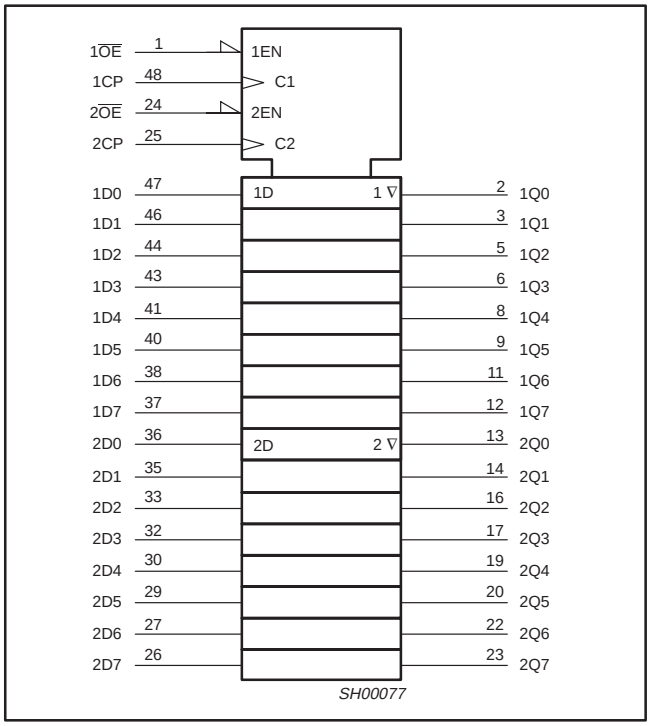
16-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT16374B

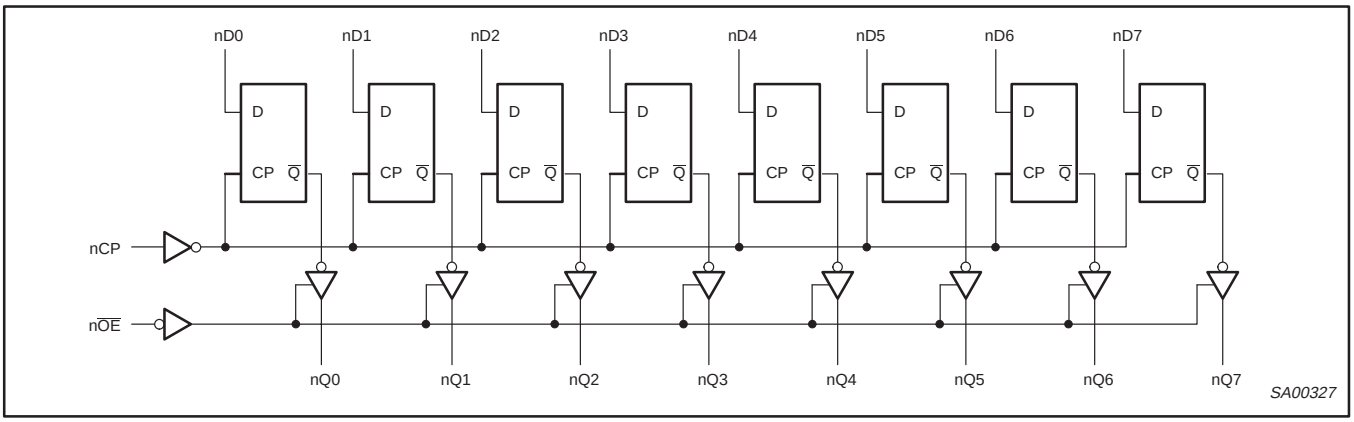
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx		nQ0 – nQ7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↥	X	NC	NC	Hold
H H	↥ ↑	X nDx	NC nDx	Z Z	Disable outputs

H = HIGH voltage level
h = HiIGH voltage level one set-up time prior to the HIGH-to-LOW E transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW E transition
NC= No change
X = Don't care
Z = High-impedance "off" state
↑ = LOW-to-HIGH clock transition
↥ = Not a LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or HIGH state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in LOW state	128	mA
		output in HIGH state	–64	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	LOW-level Input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	–32	mA
I_{OL}	LOW-level output current	–	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25 °C			T_{amb} = –40 °C to +85 °C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA	–	–0.9	–1.2	–	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	2.5	2.9	–	2.5	–	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	3.0	3.4	–	3.0	–	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA; V_I = V_{IL} or V_{IH}	2.0	2.4	–	2.0	–	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}	–	0.42	0.55	–	0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	–	0.13	0.55	–	0.55	V
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND	–	0.01	±1	–	±1	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0 V; V_O or V_I ≤ 4.5 V	–	±5.0	±100	–	±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = GND	–	±5.0	±50	–	±50	µA
I_{OZH}	3-State output HIGH current	V_{CC} = 5.5 V; V_O = 2.7 V; V_I = V_{IL} or V_{IH}	–	0.5	10	–	10	µA
I_{OZL}	3-State output LOW current	V_{CC} = 5.5 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}	–	–0.5	–10	–	–10	µA
I_{CEX}	Output HIGH leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}	–	5.0	50	–	50	µA
I_O	Output current[1]	V_{CC} = 5.5 V; V_O = 2.5 V	–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5 V; Outputs HIGH; V_I = GND or V_{CC}	–	0.5	2	–	2	mA
I_{CCL}		V_{CC} = 5.5 V; Outputs LOW; V_I = GND or V_{CC}	–	8	19	–	19	mA
I_{CCZ}		V_{CC} = 5.5 V; Outputs 3-State; V_I = GND or V_{CC}	–	0.5	2	–	2	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND	–	5	100	–	100	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 msec. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10% a transition time of up to 100 µsec is permitted.
5. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

GND = 0 V, t_R = t_F = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V			T_{amb} = –40 to +85 °C V_{CC} = +5.0V ± 0.5 V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	180	260	–	–	–	MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.7 1.4	2.6 2.2	4.0 3.4	1.7 1.4	4.7 3.9	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	3 4	1.3 1.3	2.4 2.3	3.7 3.4	1.3 1.3	4.7 4.6	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	3 4	1.9 1.7	3.1 2.6	4.6 4.0	1.9 1.7	5.5 4.4	ns

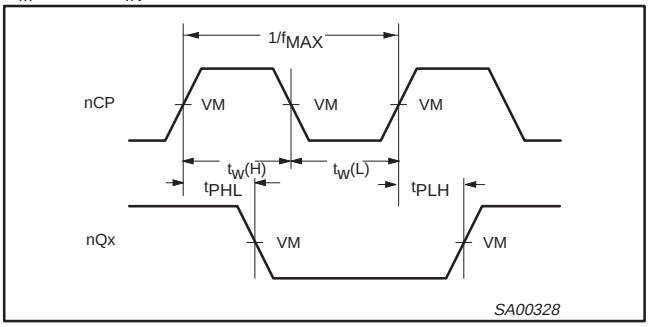
AC SET-UP REQUIREMENTS

GND = 0 V, $t_R = t_F$ = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

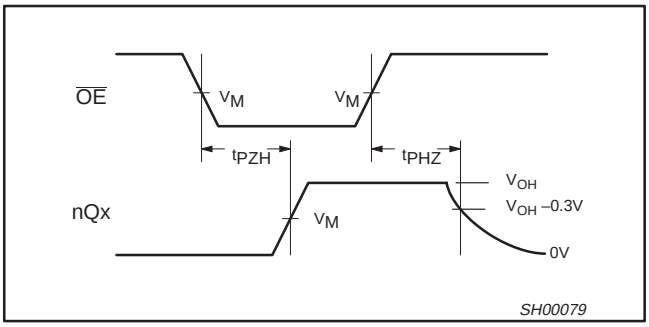
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25 °C, V_{CC} = +5.0 V		T_{amb} = –40 to +85 °C, V_{CC} = +5.0 V ± 0.5 V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW nDx to nCP	2	1.0 1.0	0.3 0.1	1.0 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW nDx to nCP	2	1.0 1.0	–0.1 –0.3	1.0 1.0	ns
$t_w(H)$ $t_w(L)$	nCP pulse width HIGH or LOW	1	2.8 2.8	1.2 1.5	2.8 2.8	ns

AC WAVEFORMS

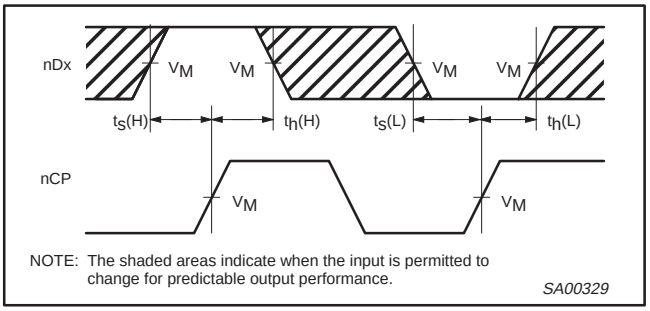
V_M = 1.5V, V_{IN} = GND to 3.0V



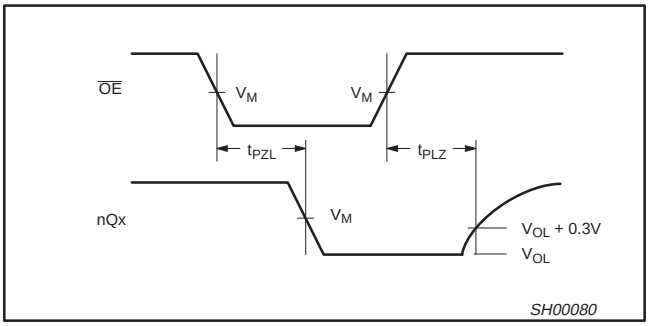
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level

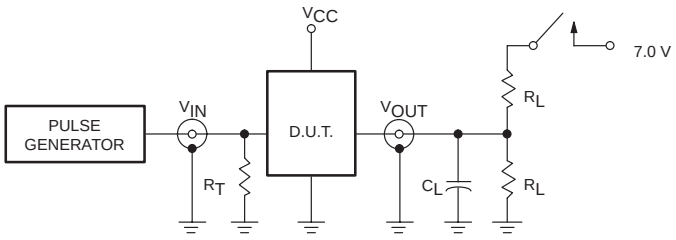


Waveform 2. Data Set-up and Hold Times

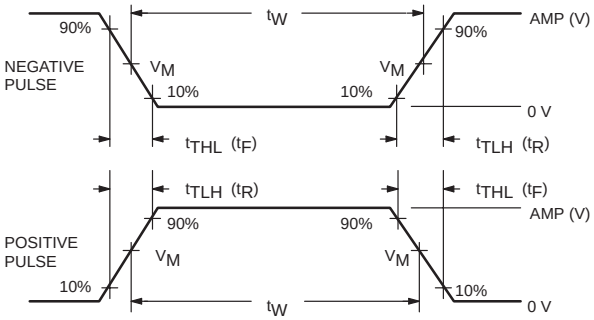


Waveform 4. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5 V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

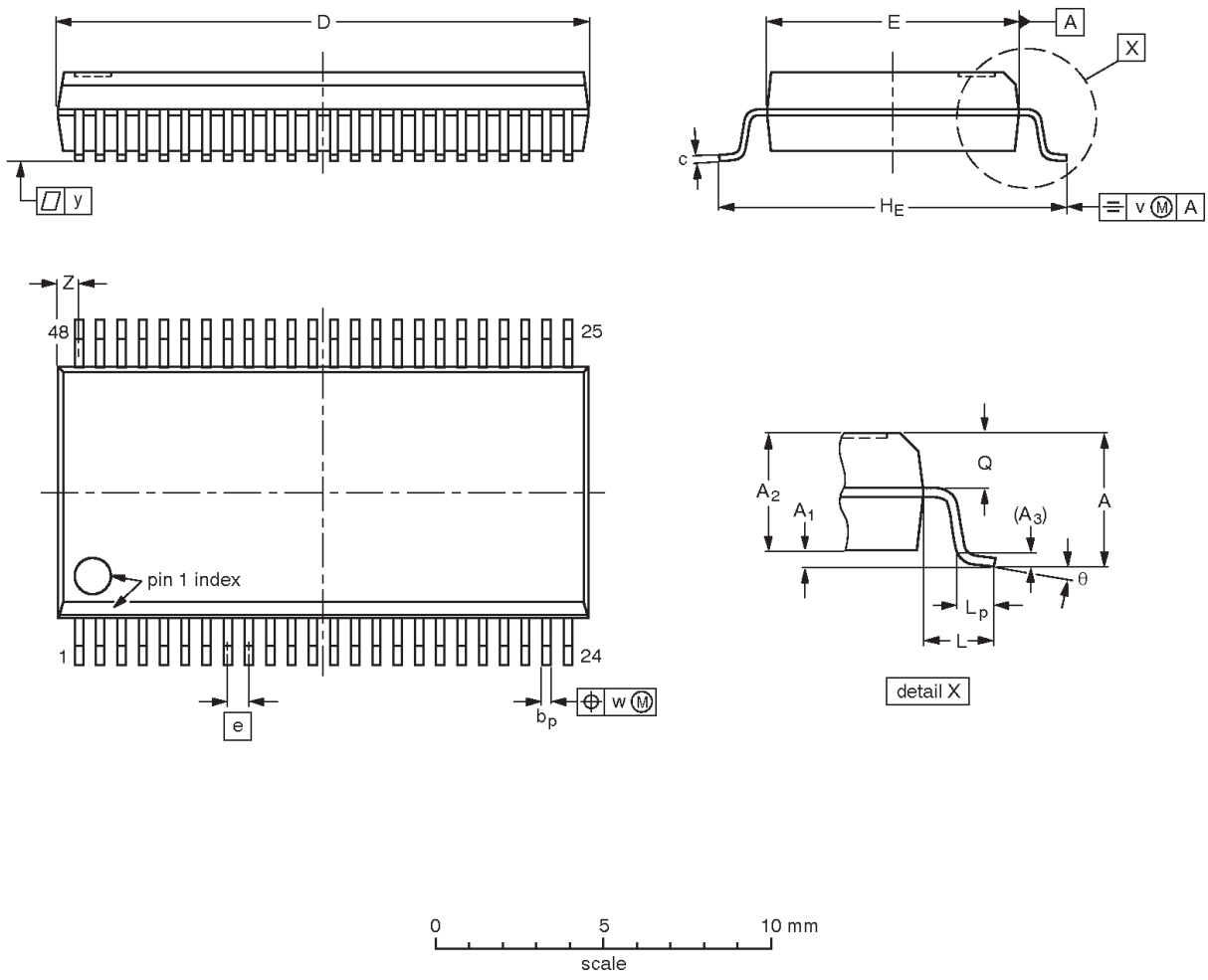
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0 V	1 MHz	500 ns	2.5 ns	2.5 ns

SA00654

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

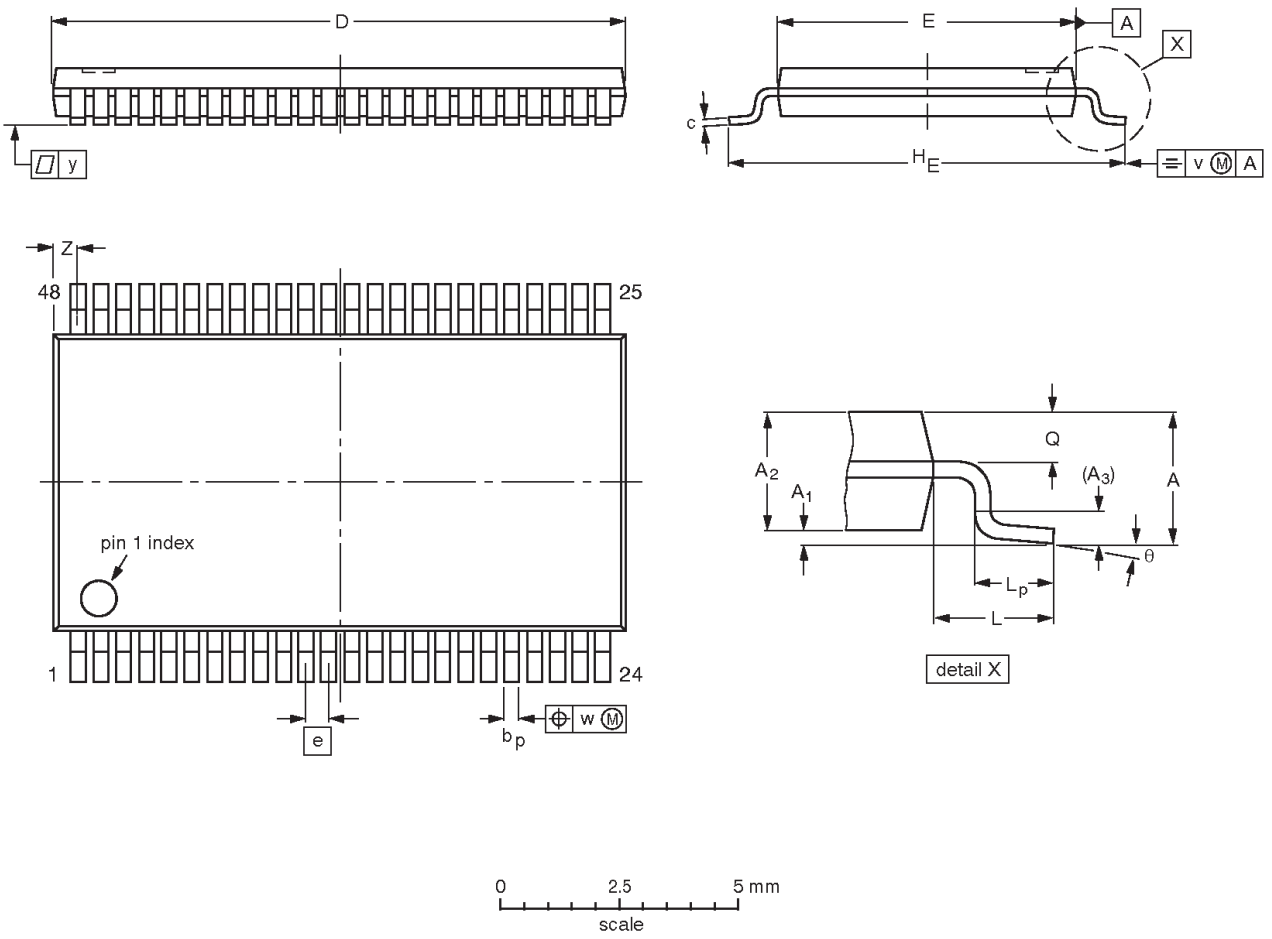
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm SOT362-1



DIMENSIONS (mm are the original dimensions).

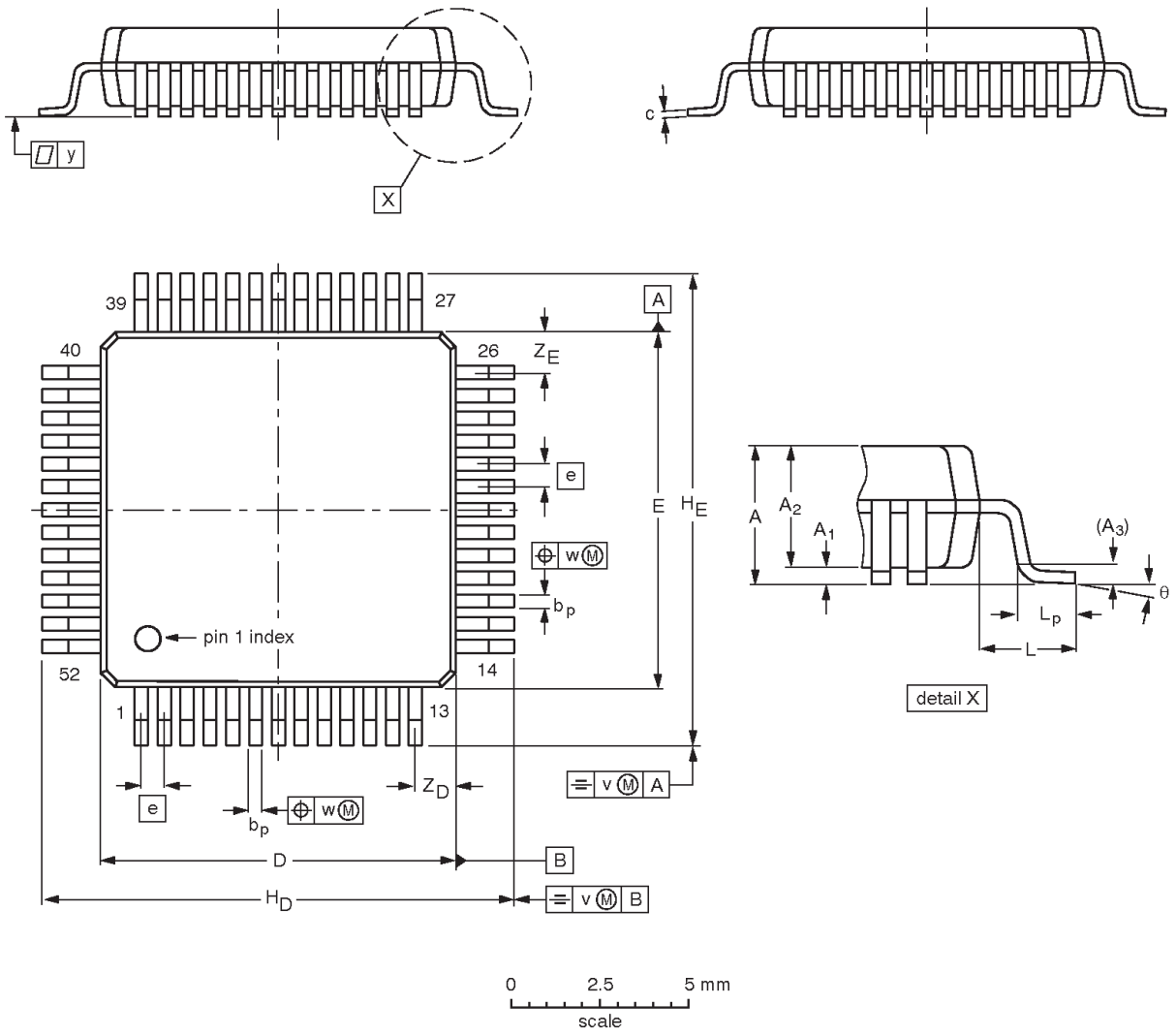
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm SOT379-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.45	0.45 0.25	2.10 1.95	0.25	0.38 0.22	0.23 0.13	10.1 9.9	10.1 9.9	0.65	13.45 12.95	13.45 12.95	1.6	0.95 0.65	0.2	0.12	0.1	1.24 0.95	1.24 0.95	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT379-1	135E04	MS-022				~~00-01-19~~ 03-02-25

REVISION HISTORY

Rev	Date	Description
_4	20040308	**Product data (9397 750 13014). Supersedes data of 2004 Mar 01 (9397 750 12988).** Modifications: ● Add type number 74ABT16374BB, QFP52 pin configuration, and SOT379-1 package outline.
_3	20040301	**Product data (9397 750 12988); 853-1752 ECN 01–A15430 of 27 January 2004. Replaces data sheet 74ABT_H16374B_2 of 1998 Feb 27 (9397 750 03496).**
_2	19980227	**Product specification (9397 750 03496); ECN 853-1752 19027 of 27 February 1998. Supersedes data of 1995 Sep 28.**
_1	19950928	

16-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT16374B

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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