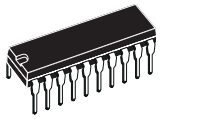
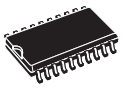
# M74HCT374

## OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT NON INVERTING

- HIGH SPEED:
  $f_{MAX}$ = 50 MHz (TYP.) at $V_{CC}$ = 4.5V
- LOW POWER DISSIPATION:
  $I_{CC}$ = 4µA(MAX.) at $T_A$=25°C
- COMPATIBLE WITH TTL OUTPUTS :
  $V_{IH}$ = 2V (MIN.) $V_{IL}$ = 0.8V (MAX)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 6mA (MIN)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 374



DIP



SOP

TSSOP

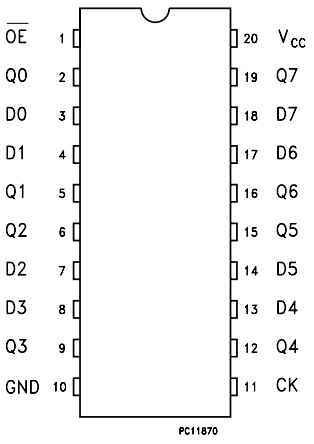
### ORDER CODES

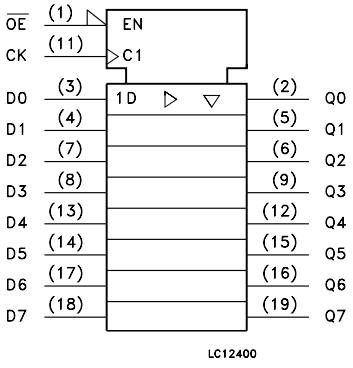
| PACKAGE | TUBE | T & R |
|---|---|---|
| DIP | M74HCT374B1R | |
| SOP | M74HCT374M1R | M74HCT374RM13TR |
| TSSOP | | M74HCT374TTR |

### DESCRIPTION

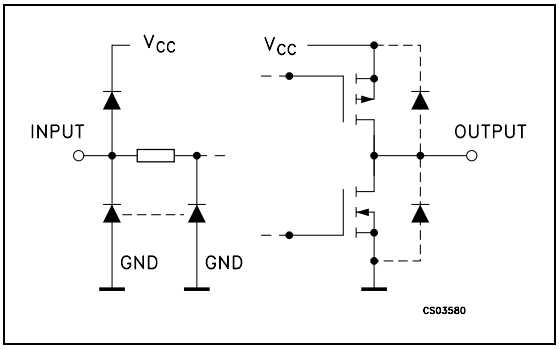
The M74HCT374 is an high speed CMOS OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS NON INVERTING fabricated with silicon gate $C^2MOS$ technology.
This 8 bit D-TYPE FLIP FLOP is controlled by a clock input (CK) and an output enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs.
While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while $\overline{OE}$ is at high level the outputs will be in a high impedance state.
The output control does not affect the internal operation of flip-flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.
The M74HCT374 is designed to directly interface $HSC^2MOS$ systems with TTL and NMOS components.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



## INPUT AND OUTPUT EQUIVALENT CIRCUIT




## PIN DESCRIPTION

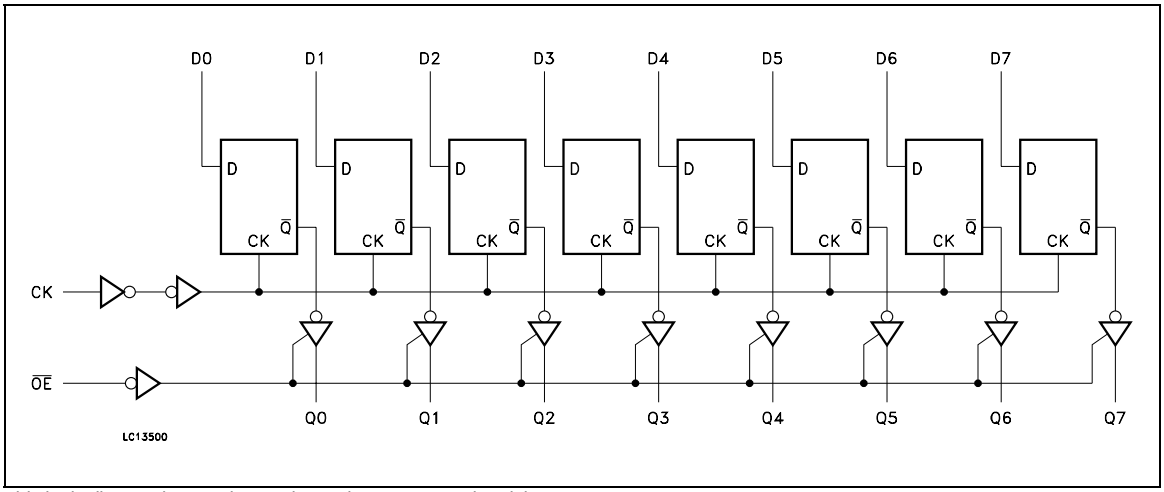
| PIN No | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | $\overline{OE}$ | 3 State Output Enable Input (Active LOW) |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q0 to Q7 | 3 State Outputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0 to D7 | Data Inputs |
| 11 | CK | Clock Input (LOW to HIGH, edge triggered) |
| 10 | GND | Ground (0V) |
| 20 | $V_{CC}$ | Positive Supply Voltage |

## TRUTH TABLE

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CK | D | Q |
| H | X | X | Z |
| L | ↓ | X | NO CHANGE |
| L | ↑ | L | L |
| L | ↑ | H | H |

X: Don't Care
Z: High Impedance

## LOGIC DIAGRAM




This logic diagram has not be used to estimate propagation delays

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.5 to +7 | V |
| $V_I$ | DC Input Voltage | -0.5 to $V_{CC}$ + 0.5 | V |
| $V_O$ | DC Output Voltage | -0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | ± 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Current | ± 35 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | ± 70 | mA |
| $P_D$ | Power Dissipation | 500(*) | mW |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 to 5.5 | V |
| $V_I$ | Input Voltage | 0 to $V_{CC}$ | V |
| $V_O$ | Output Voltage | 0 to $V_{CC}$ | V |
| $T_{op}$ | Operating Temperature | -55 to 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time ($V_{CC}$ = 4.5 to 5.5V) | 0 to 500 | ns |

## DC SPECIFICATION

| Symbol | Parameter | Test Condition | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 4.5 to 5.5 | | 2.0 | | | 2.0 | | 2.0 | | V |
| $V_{IL}$ | Low Level Input Voltage | 4.5 to 5.5 | | | | 0.8 | | 0.8 | | 0.8 | V |
| $V_{OH}$ | High Level Output Voltage | 4.5 | $I_O$=-20 µA | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | | $I_O$=-6.0 mA | 4.18 | 4.31 | | 4.13 | | 4.10 | | |
| $V_{OL}$ | Low Level Output Voltage | 4.5 | $I_O$=20 µA | | 0.0 | 0.1 | | 0.1 | | 0.1 | V |
| | | | $I_O$=6.0 mA | | 0.17 | 0.26 | | 0.33 | | 0.40 | |
| $I_I$ | Input Leakage Current | 5.5 | $V_I$ = $V_{CC}$ or GND | | | ± 0.1 | | ± 1 | | ± 1 | µA |
| $I_{OZ}$ | High Impedance Output Leakage Current | 5.5 | $V_I$ = $V_{IH}$ or $V_{IL}$<br>$V_O$ = $V_{CC}$ or GND | | | ± 0.5 | | ± 5 | | ± 10 | µA |
| $I_{CC}$ | Quiescent Supply Current | 5.5 | $V_I$ = $V_{CC}$ or GND | | | 4 | | 40 | | 80 | µA |
| $\Delta I_{CC}$ | Additional Worst Case Supply Current | 5.5 | Per Input pin<br>$V_I$ = 0.5V or<br>$V_I$ = 2.4V<br>Other Inputs at<br>$V_{CC}$ or GND<br>$I_O$ = 0 | | | 2.0 | | 2.9 | | 3.0 | mA |

## AC ELECTRICAL CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6ns)

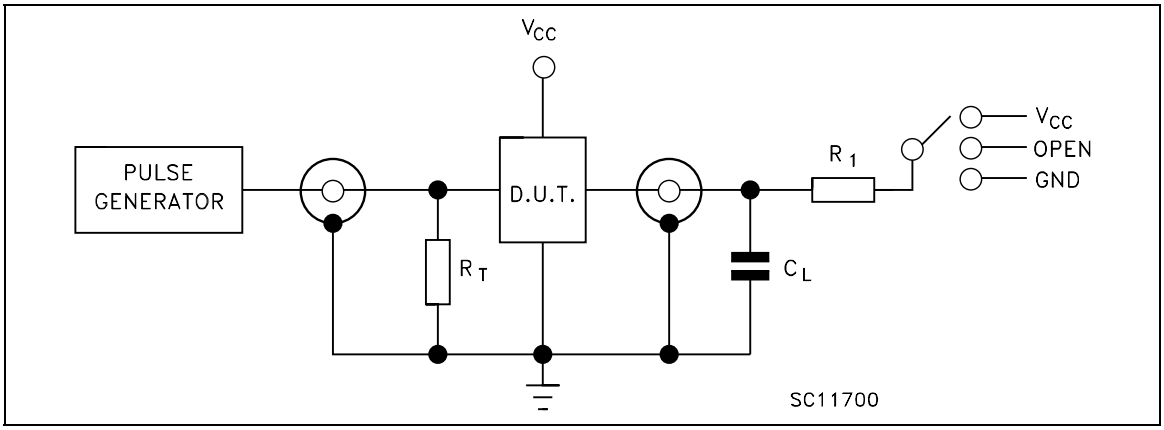
| Symbol | Parameter | Test Condition | | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | $C_L$ (pF) | | $T_A$ = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | 4.5 | 50 | | | 7 | 12 | | 15 | | 18 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (CLOCK-Q,Q) | 4.5 | 50 | | | 20 | 30 | | 38 | | 45 | ns |
| | | 4.5 | 150 | | | 25 | 38 | | 48 | | 57 | |
| $t_{PZL}$ $t_{PZH}$ | Output Enable Time | 4.5 | 50 | $R_L$ = 1 KΩ | | 17 | 30 | | 38 | | 45 | ns |
| | | 4.5 | 150 | | | 25 | 38 | | 48 | | 57 | |
| $t_{PLZ}$ $t_{PHZ}$ | Output Disable Time | 4.5 | 50 | $R_L$ = 1 KΩ | | 16 | 28 | | 35 | | 42 | ns |
| $f_{MAX}$ | Maximum Clock Frequency | 4.5 | 50 | | 31 | 50 | | 25 | | 21 | | MHz |
| $t_{W(L)}$ $t_{W(H)}$ | Minimum Pulse Width (CLOCK) | 4.5 | 50 | | | | 15 | | 19 | | 23 | ns |
| $t_s$ | Minimum Set-Up Time | 4.5 | 50 | | | | 15 | | 19 | | 23 | ns |
| $t_h$ | Minimum Hold Time | 4.5 | 50 | | | | 0 | | 0 | | 0 | ns |

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Test Condition | | Value | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $C_{IN}$ | Input Capacitance | | | | 5 | 10 | | 10 | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | | | 10 | | | | | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (note 1) | | | | 48 | | | | | | pF |

1) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per Flip Flop) and the $C_{PD}$ when n pcs of Flip Flop operate, can be gained by the following equation: $C_{PD(TOTAL)} = 30 + 18 \times n$ (pF)

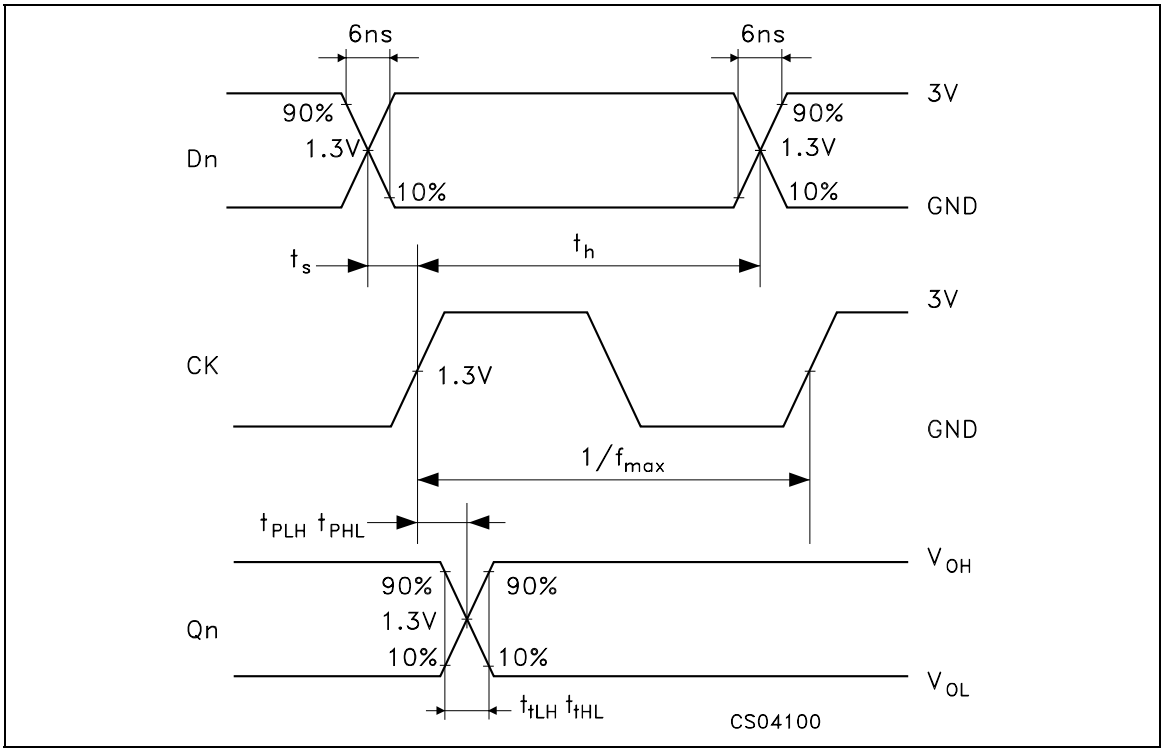
## TEST CIRCUIT



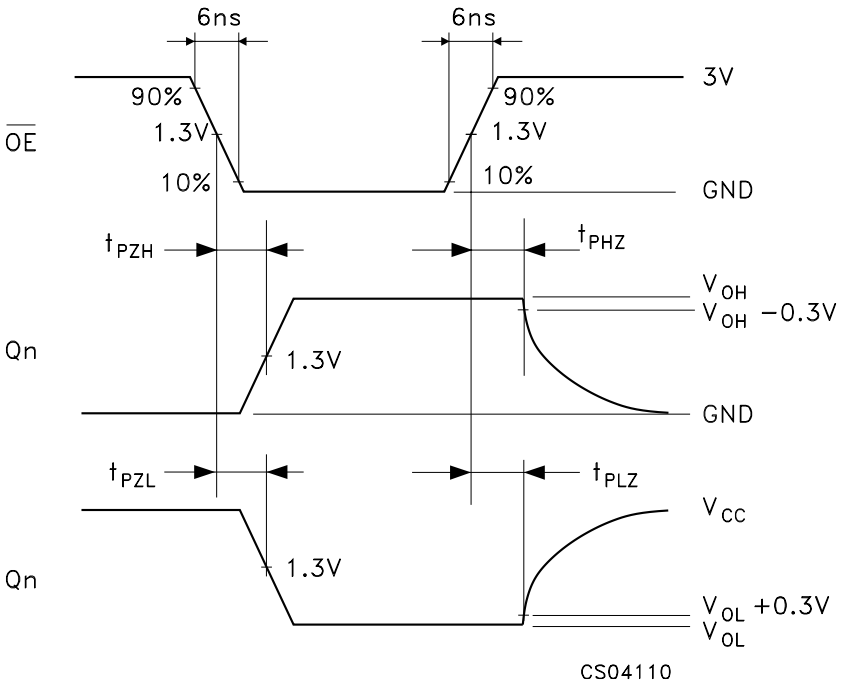

| TEST | SWITCH |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | $V_{CC}$ |
| $t_{PZH}$, $t_{PHZ}$ | GND |

$C_L$ = 50pF/150pF or equivalent (includes jig and probe capacitance)
$R_1$ = 1KΩ or equivalent
$R_T$ = $Z_{OUT}$ of pulse generator (typically 50Ω)

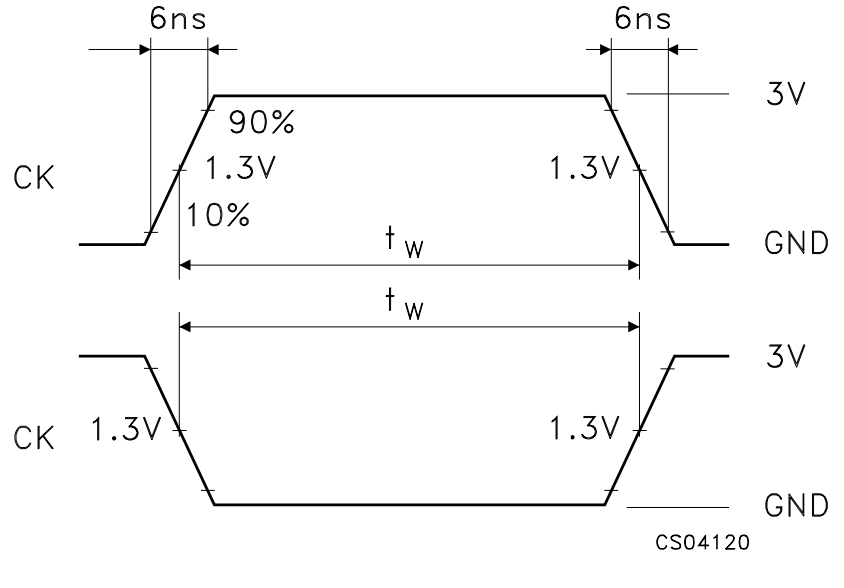
**WAVEFORM 1: CK TO Qn PROPAGATION DELAYS, MAXIMUM CK FREQUENCY, Dn TO CK SETUP AND HOLD TIMES** (f=1MHz; 50% duty cycle)



**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES** (f=1MHz; 50% duty cycle)

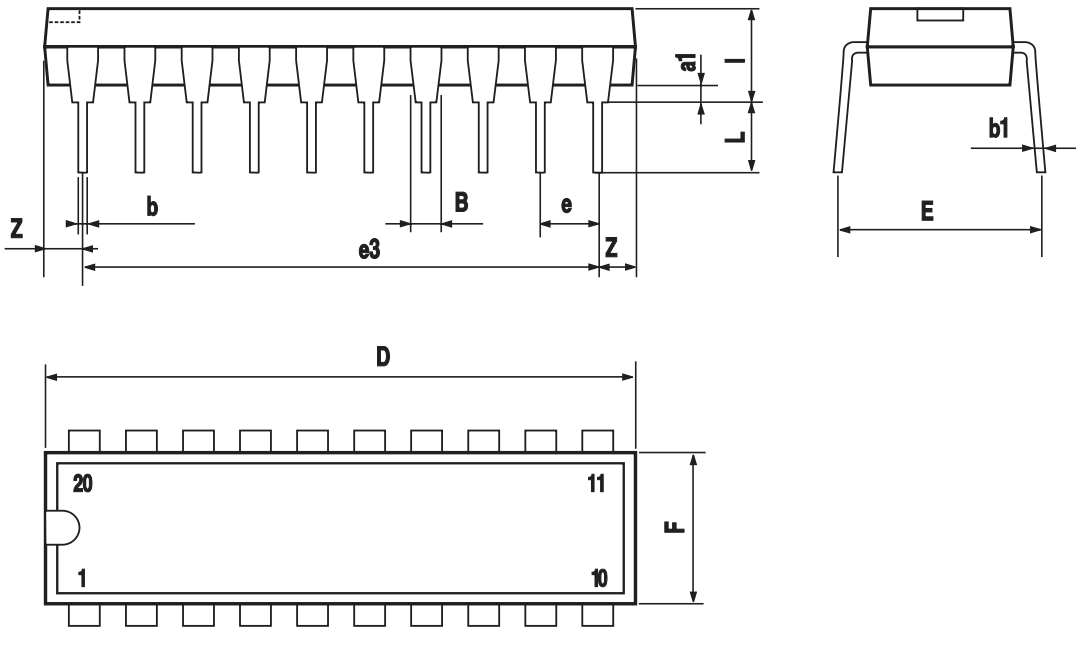



**WAVEFORM 3: MINIMUM PULSE WIDTH (CK)** (f=1MHz; 50% duty cycle)



## Plastic DIP-20 (0.25) MECHANICAL DATA

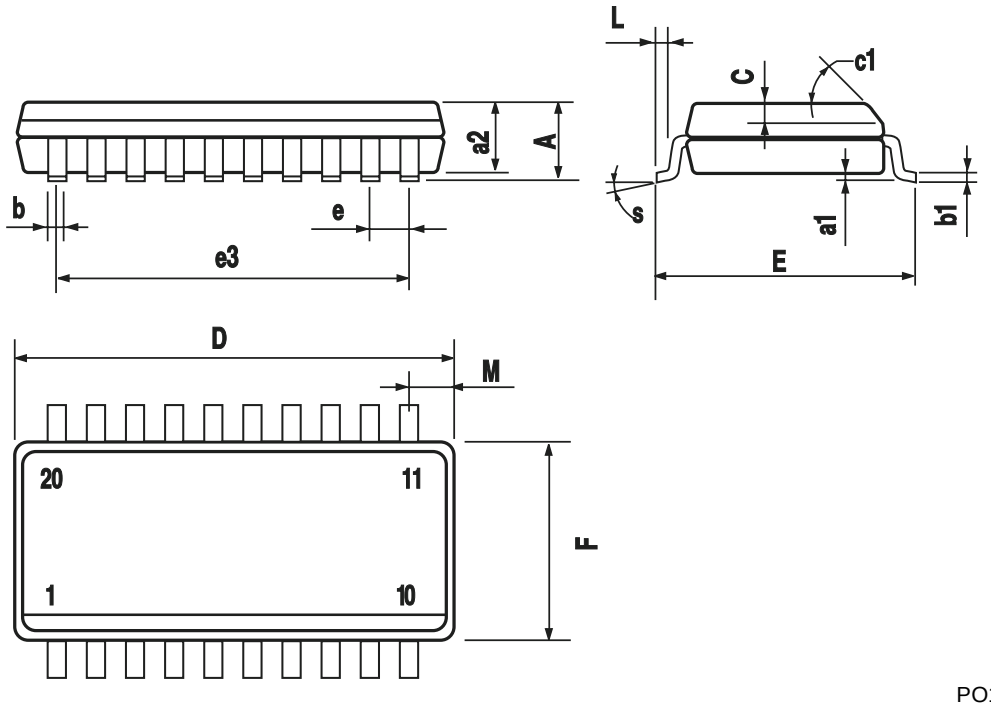
| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.254 | | | 0.010 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| b | | 0.45 | | | 0.018 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 25.4 | | | 1.000 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 22.86 | | | 0.900 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 3.93 | | | 0.155 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.34 | | | 0.053 |




P001J

## SO-20 MECHANICAL DATA

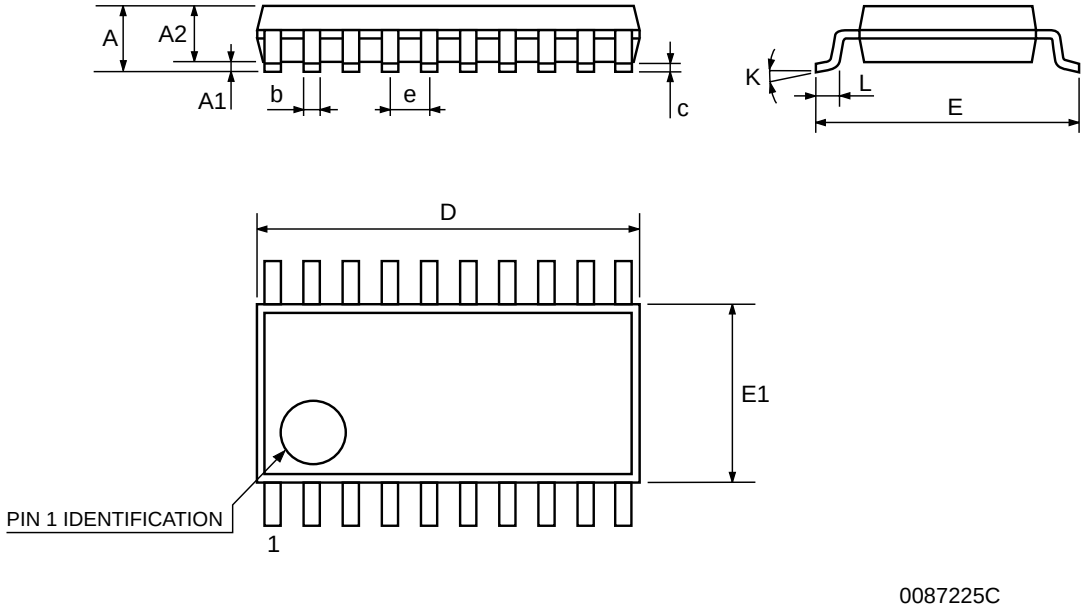
| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 12.60 | | 13.00 | 0.496 | | 0.512 |
| E | 10.00 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 11.43 | | | 0.450 | |
| F | 7.40 | | 7.60 | 0.291 | | 0.300 |
| L | 0.50 | | 1.27 | 0.020 | | 0.050 |
| M | | | 0.75 | | | 0.029 |
| S | 8° (max.) | | | | | |




PO13L

## TSSOP20 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 6.4 | 6.5 | 6.6 | 0.252 | 0.256 | 0.260 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |

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