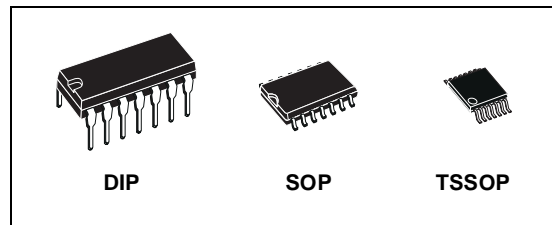


## DUAL D TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED :  
 $f_{MAX} = 67\text{MHz}$  (TYP.) at  $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 2\mu\text{A}$  (MAX.) at  $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4\text{mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH  
 74 SERIES 74



### ORDER CODES

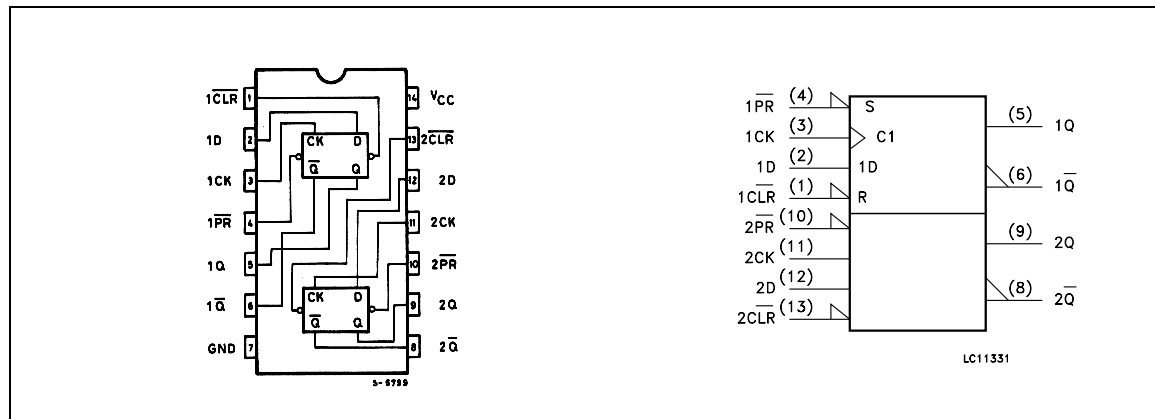
PACKAGE	TUBE	T & R
DIP	M74HC74B1R	
SOP	M74HC74M1R	M74HC74RM13TR
TSSOP		M74HC74TTR

### DESCRIPTION

The M74HC74 is an high speed CMOS DUAL D TYPE FLIP FLOP WITH CLEAR fabricated with silicon gate C<sup>2</sup>MOS technology. A signal on the D INPUT is transferred on the Q OUTPUT during the positive going transition of the clock pulse. CLEAR and PRESET are

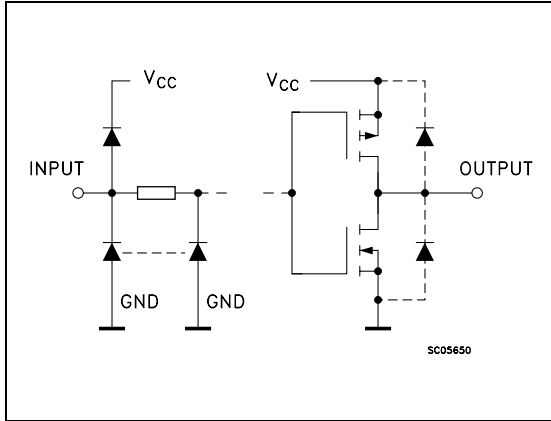
independent of the clock and accomplished by a low on the appropriate input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



# M74HC74

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## PIN DESCRIPTION

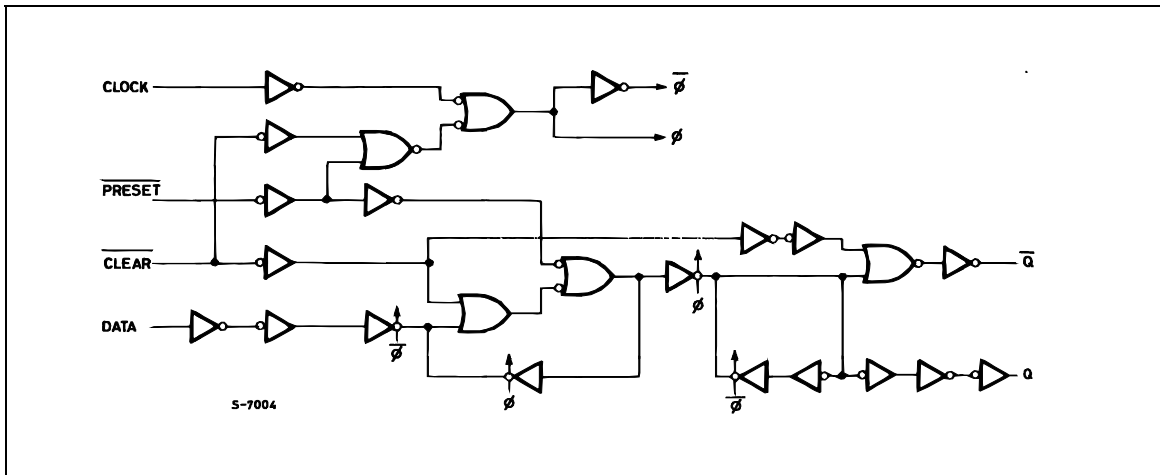
PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{\text{CLR}}, 2\overline{\text{CLR}}$	Asynchronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW-to-HIGH, Edge-Triggered)
4, 10	$1\overline{\text{PR}}, 2\overline{\text{PR}}$	Asynchronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	$1\overline{\text{Q}}, 2\overline{\text{Q}}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	Vcc	Positive Supply Voltage

## TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	----
H	H	L	$\downarrow$	L	H	----
H	H	H	$\uparrow$	H	L	----
H	H	X	$\uparrow$	$Q_n$	$\overline{Q}_n$	NO CHANGE

X : Don't Care

## LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$P_D$	Power Dissipation	500(*)	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(\*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_{op}$	Operating Temperature	-55 to 125	°C	
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V <sub>OH</sub>	High Level Output Voltage	2.0	I <sub>O</sub> =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I <sub>O</sub> =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I <sub>O</sub> =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I <sub>O</sub> =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I <sub>O</sub> =-5.2 mA	5.68	5.8		5.63		5.60		
V <sub>OL</sub>	Low Level Output Voltage	2.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		6.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I <sub>O</sub> =5.2 mA		0.18	0.26		0.33		0.40	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			2		20		40	μA

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

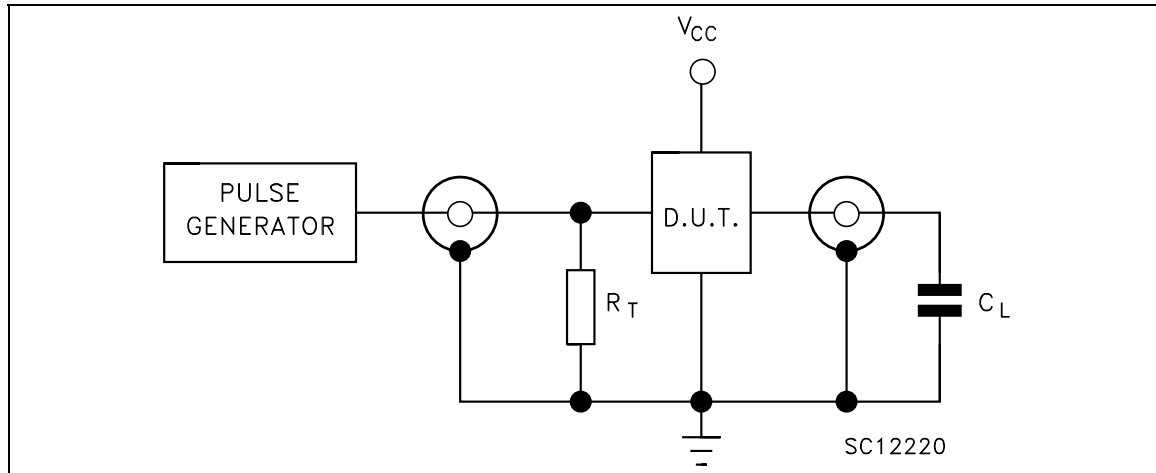
Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH}$ $t_{THL}$	Output Transition Time	2.0			30	75		95		110	ns
					8	15		19		22	
					7	13		16		19	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CK - Q, $\bar{Q}$ )	2.0			48	150		190		225	ns
					16	30		38		45	
					13	26		32		38	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLR, PR - Q, $\bar{Q}$ )	2.0			51	150		190		225	ns
					17	30		38		45	
					15	26		32		38	
$f_{MAX}$	Maximum Clock Frequency	2.0		6.2	21		5		4.2		MHz
				31	63		25		21		
				37	67		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	2.0			18	75		95		110	ns
					6	15		19		22	
					6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLR, PR)	2.0			21	75		95		110	ns
					7	15		19		22	
					6	13		16		19	
$t_s$	Minimum Set-up Time	2.0			15	75		95		110	ns
					4	15		19		22	
					3	13		16		19	
$t_h$	Minimum Hold Time	2.0			0			0		0	ns
					0			0		0	
					0			0		0	
$t_{REM}$	Minimum Removal Time (CLR, PR to CK)	2.0			0	25		30		35	ns
					0	5		6		7	
					0	4		5		6	

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$C_{IN}$	Input Capacitance	5.0			5	10		10		10	pF
$C_{PD}$	Power Dissipation Capacitance (note 1)	5.0			34						pF

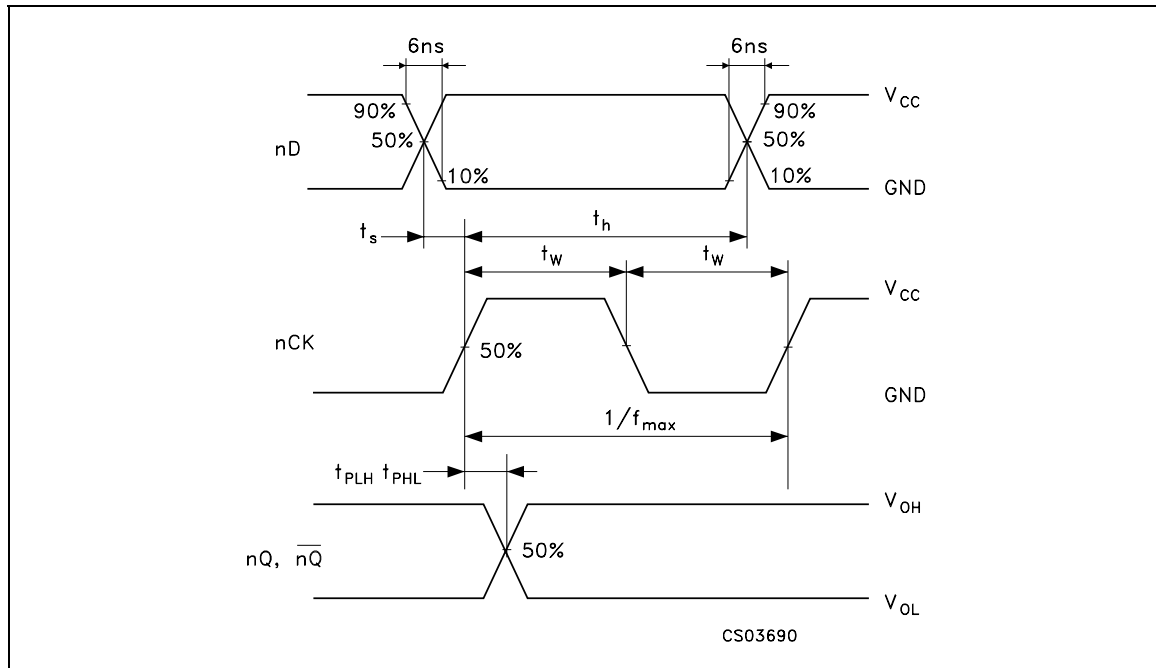
1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(OP)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$  (per FLIP/FLOP)

TEST CIRCUIT

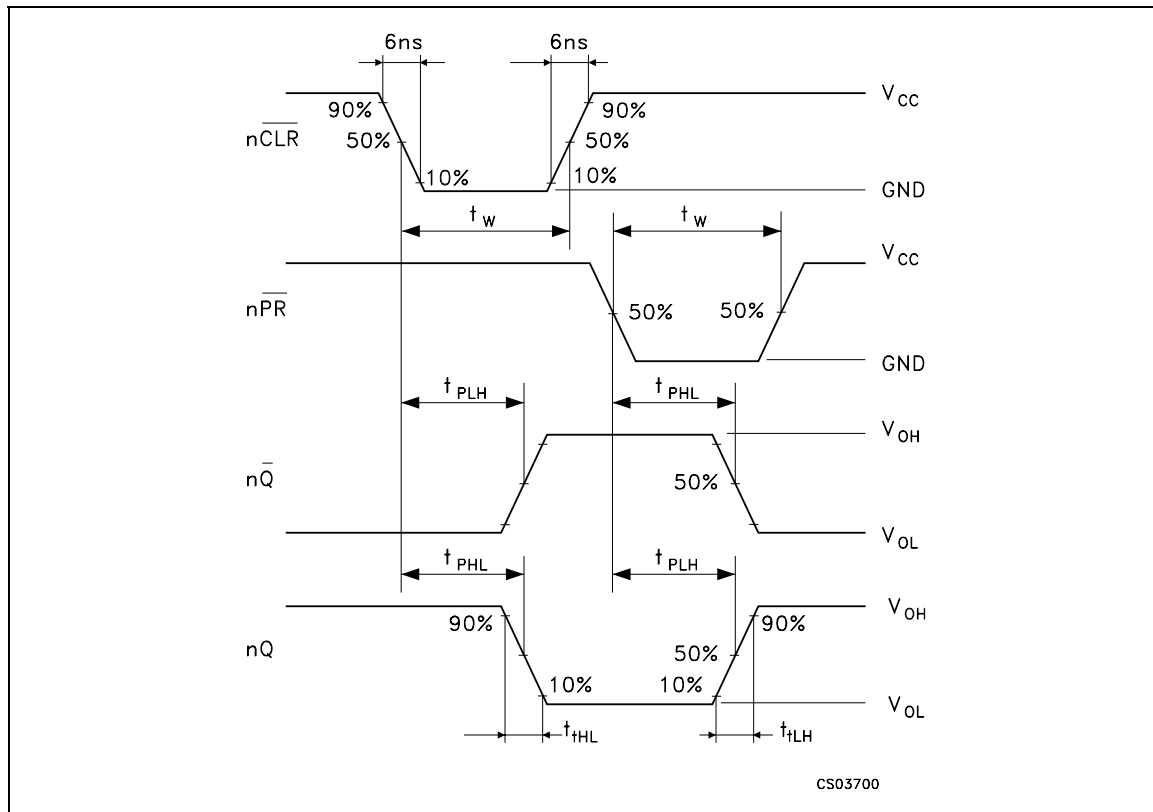


$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

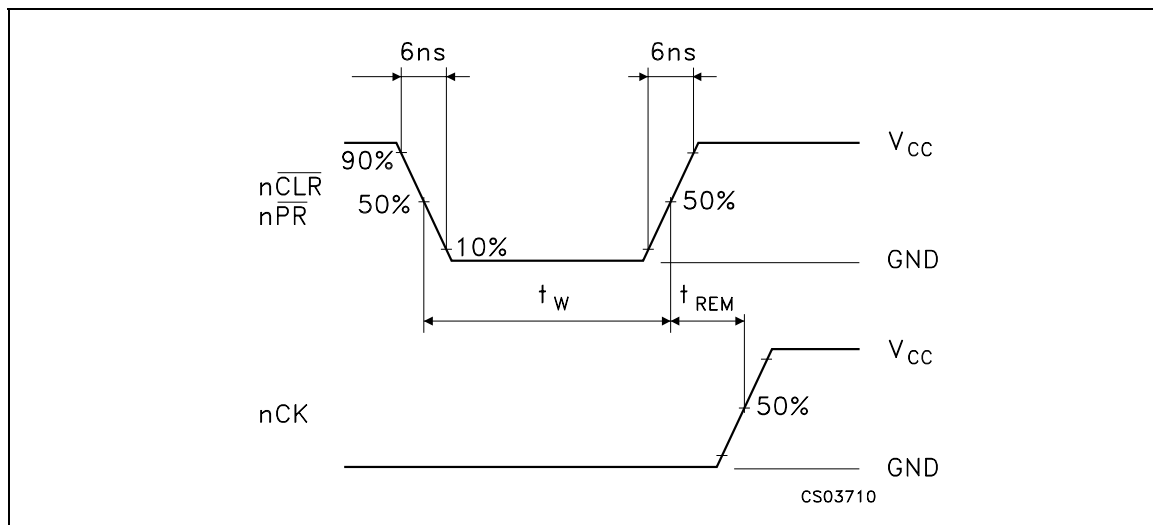
**WAVEFORM 1: nCK TO nQ,  $\overline{nQ}$  PROPAGATION DELAY TIMES, nD TO nCK SETUP AND HOLD TIMES, nCK MINIMUM PULSE WIDTH, MAXIMUM nCK FREQUENCY ( $f=1\text{MHz}$ ; 50% duty cycle)**



**WAVEFORM 2 : nQ , nQ̄ TO CLR, PR PROPAGATION DELAY TIMES, MINIMUM PULSE WIDTH (nCLR and nPR) (f=1MHz; 50% duty cycle)**

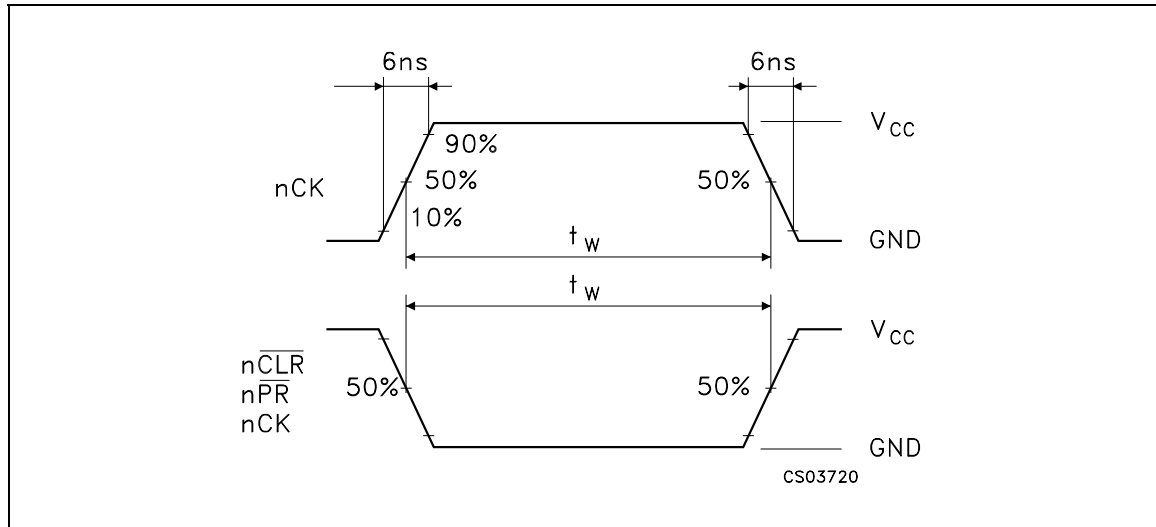


**WAVEFORM 3 : MINIMUM PULSE WIDTH (nCLR and nPR), MINIMUM REMOVAL TIME (nCLR and nPR TO nCK) (f=1MHz; 50% duty cycle)**



## M74HC74

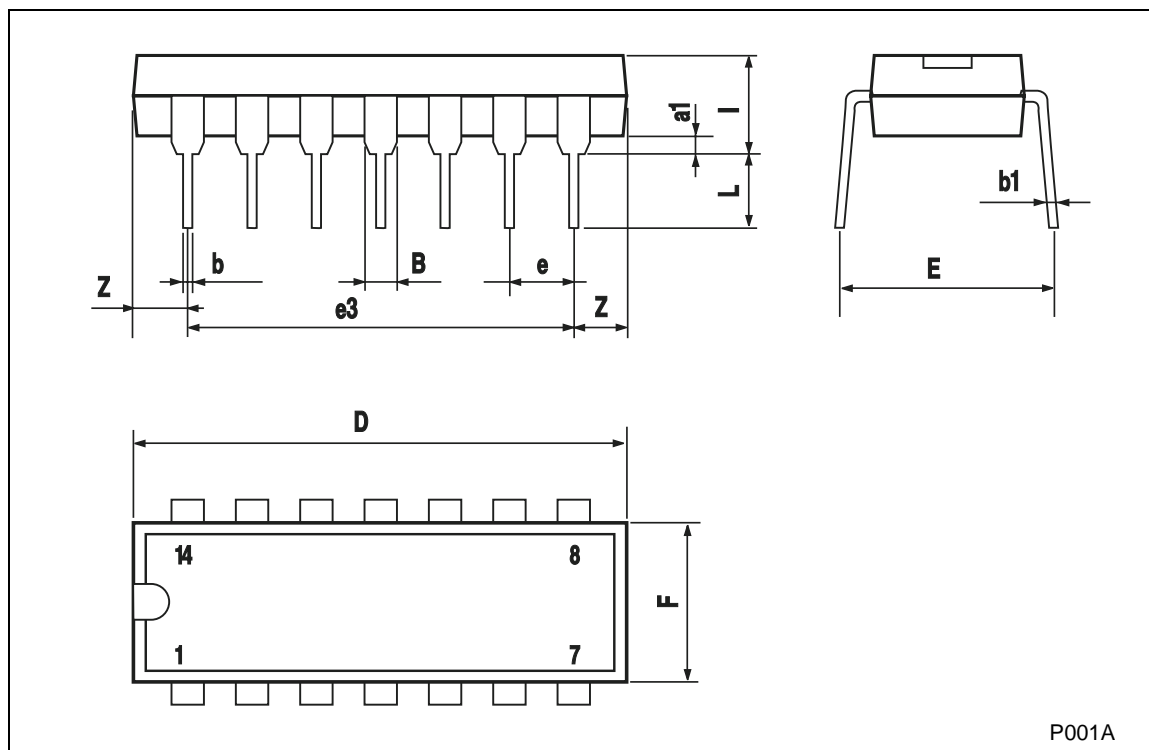
**WAVEFORM 4 : MINIMUM PULSE WIDTH ( $\overline{nCLR}$ ,  $\overline{nPR}$ ,  $nCK$ ) ( $f=1\text{MHz}$ ; 50% duty cycle)**





## Plastic DIP-14 MECHANICAL DATA

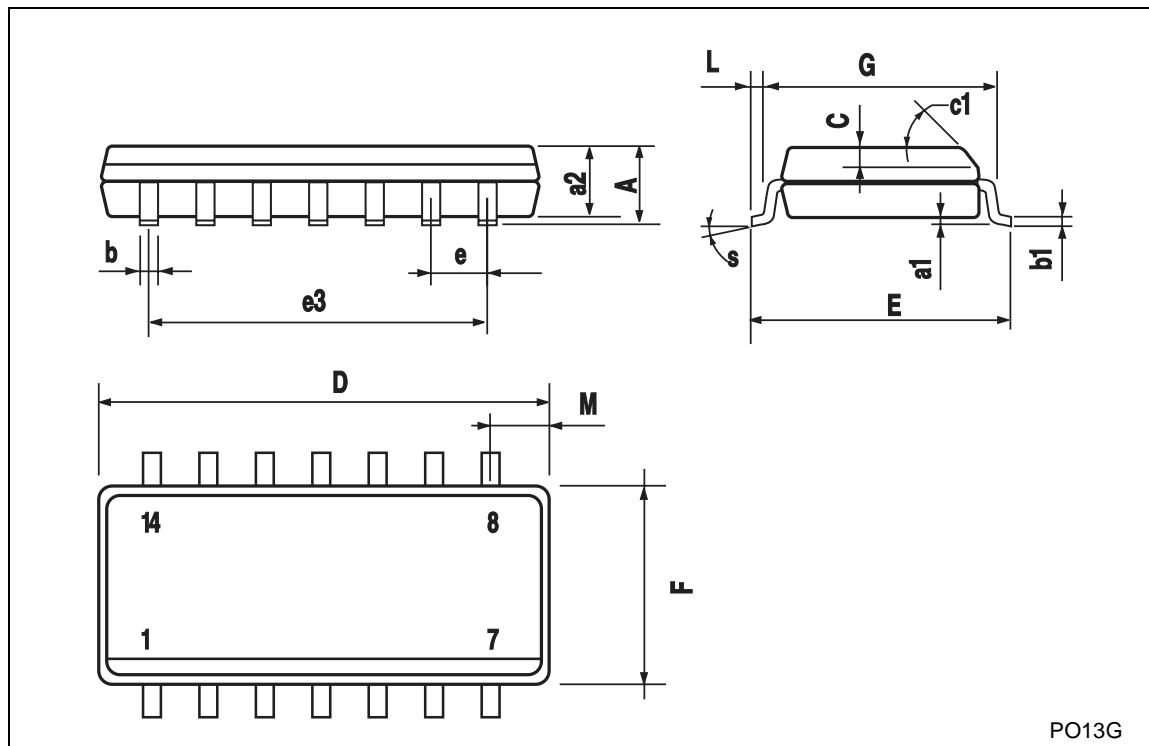
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

## SO-14 MECHANICAL DATA

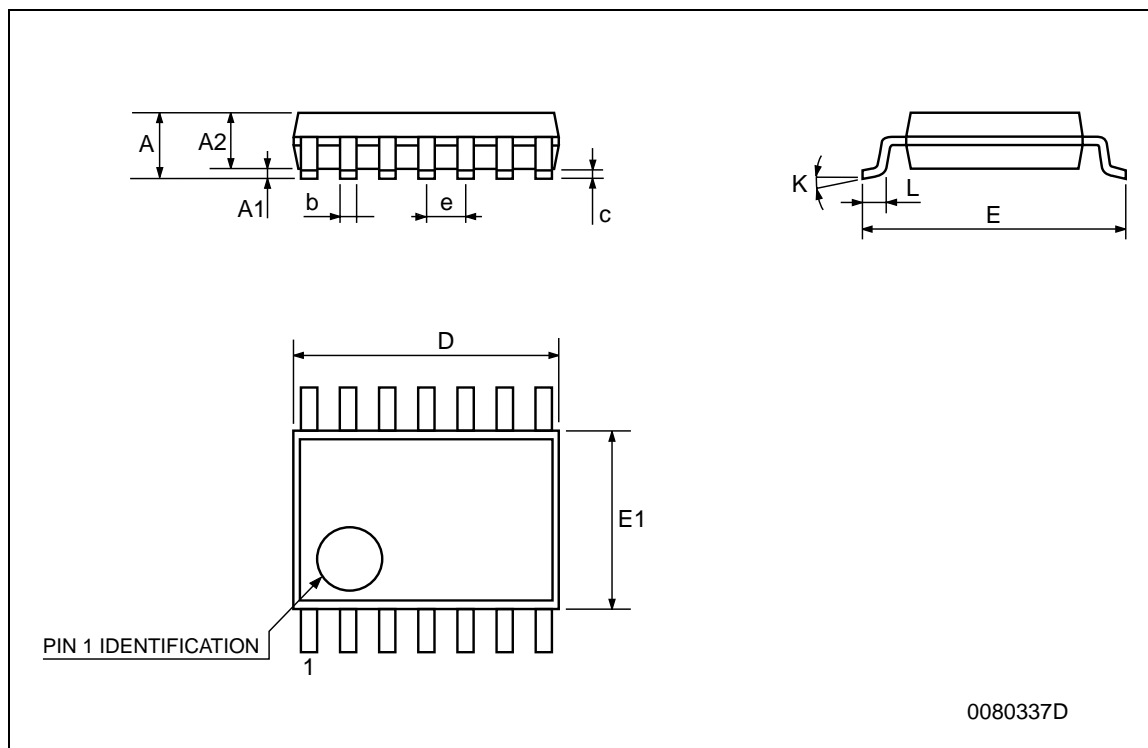
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G

## TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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