

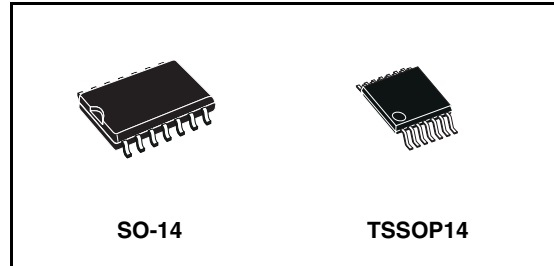


74LCX74

Low voltage CMOS dual D-Type Flip Flop with 5V tolerant inputs

Features

- 5V tolerant inputs
- High speed:
 - $f_{MAX} = 150\text{MHz}$ (Max) at $V_{CC} = 3\text{V}$
- Power down protection on inputs and outputs
- Symmetrical output impedance:
 - $I_{OHL} = I_{OL} = 24\text{mA}$ (Min) at $V_{CC} = 3\text{V}$
- PCI bus levels guaranteed at 24mA
- Balanced propagation delays:
 - $t_{PLH} \cong t_{PHL}$
- Operating voltage range:
 - $V_{CC} \text{ (Opr)} = 2.0\text{V}$ to 3.6V
- Pin and function compatible with 74 series 74
- Latch-up performance exceeds 500mA (JESD 17)
- ESD performance:
 - HBM > 2000V (MIL STD 883 method 3015); MM > 200V



Description

The 74LCX74 is a low voltage CMOS dual D-type flip flop with preset and clear non inverting fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for inputs.

A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse.

$\overline{\text{CLR}}$ and $\overline{\text{PR}}$ are independent of the clock and accomplished by a low setting on the appropriate input.

It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Order codes

| Part number | Package | Packaging |
|-------------|---------|---------------|
| 74LCX74MTR | SO-14 | Tape and reel |
| 74LCX74TTR | TSSOP14 | Tape and reel |

Contents

| | | |
|----------|---|-----------|
| 1 | Logic symbols and I/O equivalent circuit | 3 |
| 1.1 | Logic diagram | 3 |
| 2 | Pin settings | 4 |
| 2.1 | Pin connection | 4 |
| 2.2 | Pin description | 4 |
| 2.3 | Truth table | 4 |
| 3 | Maximum rating | 5 |
| 3.1 | Recommended operating conditions | 5 |
| 4 | Electrical characteristics | 6 |
| 5 | Test circuit | 8 |
| 6 | Waveforms | 8 |
| 7 | Package mechanical data | 11 |
| 8 | Revision history | 16 |

1 Logic symbols and I/O equivalent circuit

Figure 1. IEC logic symbols

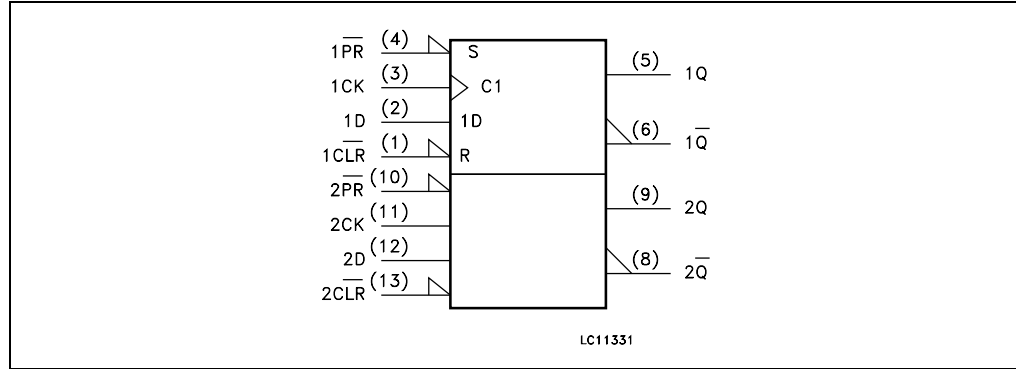
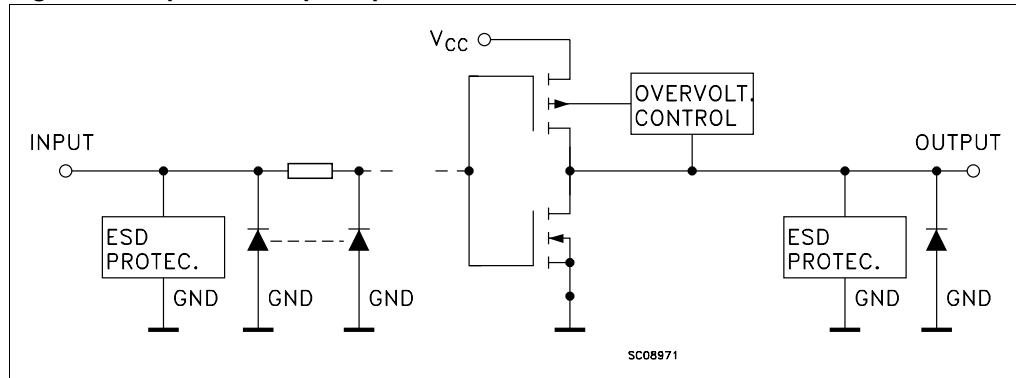
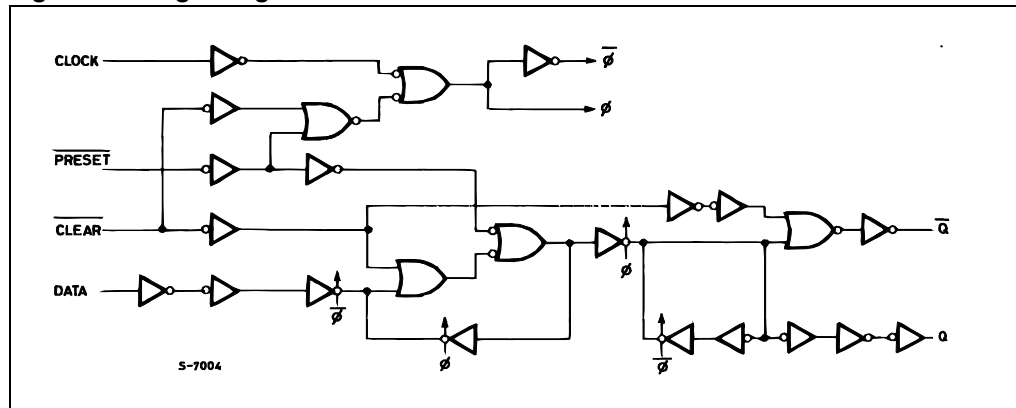


Figure 2. Input and output equivalent circuit



1.1 Logic diagram

Figure 3. Logic diagram

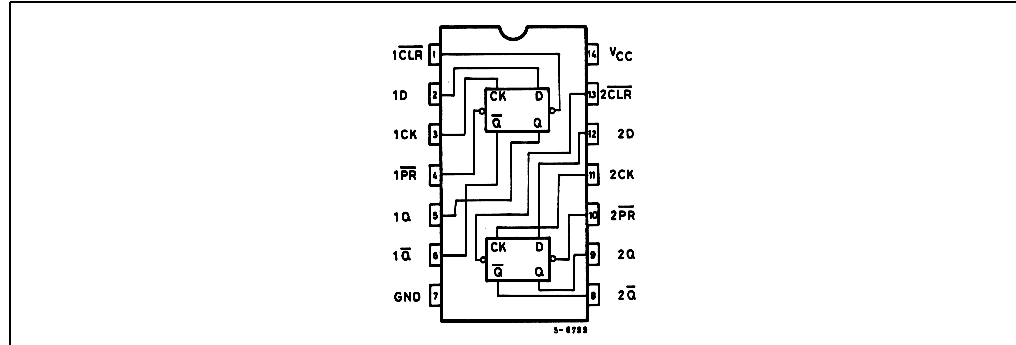


Note: This logic diagram has not to be used to estimate propagation delays

2 Pin settings

2.1 Pin connection

Figure 4. Pin connection (top through view)



2.2 Pin description

Table 1. Pin description

| Pin N° | Symbol | Name and function |
|--------|--|---|
| 1, 13 | $1\overline{\text{CLR}}, 2\overline{\text{CLR}}$ | Asynchronous reset - direct input |
| 2, 12 | 1D, 2D | Data inputs |
| 3, 11 | 1CK, 2CK | Clock input (LOW to HIGH, Edge Triggered) |
| 4, 10 | $1\overline{\text{PR}}, 2\overline{\text{PR}}$ | Asynchronous set - direct input |
| 5, 9 | 1Q, 2Q | True Flip-Flop outputs |
| 6, 8 | $1\overline{\text{Q}}, 2\overline{\text{Q}}$ | Complement Flip-Flop outputs |
| 7 | GND | Ground (0V) |
| 14 | V_{CC} | Positive supply voltage |

2.3 Truth table

Table 2. Truth table

| Inputs | | | | Outputs | | Function |
|--------|----|------------------|----|---------|-----------------------|-----------|
| CLR | PR | D | CK | Q | $\overline{\text{Q}}$ | |
| L | H | X | X | L | H | CLEAR |
| H | L | X | X | H | L | PRESET |
| L | L | X | X | H | H | |
| H | H | L | ┐ | L | H | |
| H | H | H | ┐ | H | L | |
| H | H | X ⁽¹⁾ | ┐ | Q_n | \overline{Q}_n | No change |

1. X do not care

3 Maximum rating

stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. these are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. exposure to absolute maximum rating conditions for extended periods may affect device reliability. refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------|--|------------------------|------|
| V_{CC} | Supply voltage | -0.5 to +7.0 | V |
| V_I | DC input voltage | -0.5 to +7.0 | V |
| V_O | DC output voltage ($V_{CC} = 0V$) | -0.5 to +7.0 | V |
| V_O | DC output voltage (high or low state) ⁽¹⁾ | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | DC input diode current | -50 | mA |
| I_{OK} | DC output diode current ⁽²⁾ | -50 | mA |
| I_O | DC output current | ± 50 | mA |
| I_{CC} | DC supply current per supply pin | ± 100 | mA |
| I_{GND} | DC ground current per supply pin | ± 100 | mA |
| T_{stg} | Storage temperature | -65 to +150 | °C |
| T_L | Lead temperature (10 sec) | 300 | °C |

1. I_O absolute maximum rating must be observed

2. $V_O < GND$

3.1 Recommended operating conditions

Table 4. Recommended operating conditions

| Symbol | Parameter | Value | Unit |
|------------------|---|---------------|------|
| V_{CC} | Supply voltage ⁽¹⁾ | 2.0 to 3.6 | V |
| V_I | Input voltage | 0 to 5.5 | V |
| V_O | Output voltage ($V_{CC} = 0V$) | 0 to 5.5 | V |
| V_O | Output voltage (high or low state) | 0 to V_{CC} | V |
| I_{OH}, I_{OL} | High or low level output current ($V_{CC} = 3.0$ to $3.6V$) | ± 24 | mA |
| I_{OH}, I_{OL} | High or low level output current ($V_{CC} = 2.7V$) | ± 12 | mA |
| T_{op} | Operating temperature | -40 to 85 | °C |
| dt/dv | Input Rise and Fall Time ⁽²⁾ | 0 to 10 | ns/V |

1. Truth table guaranteed: 1.5V to 3.6V

2. V_{IN} from 0.8V to 2V at $V_{CC} = 3.0V$

4 Electrical characteristics

Table 5. DC specifications

| Symbol | Parameter | Test condition | | Value | | Unit |
|------------------|---------------------------|------------------------|--|----------------------|------|------|
| | | V _{CC} (V) | | -40 to 85°C | | |
| | | | | Min | Max | |
| V _{IH} | High level input voltage | 2.7 to 3.6 | | 2.0 | | V |
| V _{IL} | Low level input voltage | | | | | 0.8 |
| V _{OH} | High level output voltage | 2.7 to 3.6 | I _O =-100 μA | V _{CC} -0.2 | | V |
| | | 2.7 | I _O =-12 mA | 2.2 | | |
| | | 3.0 | I _O =-18 mA | 2.4 | | |
| | | | I _O =-24 mA | 2.2 | | |
| V _{OL} | Low level output voltage | 2.7 to 3.6 | I _O =100 μA | | 0.2 | V |
| | | 2.7 | I _O =12 mA | | 0.4 | |
| | | 3.0 | I _O =16 mA | | 0.4 | |
| | | | I _O =24 mA | | 0.55 | |
| I _I | Input leakage current | 2.7 to 3.6 | V _I = 0 to 5.5V | | ±5 | μA |
| I _{off} | Power OFF leakage current | 0 | V _I or V _O = 5.5V | | 10 | μA |
| I _{CC} | Quiescent supply current | 2.7 to 3.6 | V _I = V _{CC} or GND | | 10 | μA |
| | | | V _I or V _O = 3.6 to 5.5V | | ±10 | |
| ΔI _{CC} | I incr. per Input | 2.7 to 3.6 | V _{IH} = V _{CC} - 0.6V | | 500 | μA |

Table 6. Dynamic switching characteristics

| Symbol | Parameter | Test condition | | Value | | | Unit |
|------------------|---|------------------------|---|------------------------|------|-----|------|
| | | V _{CC} (V) | | T _A = 25 °C | | | |
| | | | | Min | Typ | Max | |
| V _{OLP} | Dynamic low level quiet output ⁽¹⁾ | 3.3 | C _L = 50pF V _{IL} = 0V, V _{IH} = 3.3V | | 0.8 | | V |
| V _{OLV} | | | | | -0.8 | | |

1. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

Table 7. AC electrical characteristics

| Symbol | Parameter | Test condition | | | | Value | | Unit |
|--|--|------------------------|------------------------|-----------------------|---|--------------|-----|------|
| | | V _{CC} (V) | C _L (pF) | R _L (Ω) | t _s = t _r (ns) | -40 to 85 °C | | |
| | | | | | | Min | Max | |
| t _{PLH} t _{PHL} | Propagation delay time (CK to Q or \bar{Q}) | 2.7 | 50 | 500 | 2.5 | 1.5 | 8.0 | ns |
| | | 3.0 to 3.6 | | | | 1.5 | 7.0 | |
| t _{PLH} t _{PHL} | Propagation delay time (\overline{PR} or \overline{CLR} to Q or \bar{Q}) | 2.7 | 50 | 500 | 2.5 | 1.5 | 8.0 | ns |
| | | 3.0 to 3.6 | | | | 1.5 | 7.0 | |
| t _S | Setup time, HIGH or LOW level D to CK | 2.7 | 50 | 500 | 2.5 | 2.5 | | ns |
| | | 3.0 to 3.6 | | | | 2.5 | | |
| t _H | Hold time, HIGH or LOW level D to CK | 2.7 | 50 | 500 | 2.5 | 1.5 | | ns |
| | | 3.0 to 3.6 | | | | 1.5 | | |
| t _W | CK Pulse width, HIGH or LOW PR or CLR Pulse Width, LOW | 2.7 | 50 | 500 | 2.5 | 3.0 | | ns |
| | | 3.0 to 3.6 | | | | 3.0 | | |
| t _{rec} | Recovery time \overline{PR} or \overline{CLR} to CK | 2.7 | 50 | 500 | 2.5 | 0 | | ns |
| | | 3.0 to 3.6 | | | | 0 | | |
| f _{MAX} | Clock pulse frequency | 2.7 | 50 | 500 | 2.5 | 150 | | MHz |
| t _{OSLH} t _{OSSL} | Output to output skew time ⁽¹⁾ ⁽²⁾ | 3.0 to 3.6 | 50 | 500 | 2.5 | | 1.0 | ns |

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSSL} = |t_{PHLm} - t_{PHLn}|)
2. Parameter guaranteed by design

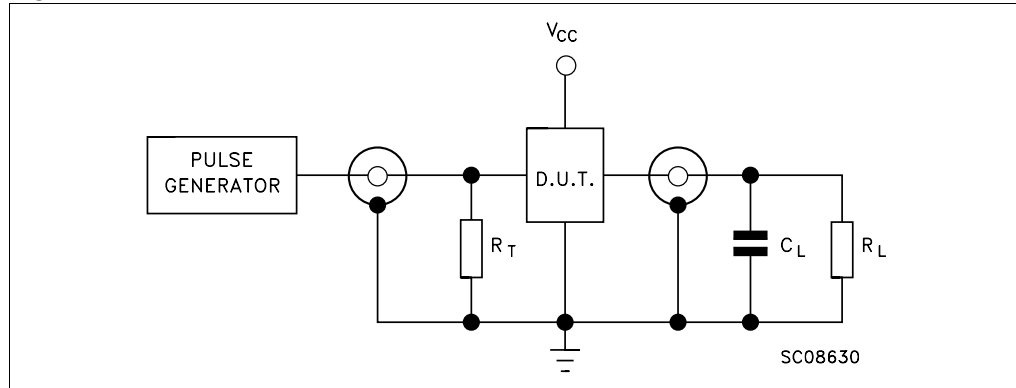
Table 8. Capacitive characteristics

| Symbol | Parameter | Test condition | | Value | | | Unit |
|-----------------|--|------------------------|---|------------------------|-----|-----|------|
| | | V _{CC} (V) | | T _A = 25 °C | | | |
| | | | | Min | Typ | Max | |
| C _{IN} | Input capacitance | 3.3 | V _{IN} = 0 to V _{CC} | | 6 | | pF |
| C _{PD} | Power dissipation capacitance ⁽¹⁾ | 3.3 | f _{IN} = 10MHz V _{IN} = 0 or V _{CC} | | 40 | | pF |

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}/2 (per gate)

5 Test circuit

Figure 5. Test circuit



$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)

$R_L = 500\Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

6 Waveforms

Figure 6. Propagation delays, setup and hold times ($f = 1\text{MHz}$; 50% duty cycle)

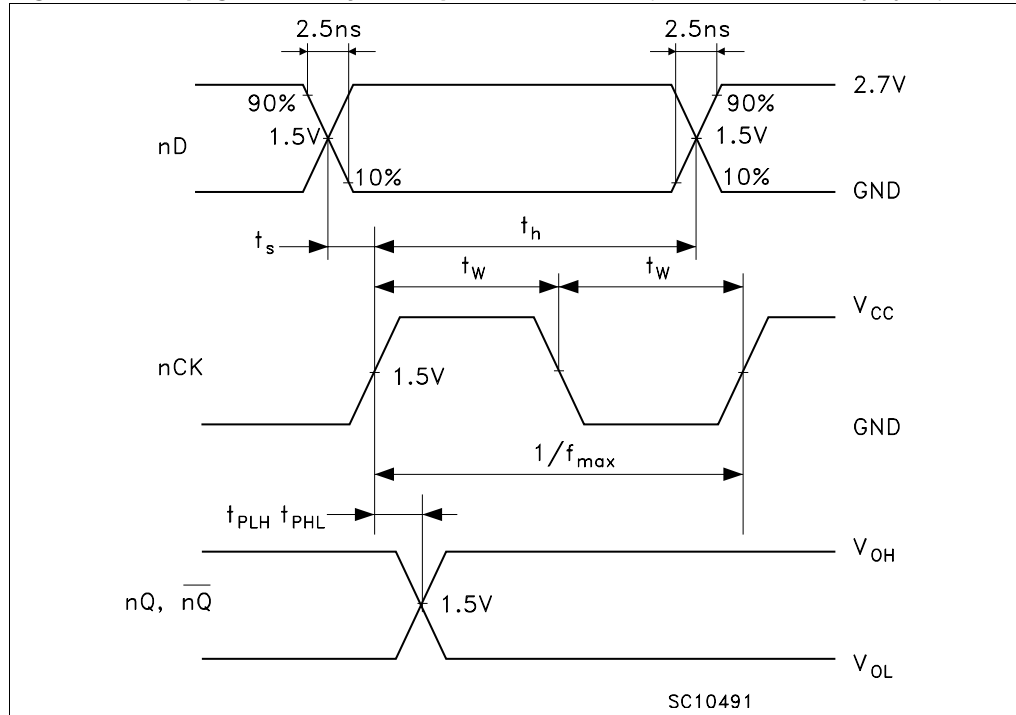


Figure 7. Propagation delays (f=1MHz; 50% duty cycle)

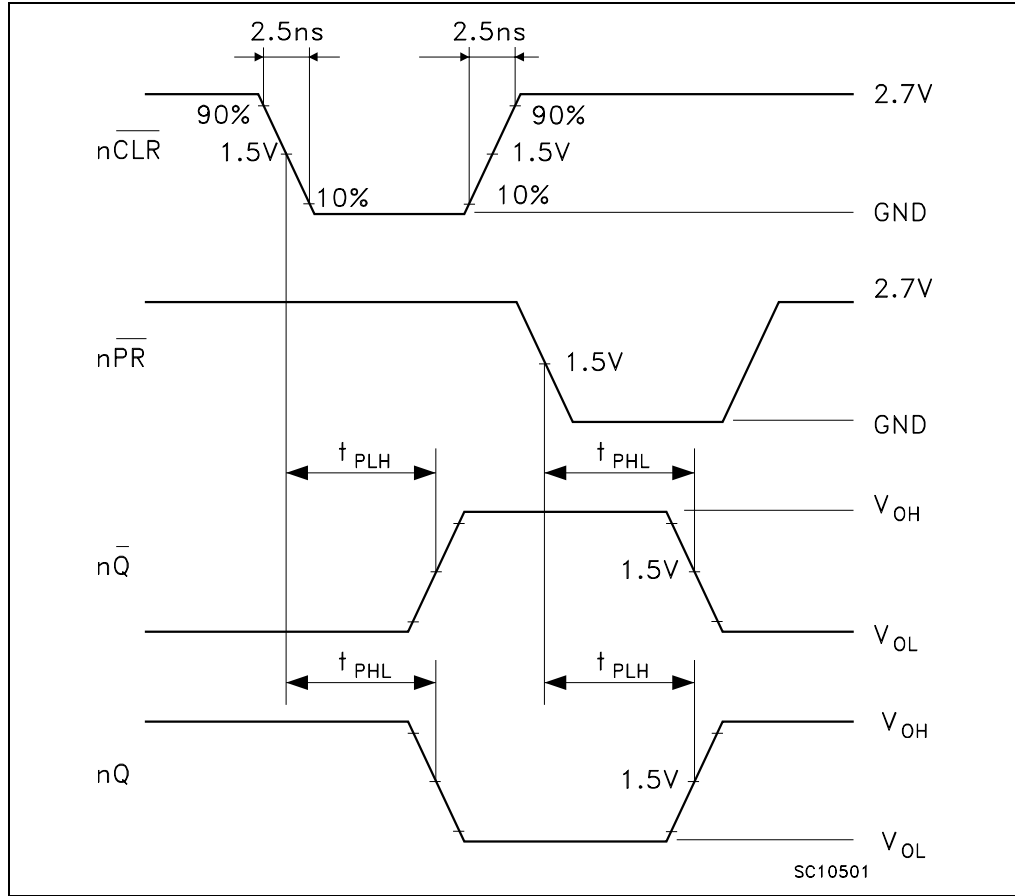


Figure 8. Recovery times (f=1MHz; 50% duty cycle)

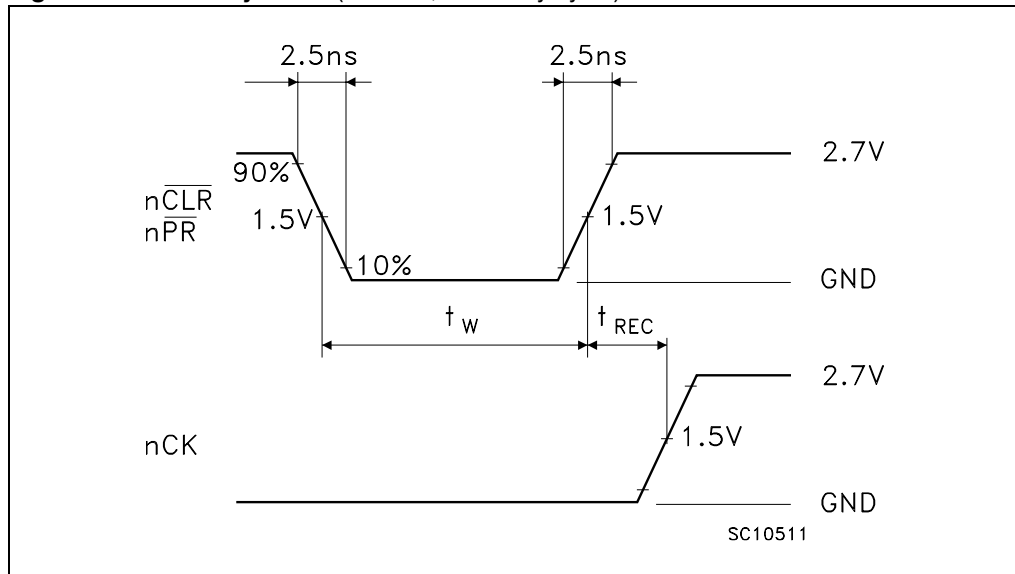
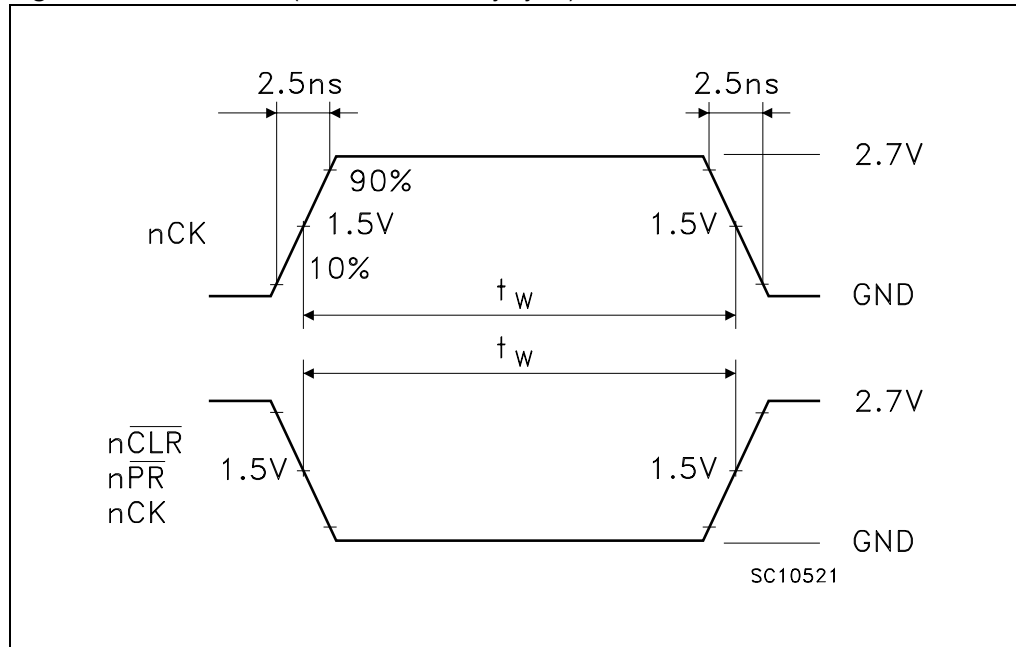


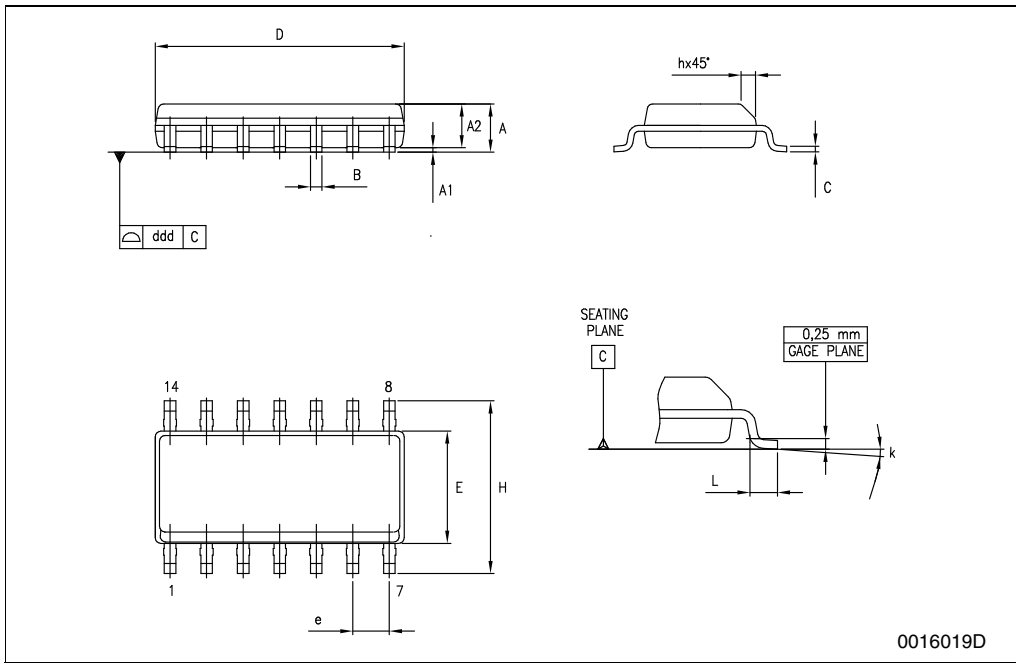
Figure 9. Pulse width (f=1MHz; 50% duty cycle)

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

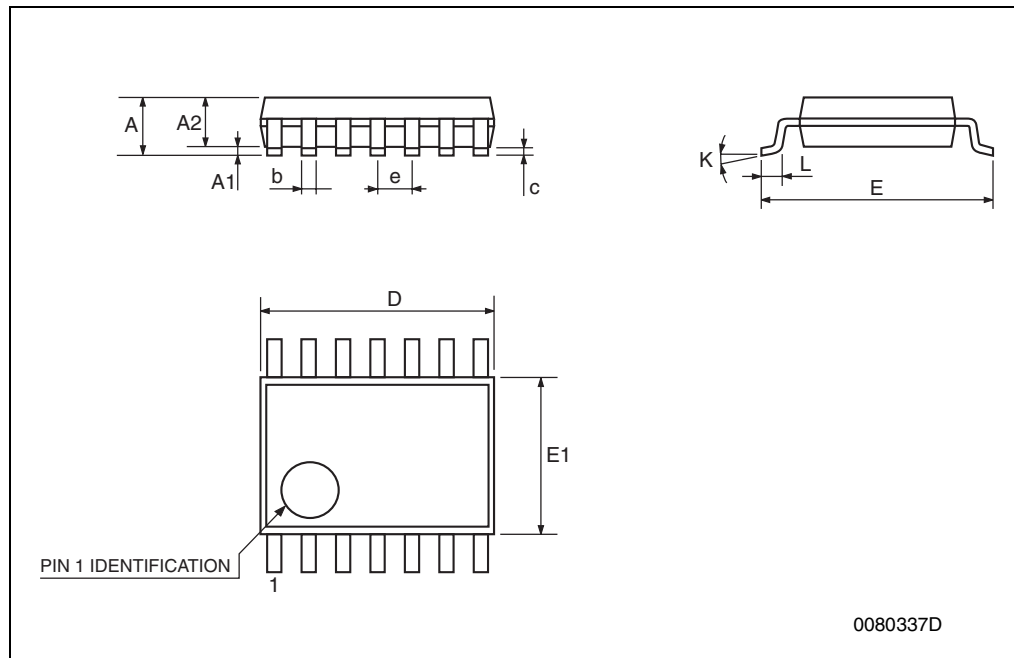
SO-14 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| A1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D | 8.55 | | 8.75 | 0.337 | | 0.344 |
| E | 3.8 | | 4.0 | 0.150 | | 0.157 |
| e | | 1.27 | | | 0.050 | |
| H | 5.8 | | 6.2 | 0.228 | | 0.244 |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| k | 0° | | 8° | 0° | | 8° |
| ddd | | | 0.100 | | | 0.004 |



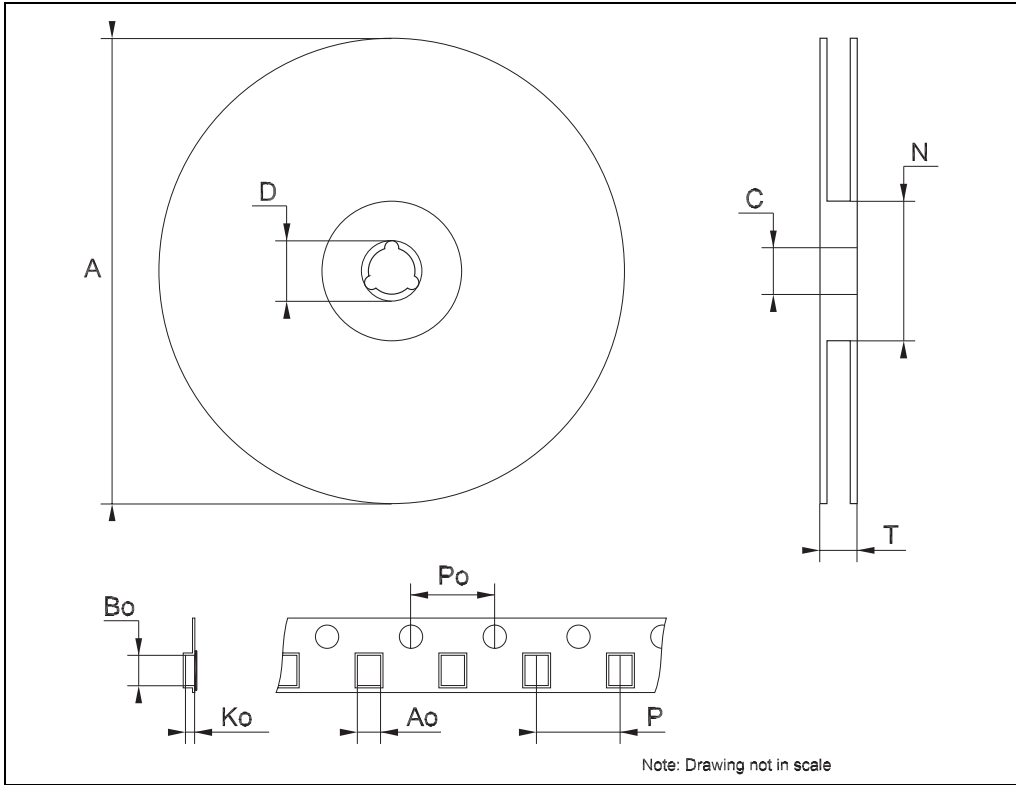
TSSOP14 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|----------|------|-------|------------|--------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 4.9 | 5 | 5.1 | 0.193 | 0.197 | 0.201 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



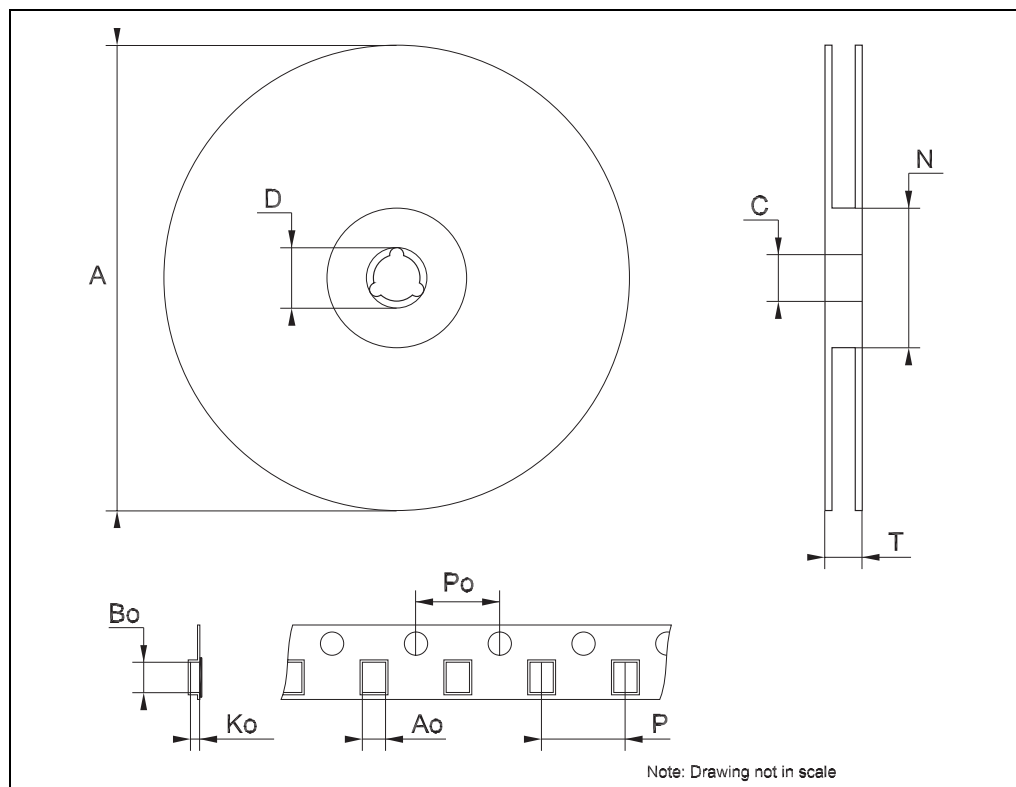
Tape & Reel SO-14 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|------|------|-------|------|--------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.4 | | 6.6 | 0.252 | | 0.260 |
| Bo | 9 | | 9.2 | 0.354 | | 0.362 |
| Ko | 2.1 | | 2.3 | 0.082 | | 0.090 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |



Tape & Reel TSSOP14 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|------|------|-------|------|--------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.7 | | 6.9 | 0.264 | | 0.272 |
| Bo | 5.3 | | 5.5 | 0.209 | | 0.217 |
| Ko | 1.6 | | 1.8 | 0.063 | | 0.071 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |



8 Revision history

Table 9. Revision history

| Date | Revision | Changes |
|-------------|-----------------|--|
| 15-Sep-2004 | 7 | Ordering codes revision - pag. 1. |
| 10-Jul-2006 | 8 | New template, temperature ranges updated |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZE REPRESENTATIVE OF ST, ST PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS, WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2006 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

