FAIRCHILD SEMICONDUCTOR™

February 1989
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74ACT2708
64 x 9 First-In, First-Out Memory

General Description

The ACT2708 is an expandable first-in, first-out memory organized as 64 words by 9 bits. An 85 MHz shift-in and 60 MHz shift-out typical data rate makes it ideal for high-speed applications. It uses a dual port RAM architecture with pointer logic to achieve the high speed with negligible fall-through time.

Separate Shift-In (SI) and Shift-Out (SO) clocks control the use of synchronous or asynchronous write or read. Other controls include a Master Reset ($\overline{MR}$) and Output Enable ($\overline{OE}$) for initializing the internal registers and allowing the data outputs to be 3-STATE. Input Ready (IR) and Output Ready (OR) signal when the FIFO is ready for I/O operations. The status flags HF and FULL indicate when the FIFO is full, empty or half full.

The FIFO can be expanded to provide different word lengths by tying off unused data inputs.

Features

- 64-words by 9-bit dual port RAM organization
- 85 MHz shift-in, 60 MHz shift-out data rate, typical
- Expandable in word width only
- TTL-compatible inputs
- Asynchronous or synchronous operation
- Asynchronous master reset
- Outputs source/sink 8 mA
- 3-STATE outputs
- Full ESD protection
- Input and output pins directly in line for easy board layout
- TRW 1030 work-alike operation

Applications

- High-speed disk or tape controllers
- A/D output buffers
- High-speed graphics pixel buffer
- Video time base correction
- Digital filtering

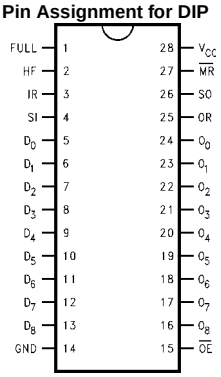
Ordering Code:

Order Number	Package Number	Package Description
74ACT2708PC	N28B	28-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignment for DIP



Pin Descriptions

Pin Names	Description
D_0–D_8	Data Inputs
$\overline{MR}$	Master Reset
$\overline{OE}$	Output Enable Input
SI	Shift-In
SO	Shift-Out
IR	Input Ready
OR	Output Ready
HF	Half Full Flag
FULL	Full Flag
O_0–O_8	Data Outputs

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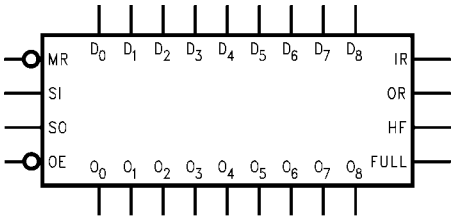
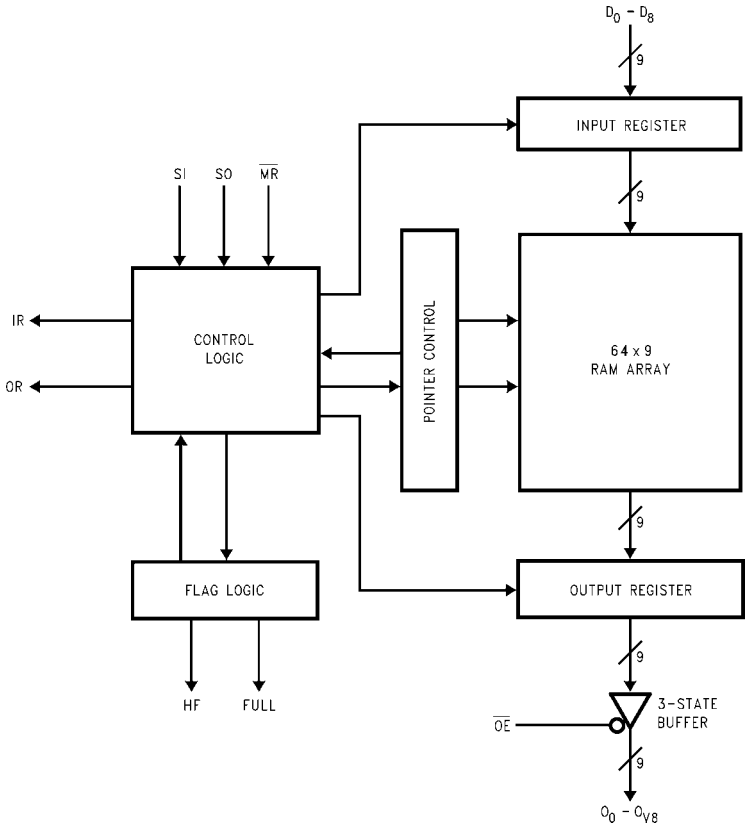
Logic Symbol



Block Diagram



Functional Description

INPUTS

Data Inputs (D_0–D_8)

Data inputs for 9-bit wide data are TTL-compatible. Word width can be reduced by trying unused inputs to ground and leaving the corresponding outputs open.

Reset ($\overline{MR}$)

Reset is accomplished by pulsing the $\overline{MR}$ input LOW. During normal operation $\overline{MR}$ is HIGH. A reset is required after power up to guarantee correct operation. On reset, the data outputs go LOW, IR goes HIGH, OR goes LOW, FH and FULL go LOW. During reset, both internal read and write pointers are set to the first location in the array.

Shift-In (SI)

Data is written into the FIFO by pulsing SI HIGH. When Shift-In goes HIGH, the data is loaded into an internal data latch. Data setup and hold times need to be adhered to with respect to the falling edge of SI. The write cycle is complete after the falling edge of SI. The shift-in is independent of any ongoing shift-out operation. After the first word has been written into the FIFO, the falling edge of SI makes HF go HIGH, indicating a non-empty FIFO. The first data word appears at the output after the falling edge of SI. After half the memory is filled, the next rising edge of SI makes FULL go HIGH indicating a half-full FIFO. When the FIFO is full, any further shift-ins are disabled.

When the FIFO is empty and $\overline{OE}$ is LOW, the falling edge of the first SI will cause the first data word just shifted-in to appear at the output, even though SO may be LOW.

Shift-Out (SO)

Data is read from the FIFO by the Shift-Out signal provided the FIFO is not empty. SO going HIGH causes OR to go LOW indicating that output stage is busy. On the falling edge of SO, new data reaches the output after propagation delay t_D. If the last data has been shifted-out of the memory, OR continues to remain LOW, and the last word shifted-out remains on the output pins.

Output Enable ($\overline{OE}$)

$\overline{OE}$ LOW enables the 3-STATE output buffers. When $\overline{OE}$ is HIGH, the outputs are in a 3-STATE mode.

OUTPUTS

Data Outputs (O_0–O_8)

Data outputs are enabled when $\overline{OE}$ is LOW and in the 3-STATE condition when $\overline{OE}$ is HIGH.

Input Ready (IR)

IR HIGH indicates data can be shifted-in. When SI goes HIGH, IR goes LOW, indicating input stage is busy. IR stays LOW when the FIFO is full and goes HIGH after the falling edge of the first shift-out.

Output Ready (OR)

OR HIGH indicates data can be shifted-out from the FIFO. When SO goes HIGH, OR goes LOW, indicating output stage is busy. OR is LOW when the FIFO is reset or empty and goes HIGH after the falling edge of the first shift-in.

Half-Full (HF)

This status flag along with the FULL status flag indicates the degree of fullness of the FIFO. On reset, HF is LOW; it rises on the falling edge of the first SI. The rising edge of the SI pulse that fills up the FIFO makes HF go LOW. Going from the empty to the full state with SO LOW, the falling edge of the first SI causes HF to go HIGH, the rising edge of the 33rd SI causes FULL to go HIGH, and the rising edge of the 64th SI causes HF to go LOW.

When the FIFO is full, HF is LOW and the falling edge of the first shift-out causes HF to go HIGH indicating a "non-full" FIFO.

Full Flag (FULL)

This status flag along with the HF status flag indicates the degree of fullness of the FIFO. On reset, FULL is LOW. When half the memory is filled, on the rising edge of the next SI, the FULL flag goes HIGH. It remains set until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. The FULL flag then goes LOW on the rising edge of the next SO.

Status Flags Truth Table

HF	FULL	Status Flag Condition
L	L	Empty
L	H	Full
H	L	<32 Locations Filled
H	H	≥32 Locations Filled

H = HIGH Voltage Level
L = LOW Voltage Level

Reset Truth Table

Inputs			Outputs				
$\overline{MR}$	SI	SO	IR	OR	HF	FULL	O_0–O_8
H	X	X	X	X	X	X	X
L	X	X	H	L	L	L	L

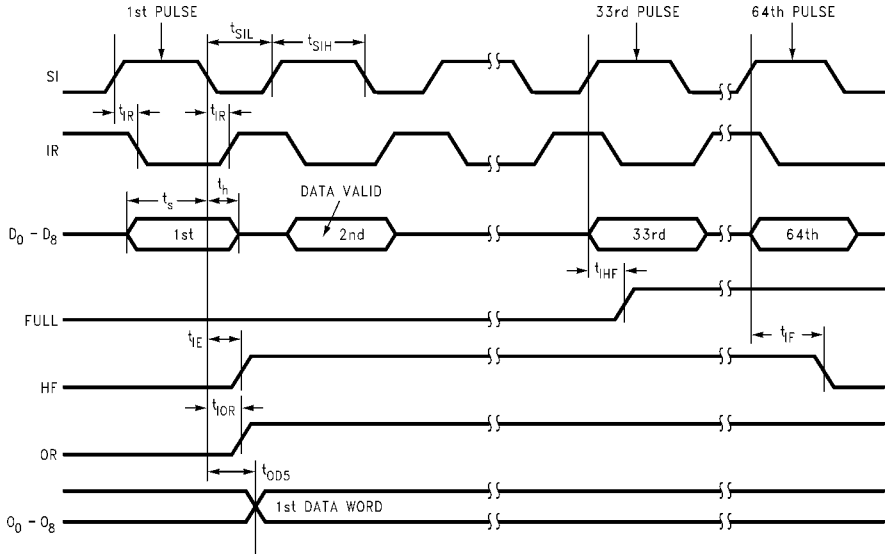
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

MODES OF OPERATION

Mode 1: Shift in Sequence for FIFO Empty to Full

Sequence of Operation

1. Input Ready is initially HIGH; HF and FULL flags are LOW. The FIFO is empty and prepared for valid data. OR is LOW indicating that the FIFO is not yet ready to output data.
2. Shift-In is set HIGH, and data is loaded into the FIFO. Data has to be settled t_s before the falling edge of SI and held t_h after.
3. Input Ready (IR) goes LOW propagation delay t_{IR} after SI goes HIGH: input stage is busy.
4. Shift-In is set LOW; IR goes HIGH indicating the FIFO is ready for additional data. Data just shifted-in arrives at output propagation delay t_{OD5} after SI falls. OR goes HIGH propagation delay t_{IOR} after SI goes LOW, indicating the FIFO has valid data on its outputs. HF goes HIGH propagation delay t_{IE}after SI falls, indicating the FIFO is no longer empty.
5. The process is repeated through the 64th data word. On the rising edge of the 33rd SI, FULL flag goes HIGH propagation delay t_{IHF} after SI, indicating a half-full FIFO. HF goes LOW propagation delay t_{IF} after the rising edge of the 64th pulse indicating that the FIFO is full. Any further shift-ins are disabled.



Note: SO and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH.

FIGURE 1. Modes of Operation Mode 1

Mode 2: Master Reset

Sequence of Operation

1. Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset ($\overline{MR}$) HIGH.
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t_{MRW} before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time t_{MRIRH} after the falling edge of $\overline{MR}$. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times t_{MRE} and t_{MRO} respectively after the falling edge of $\overline{MR}$. OR falls recovery time t_{MRORL} after $\overline{MR}$ falls. Data at outputs goes LOW recovery time t_{MRONL} after $\overline{MR}$ goes LOW.
5. Shift-In can be taken HIGH after a minimum recovery time t_{MRSIH} after $\overline{MR}$ goes HIGH.

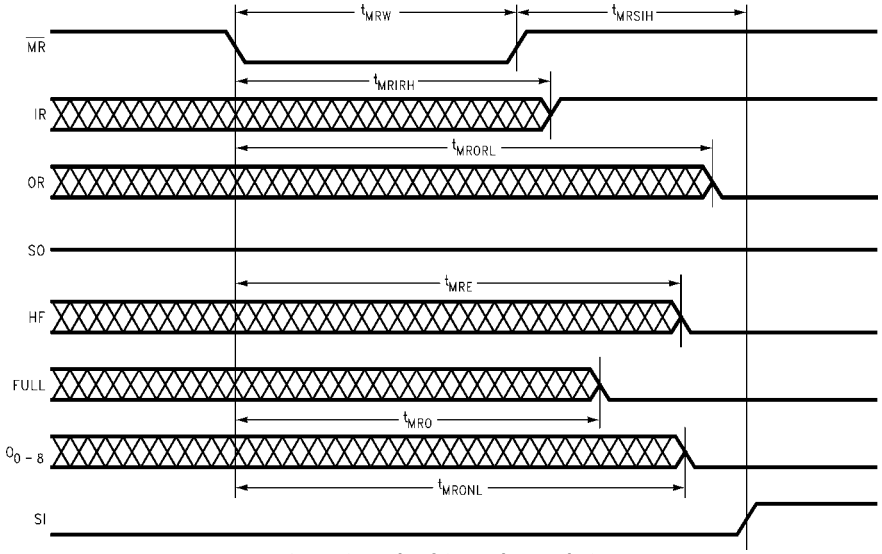
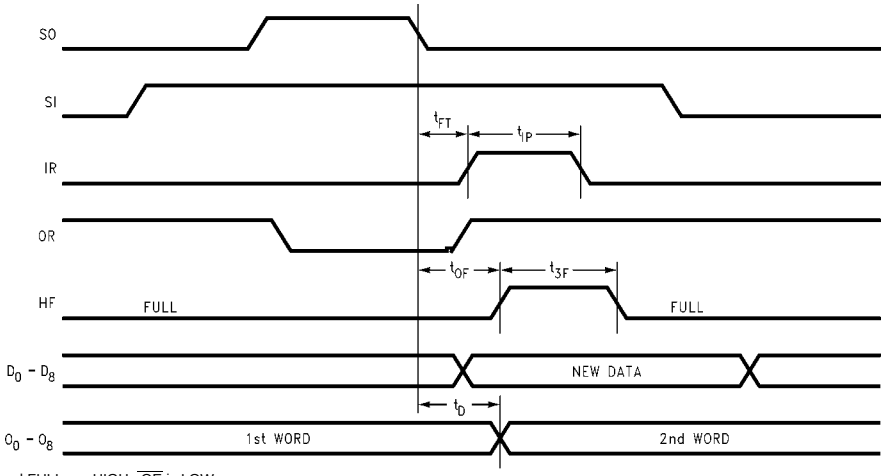


FIGURE 2. Mode of Operation Mode 2

Mode 3: With FIFO Full, Shift-In is Held HIGH in Anticipation of an Empty Location

Sequence of Operation

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay t_D. New data is written into the FIFO after SO goes LOW.
3. Input Ready goes HIGH one fall-through time, t_{FT}, after the falling edge of SO. Also, HF goes HIGH one t_{OF} after SO falls, indicating that the FIFO is no longer full.
4. IR returns LOW pulse width t_{IP} after rising and shifting new data in. Also, HF returns LOW pulse width t_{3F} after rising, indicating the FIFO is once more full.
5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation.



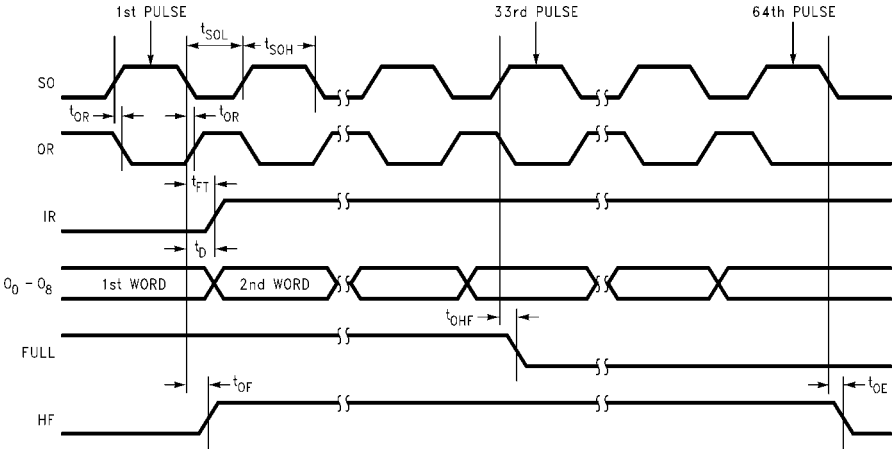
Note: $\overline{MR}$ and FULL are HIGH; $\overline{OE}$ is LOW.

FIGURE 3. Modes of Operation Mode 3

Mode 4: Shift-Out Sequence, FIFO Full to Empty

Sequence of Operation

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW one propagation delay, t_{OR}, after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output one propagation delay, t_D, after SO falls; OR goes HIGH one propagation delay, t_{OR}, after SO falls and HF rises one propagation delay, t_{OF}, after SO falls. IR rises one fall-through time, t_{FT}, after SO falls.
4. Repeat process through the 64th SO pulse. FULL flag goes LOW one propagation delay, t_{OHF}, after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW one propagation delay, t_{OE}, after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.



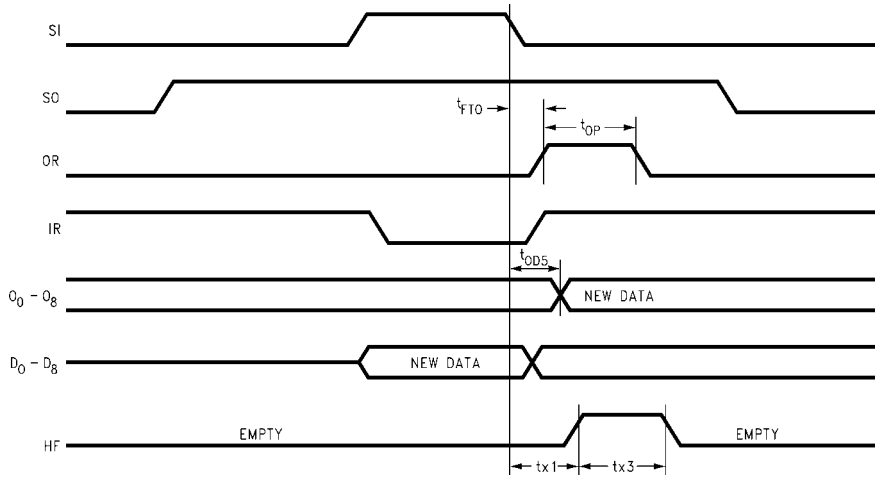
Note: SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; D_0–D_8 are immaterial.

FIGURE 4. Modes of Operation Mode 4

Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data

Sequence of Operation

1. FIFO is initially empty; Shift-Out goes HIGH.
2. Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay t_{X1} after the falling edge of SI.
3. OR rises a fall-through time of t_{FTO} after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output one propagation delay, t_{OD5}, after the falling edge of Shift-In.
5. OR goes LOW pulse width t_{OP} after rising and HF goes LOW pulse width t_{X3} after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.



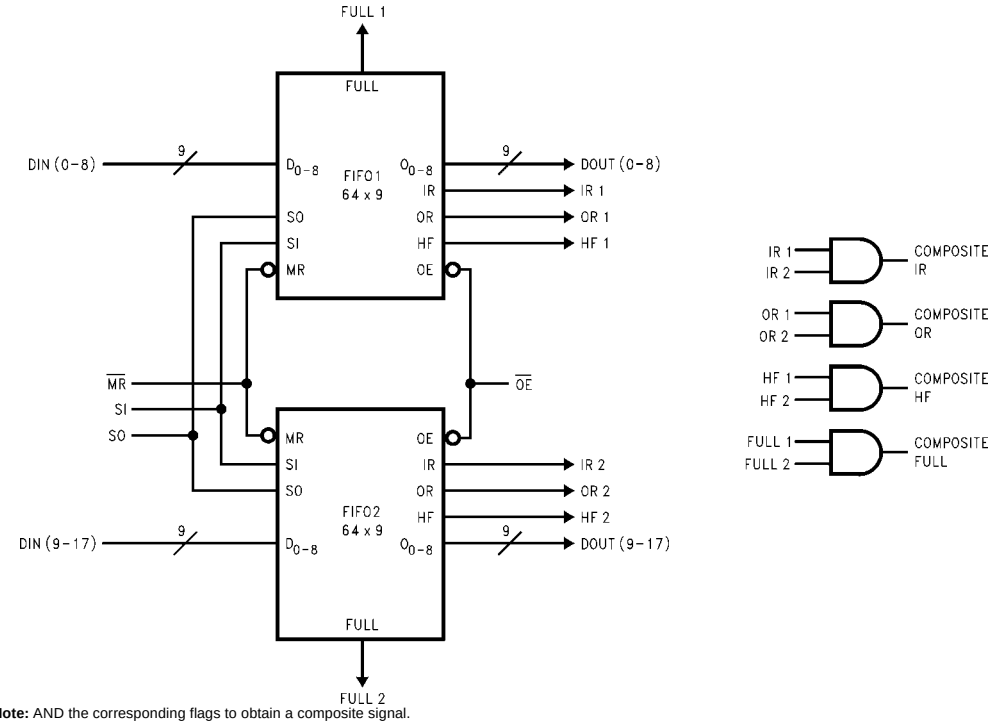
Note: FULL is LOW; $\overline{MR}$is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$. Data output transition—valid data arrives at output stage t_{DOF} after OR is HIGH.

FIGURE 5. Modes of Operation Mode 5

FIFO Expansion

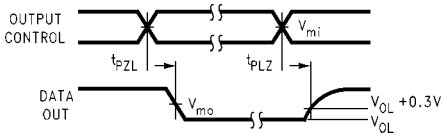
Word Width Expansion

Word width can be increased by connecting the corresponding input control signals of multiple devices. Flags can be monitored to obtain a composite signal by ANDing the corresponding flags.



Note: AND the corresponding flags to obtain a composite signal.

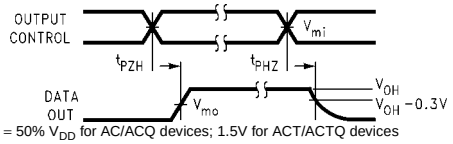
FIGURE 6. Word Width Expansion—64 x 18 FIFO



V_{mi} = 50% V_{DD} for AC/ACQ devices; 1.5V for ACT/ACTQ devices

V_{mo} = 50% V_{DD} for AC/ACT, ACQ/ACTQ devices

FIGURE 7. 3-STATE Output Low Enable and Disable Times for AC/ACT, ACQ/ACTQ



V_{mi} = 50% V_{DD} for AC/ACQ devices; 1.5V for ACT/ACTQ devices

V_{mo} = 50% V_{DD} for AC/ACT, ACQ/ACTQ devices

FIGURE 8. 3-STATE Output High Enable and Disable Times for AC/ACT, ACQ/ACTQ

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±32 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±32 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C Typ	T_A = −40° to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum High Level	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 µA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.76	V	I_{OH} = −8 mA
		5.5		4.86	4.76		I_{OH} = −8 mA (Note 2)
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 µA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.44	V	I_{OL} = 8 mA
		5.5		0.36	0.44		I_{OL} = 8 mA (Note 2)
I_{IN}	Maximum Input	5.5		±0.1	±1.0	µA	V_I = V_{CC}, GND
I_{OZ}	Maximum 3-STATE Current	5.5		±0.5	±5.0	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6	1.0	1.5	mA	V_I = V_{CC} −2.1V
I_{OLD}	Maximum Dynamic Output Current (Note 3)	5.5			32	mA	V_{OLD} = 1.65V
I_{OHD}		5.5			−32	mA	V_{OHD} = 3.85V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	µA	V_{IN} = V_{CC} or GND
I_{CCD}	Supply Current 20 MHz Loaded	5.5	125	150	150	mA	f = 20 MHz (Note 4)

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: Test load 50 pF, 500Ω to ground

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay, t_{IR} SI to IR	5.0	2.0	6.5	11.0	1.5	12.5	ns
t_{PHL}	Propagation Delay, t_{IR} SI to IR	5.0	2.0	6.5	11.0	1.5	12.0	ns
t_{PLH}	Propagation Delay, t_{IHF} SI to > HF	5.0	4.0	10.5	17.0	4.0	19.5	ns
t_{PHL}	Propagation Delay, t_{IF} SI to Full Condition	5.0	4.5	10.5	16.5	4.5	19.5	ns
t_{PLH}	Propagation Delay, t_{IE} SI to Not Empty	5.0	4.0	10.0	15.5	4.0	17.5	ns
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	5.0	4.0	13.5	16.5	4.0	19.0	ns
t_{PLH}	Propagation Delay t_{MRIRH} $\overline{MR}$ to IR	5.0	3.0	8.5	13.5	3.0	15.5	ns
t_{PHL}	Propagation Delay, t_{MRORL} $\overline{MR}$ to OR	5.0	7.0	16.5	25.5	7.0	29.0	ns
t_{PHL}	Propagation Delay, t_{MRO} $\overline{MR}$ to Full Flag	5.0	3.5	9.0	14.0	3.5	16.0	ns
t_{PHL}	Propagation Delay, t_{MRE} $\overline{MR}$ to HF Flag	5.0	8.0	17.5	27.5	8.0	30.5	ns
t_{PHL}	Propagation Delay, t_{MRONL} $\overline{MR}$ to O_n, LOW	5.0	3.0	9.0	15.0	3.0	17.0	ns
t_{PLH}	Propagation Delay, t_D SO to Data Out	5.0	6.5	18.5	27.0	6.5	31.0	ns
t_{PHL}	Propagation Delay, t_D SO to Data Out	5.0	6.5	18.5	29.5	6.5	34.5	ns
t_{PHL}	Propagation Delay, t_{OHF} SO to < HF	5.0	3.5	8.5	13.5	3.5	15.5	ns
t_{PLH}	Propagation Delay, t_{OF} SO to Not Full	5.0	5.0	12.5	19.5	5.0	22.0	ns
t_{PLH}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	5.0	2.5	7.0	11.5	2.5	13.5	ns
t_{PHL}	Propagation Delay, t_{OE} SO to Empty	5.0	3.5	9.5	15.5	3.0	17.5	ns
t_{PLH}	Propagation Delay, t_{OD5} SI to New Data Out	5.0	7.0	19.0	30.5	6.0	35.5	ns
t_{PHL}	Propagation Delay, t_{OD5} SI to New Data Out	5.0	7.0	19.0	29.5	6.0	34.5	ns
t_{PLH}	Propagation Delay, t_{X1} SI to HF	5.0	3.5	10.0	16.0	2.5	18.0	ns
t_{PLH}	Fall-Through Time, t_{FTO} SI to OR	5.0	3.5	13.5	21.0	1.5	24.0	ns
t_W	R Pulse Width, t_{OP}	5.0	12.5	17.0	26.0	12.5	30.5	ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_W	HF Pulse Width, t_{X3}	5.0	14.5	20.5	30.5	14.5	36.5	ns
t_W	IR Pulse Width, t_{IP}	5.0	16.5	28.0	43.0	16.5	51.5	ns
t_W	HF Pulse Width, t_{3F}	5.0	17.5	30.0	46.5	17.5	56.0	ns
t_{PLH}	Fall-Through Times, t_{FT} SO to IR	5.0	6.0	15.0	23.5	2.5	28.0	ns
t_{PZL}	Output Enable $\overline{OE}$ to O_n	5.0	2.0	6.5	11.0	1.5	12.0	ns
t_{PLZ}	Output Disable $\overline{OE}$ to O_n	5.0	1.5	5.0	8.5	1.5	9.5	ns
t_{PZH}	Output Enable $\overline{OE}$ to O_n	5.0	2.0	7.0	12.0	1.5	13.0	ns
t_{PHZ}	Output Disable $\overline{OE}$ to O_n	5.0	1.5	7.0	12.0	1.5	13.0	ns
f_{SI}	Maximum SI Clock Frequency	5.0	55	85		45		MHz
f_{SO}	Maximum SO Clock Frequency	5.0	42	60		35		MHz

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

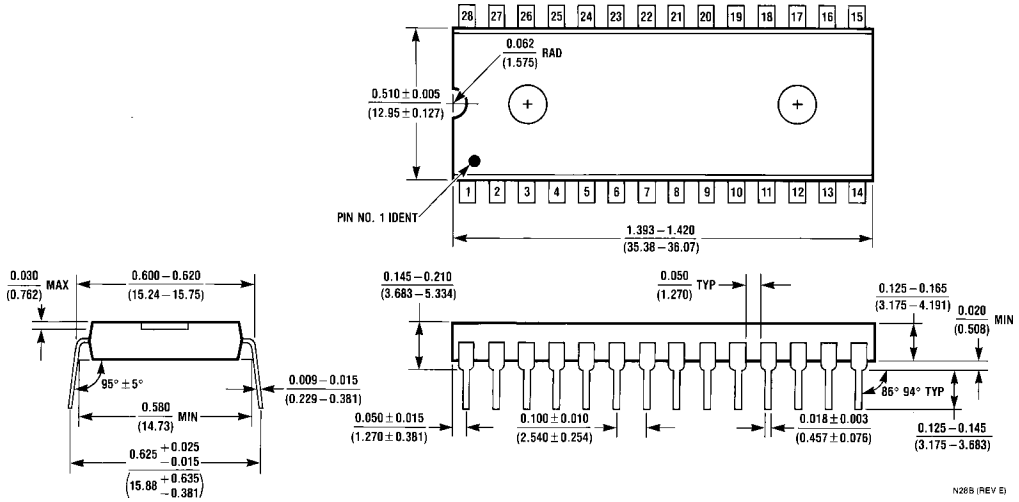
Symbol	Parameter	V_{CC} (V) (Note 6)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
$t_W(H)$	SI Pulse Width, t_{SIH}	5.0	3.5	6.5	7.5	ns
$t_W(L)$	SI Pulse Width, t_{SIL}	5.0	6.0	10.0	12.0	ns
t_S	Setup Time, HIGH or LOW, D_n to SI	5.0	1.0	3.5	4.5	ns
t_H	Hold Time, HIGH or LOW, D_n to SI	5.0	1.5	3.5	4.5	ns
t_W	$\overline{MR}$ Pulse Width, t_{MRW}	5.0	13.0	20.0	24.5	ns
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	5.0	4.5	7.5	8.5	ns
$t_W(H)$	SO Pulse Width, t_{SOH}	5.0	7.5	6.5	8.0	ns
$t_W(L)$	SO Pulse Width, t_{SOL}	5.0	9.0	14.0	17.0	ns

Note 6: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	20.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide
Package Number N28B

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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