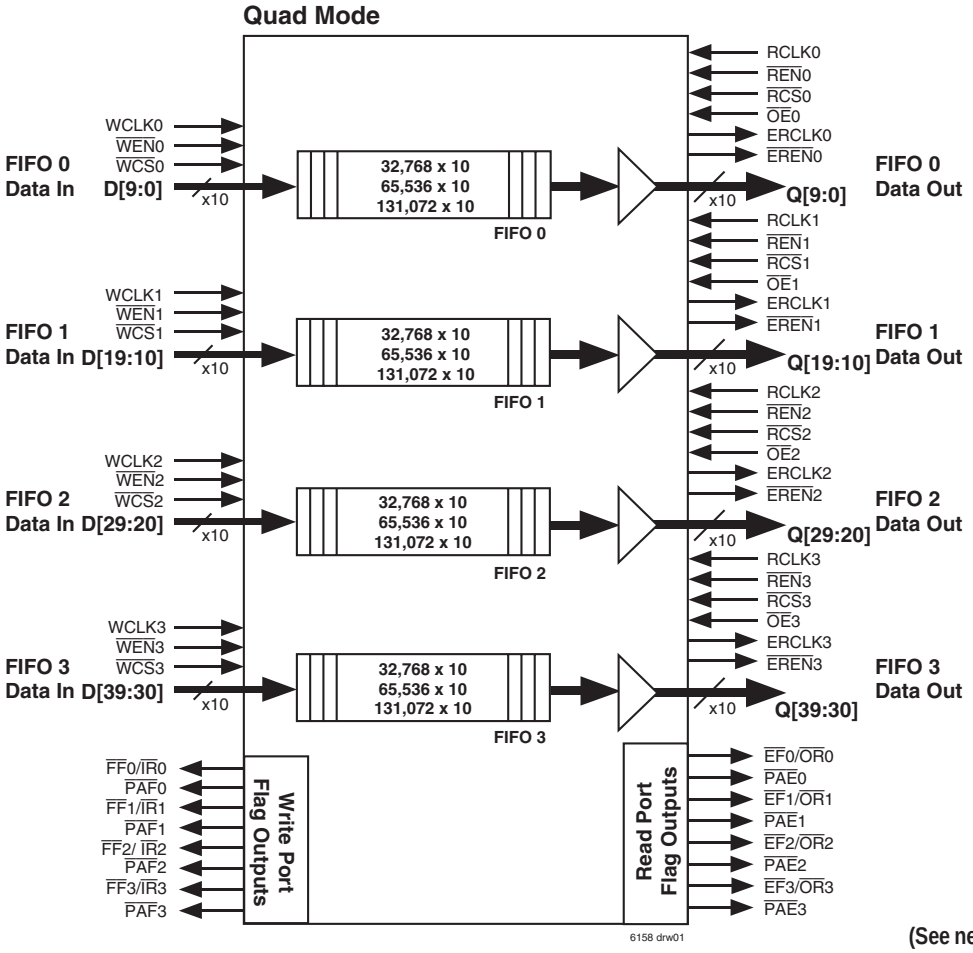
2.5V QUAD/DUAL TeraSync™ DDR/SDR FIFO
x10 QUAD FIFO or x10/x20 DUAL FIFO CONFIGURATIONS

32,768 x 10 x 4/16,384 x 20 x 2	*IDT72T54242*
65,536 x 10 x 4/32,768 x 20 x 2	*IDT72T54252*
131,072 x 10 x 4/65,536 x 20 x 2	*IDT72T54262*

FEATURES

- Choose from among the following memory organizations:
  IDT72T54242 - 32,768 x 10 x 4/32,768 x 10 x 2
  IDT72T54252 - 65,536 x 10 x 4/65,536 x 10 x 2
  IDT72T54262 - 131,072 x 10 x 4/131,072 x 10 x 2
- User Selectable Quad / Dual Mode - Choose between two or four independent FIFOs
- Quad Mode offers
  - *Eight discrete clock domain, (four write clocks & four read clocks)*
  - *Four separate write ports, write data to four independent FIFOs*
  - *10-bit wide write ports*
  - *Four separate read ports, read data from any of four independent FIFOs*
  - *Independent set of status flags and control signals for each FIFO*
- Dual Mode offers
  - *Four discrete clock domain, (two write clocks & two read clocks)*
  - *Two separate write ports, write data to two independent FIFOs*
  - *10-bit/20-bit wide write ports*
  - *Two separate read ports, read data from any of two independent FIFOs*
  - *Independent set of status flags and control signals for each FIFO*
  - *Bus-Matching on read and write port x10/x20*
  - *Maximum depth of each FIFO is the same as in Quad Mode*
- Up to 200MHz operating frequency or 2Gbps throughput in SDR mode
- Up to 100MHz operating frequency or 2Gbps throughput in DDR mode
- Double Data Rate, DDR is selectable, providing up to 400Mbps bandwidth per data pin
- User selectable Single or Double Data Rate modes on both the write port(s) and read port(s)
- All I/Os are LVTTL/ HSTL/ eHSTL user selectable
- 3.3V tolerant inputs in LVTTL mode
- ERCLK and $\overline{\text{EREN}}$ Echo outputs on all read ports
- Write enable $\overline{\text{WEN}}$ and Chip Select $\overline{\text{WCS}}$ input for each write port
- Read enable $\overline{\text{REN}}$ and Chip Select $\overline{\text{RCS}}$ input for each read port
- User Selectable IDT Standard mode (using $\overline{\text{EF}}$ and $\overline{\text{FF}}$) or FWFT mode (using $\overline{\text{IR}}$ and $\overline{\text{OR}}$)
- Programmable Almost Empty and Almost Full flags per FIFO
- Dedicated Serial Port for flag offset programming
- Power Down pin minimizes power consumption
- 2.5V Supply Voltage
- Available in a 324-pin PBGA, 1mm pitch, 19mm x 19mm
- IEEE 1149.1 compliant JTAG port provides boundary scan function
- Low Power, High Performance CMOS technology
- Industrial temperature range (-40°C to +85°C)
- Green parts available, see ordering information

FUNCTIONAL BLOCK DIAGRAMS



(See next page for Dual Mode)

FUNCTIONAL BLOCK DIAGRAMS (CONTINUED)

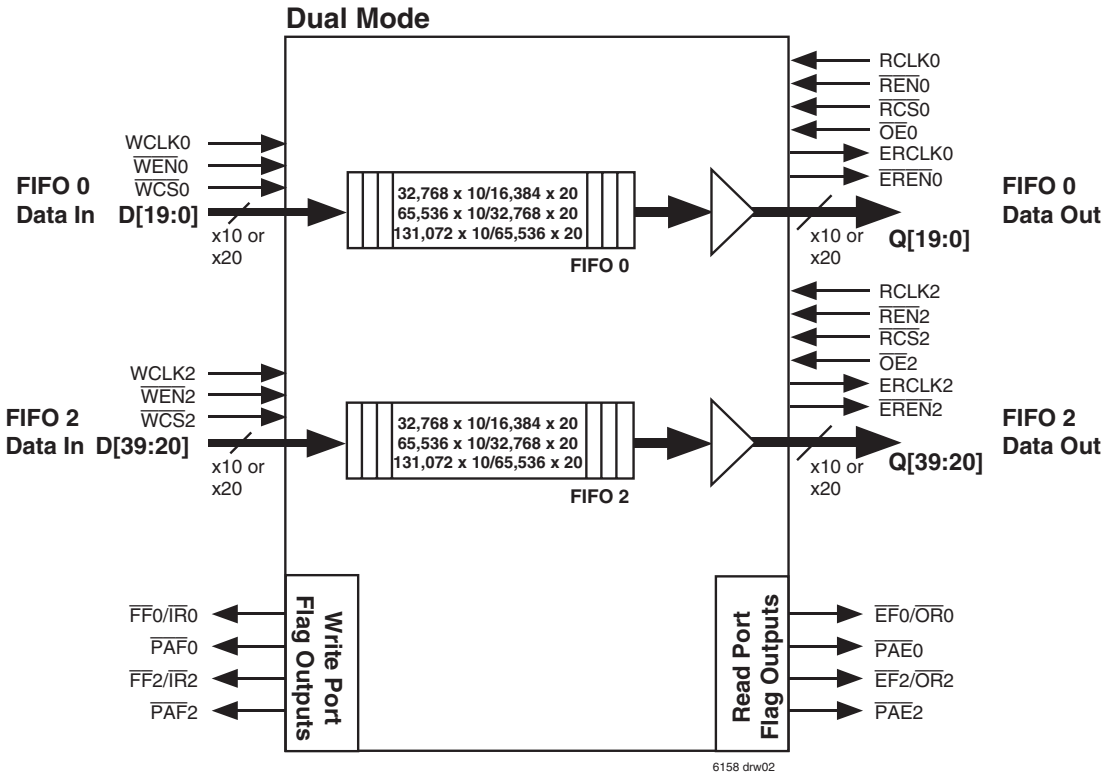


Table of Contents

Features 1
Description 4
Pin Configuration 6
Pin Descriptions 7
Device Characteristics 11
DC Electrical Characteristics 12
AC Electrical Characteristics 14
AC Test Conditions 15
Functional Description 17
Signal Descriptions 23
JTAG Timing Specifications 29

List of Tables

Table 1 — Device Configuration 17
Table 2 — Default Programmable Flag Offsets 17
Table 3 — Status Flags for IDT Standard mode 20
Table 4 — Status Flags for FWFT mode 20
Table 5 — I/O Voltage Level Associations 21
Table 6 — TSKEW Measurement 27

List of Figures

Figure 1. Quad/Dual Block Diagram 5
Figure 2a. AC Test Load 15
Figure 2b. Lumped Capacitive Load, Typical Derating 15
Figure 3. Programmable Flag Offset Programming Methods 18
Figure 4. Offset Registers Serial Bit Sequence 19
Figure 5. Bus-Matching in Dual mode 22
Figure 6. Echo Read Clock and Data Output Relationship 27
Figure 7. Standard JTAG Timing 28
Figure 8. JTAG Architecture 29
Figure 9. TAP Controller State Diagram 30
Figure 10. Master Reset Timing 33
Figure 11. Partial Reset Timing 34
Figure 12. Write Cycle and Full Flag Timing (Quad mode, IDT Standard mode, SDR to SDR) 35
Figure 13. Write Cycle and Full Flag Timing (Quad mode, IDT Standard mode, DDR to DDR) 36
Figure 14. Write Cycle and Full Flag Timing (Dual mode, IDT Standard mode, DDR to SDR, x10 In to x20 Out) 37
Figure 15. Write Cycle and Full Flag (Dual mode, IDT Standard mode, SDR to DDR, x20 In to x10 Out) 38
Figure 16. Write Cycle and Output Ready Timing (Quad mode, FWFT mode, SDR to SDR) 39
Figure 17. Write Cycle and Output Ready Timing (Quad mode, FWFT mode, DDR to DDR) 40
Figure 18. Read Cycle, Output Enable and Empty Flag Timing (Quad mode, IDT Standard mode, SDR to SDR) 41
Figure 19. Read Cycle, Output Enable and Empty Flag Timing (Quad mode, IDT Standard mode, DDR to DDR) 42
Figure 20. Read Cycle and Empty Flag Timing (Dual mode, IDT Standard mode, DDR to SDR, x20 In to x10 Out) 43
Figure 21. Read Cycle and Empty Flag Timing (Dual mode, IDT Standard mode, SDR to DDR, x10 In to x20 Out) 44
Figure 22. Read Timing and Output Ready Flag (Quad mode, FWFT mode, SDR to SDR) 45
Figure 23. Read Timing and Output Ready Timing (Quad mode, FWFT mode, DDR to DDR) 46
Figure 24. Read Cycle and Read Chip Select (Quad mode, IDT Standard mode, SDR to SDR) 47
Figure 25. Read Cycle and Read Chip Select Timing (Quad mode, FWFT mode, SDR to SDR) 48
Figure 26. Echo Read Clock and Read Enable Operation (Quad mode, IDT Standard mode, DDR to DDR) 49
Figure 27. Echo RCLK and Echo Read Enable Operation (Quad mode, FWFT mode, SDR to SDR) 50
Figure 28. Echo Read Clock and Read Enable Operation (Quad mode, IDT Standard mode, SDR to SDR) 51
Figure 29. Loading of Programmable Flag Registers (IDT Standard and FWFT modes) 52
Figure 30. Reading of Programmable Flag Registers (IDT Standard and FWFT modes) 52
Figure 32. Synchronous Programmable Almost-Empty Flag Timing (Quad mode, IDT Standard and FWFT mode, SDR to SDR) 53
Figure 31. Synchronous Programmable Almost-Full Flag Timing (Quad mode, IDT Standard and FWFT mode, SDR to SDR) 53
Figure 33. Asynchronous Programmable Almost-Full Flag Timing (Quad mode, IDT Standard and FWFT mode, SDR to SDR) 54
Figure 34. Asynchronous Programmable Almost-Empty Flag Timing (Quad mode, IDT Standard and FWFT mode, SDR to SDR) 54
Figure 35. Power Down Operation 55

DESCRIPTION

The IDT72T54242/72T54252/72T54262 Quad/Dual TeraSync FIFO devices are ideal for many applications where data stream convergence and parallel buffering of multiple data paths are required. These applications may include communication systems such as data bandwidth aggregation, data acquisition systems and medical equipment, etc. The Quad/Dual FIFO allows the user to select either two or four individual internal FIFOs for operation. Each internal FIFO has its own discrete read and write clock, independent read and write enables, and separate status flags. The density of each FIFO is fixed.

If Quad mode is selected, there will be a total of eight clock domains, four read and four write clocks. Data can be written into any of the four write ports totally independent of any other port, and can be read out of any of the four read ports corresponding to their respective write port. Each port has its own control enables and status flags and is 10 bits wide. The device functions as four separate 10-bit wide FIFOs.

If Dual mode is selected, there will be a total of four clock domains, two read and two write clocks. Data can be written into any of the two write ports totally independent of any other port, and can be read out of any of the two read ports corresponding to their respective write port. Each port has its own control enables and status flags. All input and output ports have bus-matching capabilities of x10 or x20 bits wide.

As typical with most IDT FIFOs, two types of data transfer are available, IDT Standard mode and First Word Fall Through (FWFT) mode. This affects the device operation and also the flag outputs. The device provides eight flag outputs per input and output port. A dedicated Serial Clock is used for programming the flag offsets. This clock is also used for reading the offset values. The serial read and write operations are performed via the SCLK, FWFT/SI, $\overline{SWEN}$, $\overline{SREN}$, and SDO pins. The flag offsets can also be programmed using the JTAG port. If this option is selected, the SCLK, $\overline{SWEN}$, and $\overline{SREN}$ pins must be disabled.

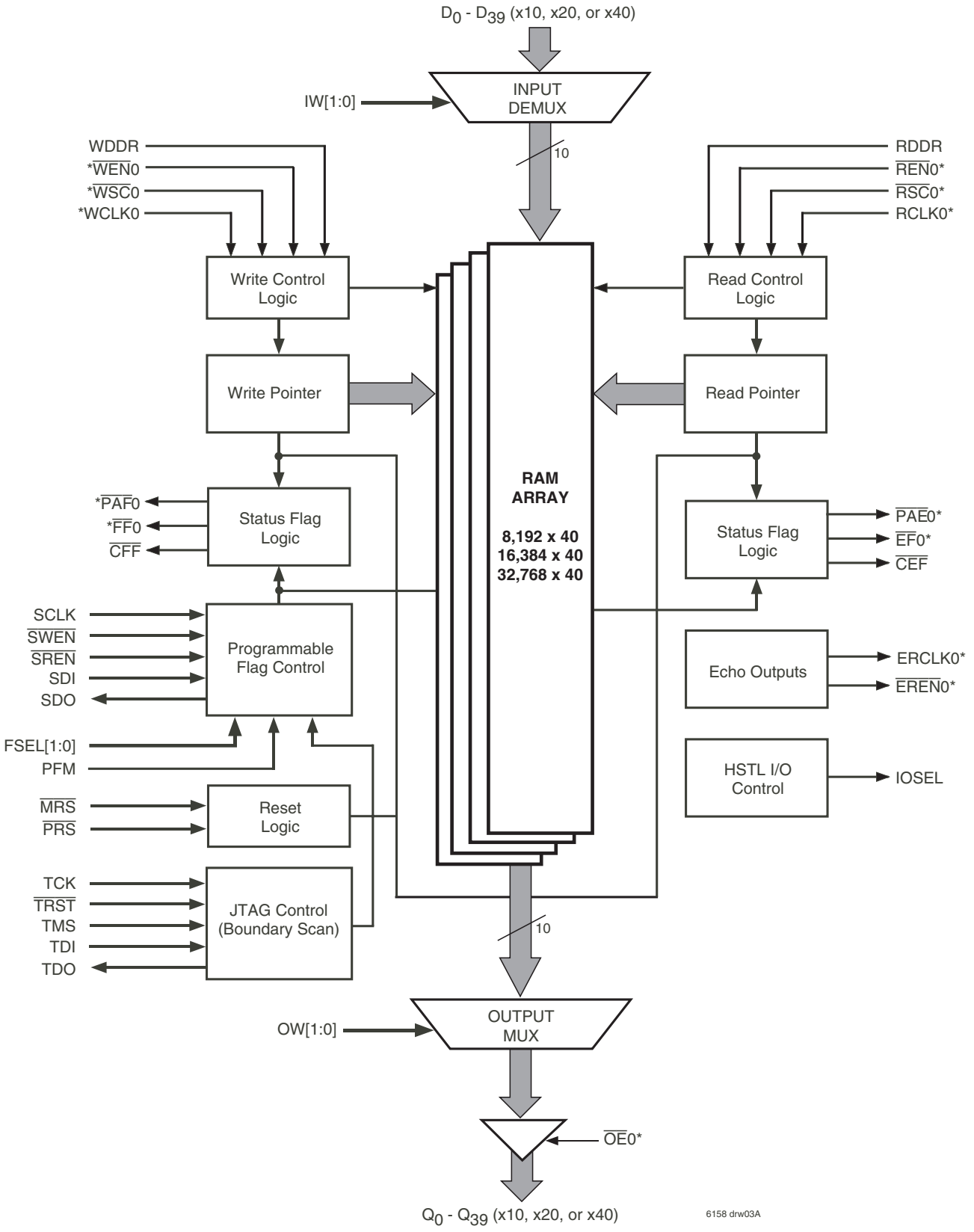
The Quad/Dual device offers a maximum throughput of 2Gbps per port, with selectable SDR or DDR data transfer modes for the inputs and outputs. In SDR mode, the input clock can operate up to 200MHz. Data will transition/latch on the rising edge of the clock. In DDR mode, the input clock can operate up to 100 MHz, with data transitioning/latched on both rising and falling edges of the clock. The advantage of DDR is that it can achieve the same throughput as SDR with only half the number of bits, assuming the frequency is constant. For example, a 4Gbps throughput in SDR is 100MHz x 40 bits. In DDR mode, it is 100MHz x 20 bits, because two bits transition per clock cycle.

All Read ports provide the user with a dedicated Echo Read Enable, $\overline{EREN}$ and Echo Read Clock, ERCLK output. These outputs aid in high speed applications where synchronization of the input clock and data of receiving device is critical. Otherwise known as "Source Synchronous Clocking," the echo outputs provide tighter synchronization of the data transmitted from the FIFO and the read clock interfacing the FIFO outputs.

A Master Reset input is provided and all setup and configuration pins are latched with respect to a Master Reset pulse. For example, the mode of operation, bus-matching, and data rate are selected at Master Reset. A Partial Reset is provided for each internal FIFO. When a Partial Reset is performed on a FIFO the read and write pointers of that FIFO are reset to the first memory location. The flag offset values, timing modes, and initial configurations are retained.

The Quad/Dual device has the capability of operating its I/O at either 2.5V LVTTL, 1.5V HSTL or 1.8V eHSTL levels. A Voltage Reference, Vref input is provided for HSTL and eHSTL interfaces. The type of I/O is selected via the IOSEL pin. The core supply voltage of the device, V_{CC} is always 2.5V, however the output pins have a separate supply, V_{DDQ} which can be 2.5V, 1.8V, or 1.5V. The inputs of this device are 3.3V tolerant when V_{DDQ} is set to 2.5V. The device also offers significant power savings, most notably achieved by the presence of a Power Down input, $\overline{PD}$.

A JTAG test port is provided. The Quad/Dual device has a fully functional Boundary Scan feature, compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

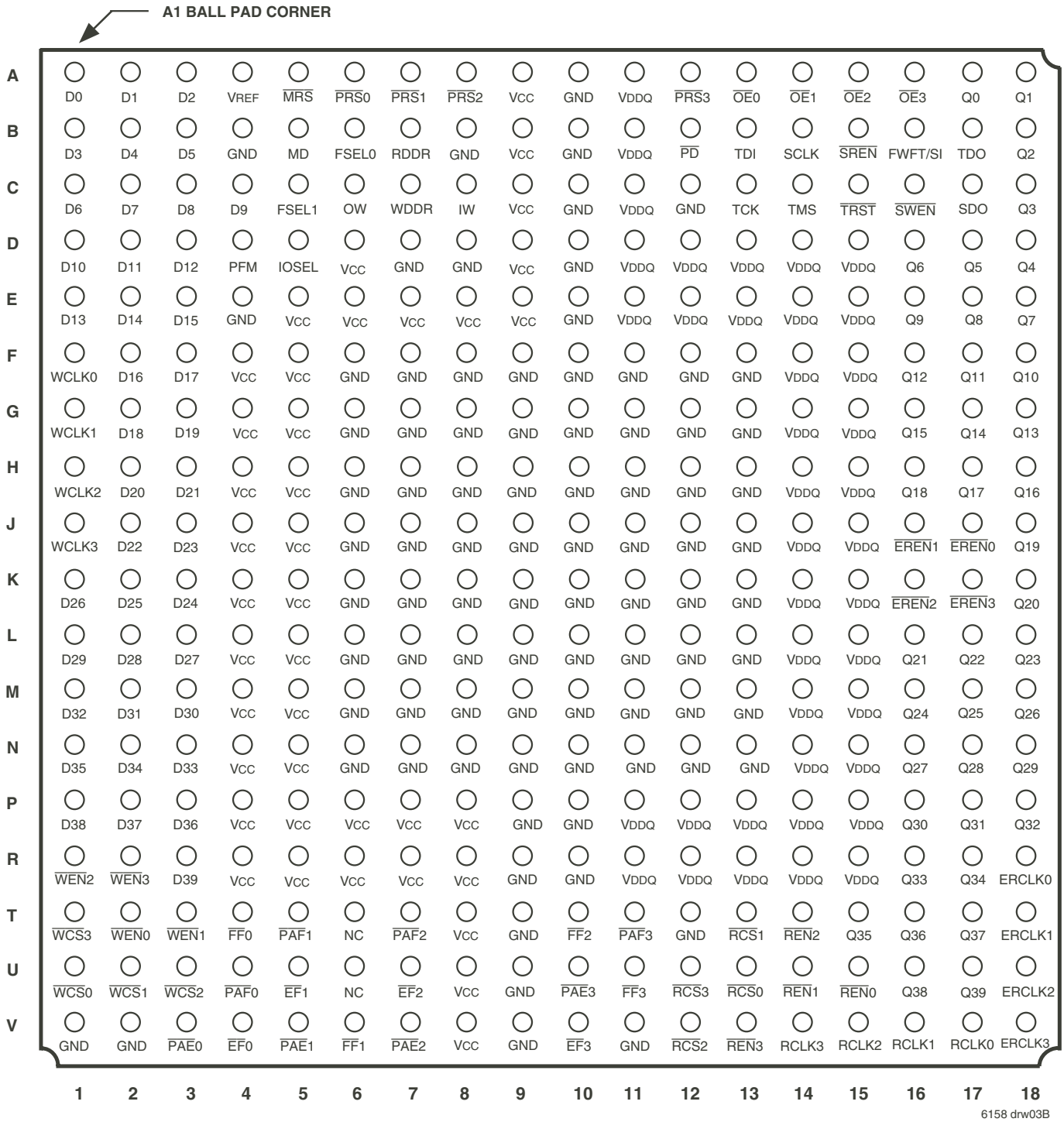


NOTES:

1. This block diagram only shows the architecture for FIFO 0. There are a total of four FIFOs inside this device all with the identical architecture.
2. *Denotes dedicated signal for each internal FIFO inside the device.

Figure 1. Quad/Dual Block Diagram

PIN CONFIGURATION



NOTE:
1. NC = No Connection.

PBGA (BB324-1, order code: BB)
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O Type	Description
D[39:0]	Data Input Bus	HSTL-LVTTL INPUT	These are the data inputs for the device. Data is written into the part via these inputs using the respective write port clocks and enables. In Quad mode, these inputs provide four separate busses to the four separate FIFOs. D[9:0] is FIFO[0], D[19:10] is FIFO[1], D[29:20] is FIFO[2], D[39:30] is FIFO[3]. In Dual mode, these inputs provide two separate busses to the two separate FIFOs. D[19:0] is FIFO[0], D[39:20] is FIFO[2]. Any unused inputs should be tied to GND.
$\overline{EF}$0/1/2/3, $\overline{OR}$0/1/2/3	Empty Flag 0/1/2/3 or Output Ready Flags 0/1/2/3	HSTL-LVTTL OUTPUT(1)	These are the Empty Flags (IDT Standard mode) or Output Ready Flag (FWFT mode) corresponding to each of the four FIFOs on the read port. If Dual mode is selected $\overline{EF}$1/$\overline{OR}$1 and $\overline{EF}$3/$\overline{OR}$3 are not used and can be left floating.
ERCLK0/1/2/3	Echo Read Clock 0/1/2/3	HSTL-LVTTL OUTPUT(1)	These are the echo clock outputs corresponding to each of the four FIFOs on the read port. The echo read clock is guaranteed to transition after the slowest output data switching. If Dual mode is selected ERCLK1 and ERCLK3 are not used and can be left floating
$\overline{EREN}$0/1/2/3	Echo Read Enable 0/1/2/3	HSTL-LVTTL OUTPUT(1)	These are the echo read enable outputs corresponding to each of the four FIFOs on the read port. The echo read enable is synchronous to the RCLK input and is active when a read operation has occurred and a new word has been placed onto the data output bus. If Dual mode is selected $\overline{EREN}$1 and $\overline{EREN}$3 are not used and can be left floating.
$\overline{FF}$0/1/2/3, $\overline{IR}$0/1/2/3	Full Flags 0/1/2/3 or Input Ready Flags 0/1/2/3	HSTL-LVTTL OUTPUT(1)	These are the Full Flags (IDT Standard mode) and Input Ready Flags (FWFT mode) corresponding to each of the four FIFOs on the read port. If Dual mode is selected $\overline{FF}$1/$\overline{IR}$1 and $\overline{FF}$3/$\overline{IR}$3 are not used and can be left floating.
FSEL [1:0]	Flag Select	HSTL-LVTTL INPUT	Flag select default offset pins. During master reset, the FSEL pins are used to select one of four default $\overline{PAE}$ and $\overline{PAF}$ offsets. Both the $\overline{PAE}$ and the $\overline{PAF}$ offsets are programmed to the same value. Values are: 00 = 7; 01 = 63; 10 = 127; 11 = 1023. The offset value selected is supplied to all internal FIFOs.
FWFT/SI	First Word Fall Through/ Serial Input	HSTL-LVTTL INPUT	During Master Reset, FWFT=1 selects First Word Fall Through mode, FWFT=0 selects IDT Standard mode. After Master Reset this pin is used for the Serial Data input for the programming of the $\overline{PAE}$ and $\overline{PAF}$ flag's offset registers.
IOSEL	I/O Select	CMOS(2) INPUT	This input determines whether the inputs will operate in LVTTL or HSTL/eHSTL mode. If IOSEL pin is HIGH, then all inputs and outputs that are designated "LVTTL or HSTL" in this section will be set to HSTL. If IOSEL is LOW then LVTTL is selected. This signal must be tied to either VCC or GND for proper operation.
IW	Input Width	CMOS(2) INPUT	If Dual mode is selected , this pin is used during master reset to select the input word width bus size for the device. 0 = x10; 1 = x20. If Quad mode is selected the input word width will be x10 regardless of IW. IW must be tied to VCC or GND and cannot be left floating.
MD	Mode	CMOS(2) INPUT	This mode selection pin is used during master reset to select either Quad or Dual mode operation. A HIGH on this pin selects Quad mode, a LOW selects Dual mode.
$\overline{MRS}$	Master Reset	HSTL-LVTTL INPUT	This input provides a full device reset. All set-up pins are latched based on a master reset operation. Read and write pointers will be reset to the first location memory. All flag offsets are cleared and reset to default values determined by FSEL[1:0].
$\overline{OE}$0/1/2/3	Output Enable 0/1/2/3	HSTL-LVTTL INPUT	These are the output enables corresponding to each individual FIFO on the read port. All data outputs will be placed into High Impedance if this pin is High. These inputs are asynchronous. If Dual mode is selected $\overline{OE}$1 and $\overline{OE}$3 are not used and should be tied to VCC.
OW	Output Width	CMOS(2) INPUT	If Dual mode is selected, this pin is used during master reset to select the output word width bus size for the device. 0 = x10; 1 = x20. If Quad mode is selected the output word width will be x10 regardless of OW. OW must be tied to VCC or GND and cannot be left floating.
$\overline{PAE}$0/1/2/3	Programmable Almost-Empty Flags 0/1/2/3	HSTL-LVTTL OUTPUT(1)	These are the programmable almost empty flags that can be used as an early indicator for the empty boundary of each FIFO. The $\overline{PAE}$ flags can be set to one of four default offsets determined by the state of FSEL0 and FSEL1 during master reset. The $\overline{PAE}$ offset value can also be written and read from serially by either the JTAG port or the serial programming pins (SCLK, SI, SDO, $\overline{SWEN}$, $\overline{SREN}$). This flag can operate in synchronous or asynchronous mode depending on the sate of the PFM pin during master reset. If Dual mode is selected $\overline{PAE}$1 and $\overline{PAE}$3 are not used and can be left floating.
$\overline{PAF}$0/1/2/3	Programmable Almost-Full Flags 0/1/2/3	HSTL-LVTTL OUTPUT(1)	These are the programmable almost full flags that can be used as an early indicator for the full boundary of each FIFO. The $\overline{PAF}$ flags can be set to one of four default offsets determined by the state of FSEL0 and FSEL1 during master reset. The $\overline{PAF}$ offset value can also be written and read from serially by either the JTAG port or the serial programming pins (SCLK, SI, SDO, $\overline{SWEN}$, $\overline{SREN}$).

PIN DESCRIPTIONS (CONTINUED)

Symbol	Name	I/O Type	Description
$\overline{PAF}$0/1/2/3 (Continued)	Programmable Almost-Full Flags0-3	HSTL-LVTTL OUTPUT(1)	This flag can operate in synchronous or asynchronous mode depending on the sate of the PFM pin during master reset. If Dual mode is selected $\overline{PAF}$1 and $\overline{PAF}$3 are not used and can be left floating.
$\overline{PD}$	Power Down	HSTL-LVTTL INPUT	This input provides considerable power saving in HSTL/eHSTL mode. If this pin is low, the input level translators for all the data input pins, clocks and non-essential control pins are turned off. When $\overline{PD}$ is brought high, power-up sequence timing will have to be adhered to before the inputs will be recognized. It is essential that the user respect these conditions when powering down the part and powering up the part, so as to not produce runt pulses or glitches on the clocks if the clocks are free running. $\overline{PD}$ does not provide any power consumption savings when the inputs are configured for LVTTL.
PFM	Programmable Flag Mode	CMOS(2) INPUT	During master reset, a HIGH on PFM selects synchronous $\overline{PAE}$/$\overline{PAF}$ flag timing, a Low during master reset selects asynchronous $\overline{PAE}$/$\overline{PAF}$ flag timing. This pin controls all $\overline{PAE}$/$\overline{PAF}$ flag outputs.
$\overline{PRS}$0/1/2/3	Partial Reset	HSTL-LVTTL INPUT	These are the partial reset inputs for each internal FIFO. The read, write, flag pointers, and output registers will all be set to zero when partial reset is activated. During partial reset, the existing mode (IDT or FWFT), input/output bus width and rate mode, and the programmable flag settings are all retained. If Dual mode is selected, $\overline{PRS}$1 and $\overline{PRS}$3 are not used and should be tied to VCC.
Q[39:0]	Data Output Bus	HSTL-LVTTL OUTPUT(1)	These are the Data Outputs for the device. Data is read from the part via these outputs using the respective read port clocks and enables. In Quad mode, these outputs provide four separate busses from the four separate FIFO's. Q[9:0] is FIFO[0], Q[19:10] is FIFO[1], Q[29:20] is FIFO[2], Q[39:30] is FIFO[3]. In Dual mode these outputs provide two separate busses from the two separate FIFO's. Q[19:0] is FIFO[0] and Q[39:20] is FIFO[2].
RCLK0/1/2/3	Read Clock 0/1/2/3	HSTL-LVTTL INPUT	These are the clock inputs corresponding to each of the four FIFOs on the read port. If Dual mode is selected then RCLK1 and RCLK3 are not used and should be tied to GND. In SDR mode data will be accessed on the rising edge of RCLK when $\overline{REN}$ and $\overline{RCS}$ are LOW at the rising edge of RCLK. In DDR mode data will be accessed on both rising and falling edge of RCLK when $\overline{REN}$ is LOW.
$\overline{RCS}$0/1/2/3	Read Chip Select	HSTL-LVTTL INPUT	These are the read chip select inputs corresponding to each of the four FIFOs on the read port. This pin provides synchronous control of the read port and high impedance control of the output data bus. $\overline{RCS}$ is only sampled on the rising edge of RCLK. During master or partial reset this input is a don't care, if $\overline{OE}$ is LOW the data inputs will be in Low-Impedance regardless of the state of $\overline{RCS}$. If Dual mode is selected then $\overline{RCS}$1 and $\overline{RCS}$3 are not used and should be tied to VCC.
$\overline{REN}$0/1/2/3	Read Enable	HSTL-LVTTL INPUT	These are the read enable inputs corresponding to each of the four FIFOs on the read port. In SDR, when this signal (and $\overline{RCS}$) are LOW data will be sent from the FIFO memory to the output bus on every rising edge of RCLK. In DDR mode, data will be accessed on both rising and falling edges of RCLK. Note in DDR mode the $\overline{REN}$ and $\overline{RCS}$ are only sampled on the rising edge of RCLK. New data will always begin from the rising edge not the falling edge of RCLK. If Dual mode is selected then $\overline{REN}$1 and $\overline{REN}$3 are not used and should be tied to VCC.
RDDR	Read Port DDR	CMOS(2) INPUT	During master reset, this pin selects the output port to operate in DDR or SDR format. If RDDR is HIGH, then a word is read on the rising and falling edge of the appropriate RCLK0, 1, 2 and 3 input. If RDDR is LOW, then a word is read only on the rising edge of the appropriate RCLK0, 1, 2 and 3 inputs.
SCLK	Serial Clock	HSTL-LVTTL INPUT	Serial clock for writing and reading the $\overline{PAE}$ and $\overline{PAF}$ offset registers. On the rising edge of each SCLK, when $\overline{SWEN}$ is low, one bit of data is shifted into the $\overline{PAE}$ and $\overline{PAF}$ registers. On the rising edge of each SCLK, when $\overline{SREN}$ is low, one bit of data is shifted out of the $\overline{PAE}$ and $\overline{PAF}$ offset registers. The reading of the $\overline{PAE}$ and $\overline{PAF}$ registers is non-destructive. If programming of the $\overline{PAE}$/$\overline{PAF}$ offset registers are done via the JTAG port, this input must be tied to VCC.
SDO	Serial Data	LVTTL OUTPUT(1)	This output is used to read data from the programmable flag offset registers. It is used in conjunction with the $\overline{SREN}$ and SCLK signals.
$\overline{SREN}$	Serial Read Enable	HSTL-LVTTL INPUT	When $\overline{SREN}$ is brought LOW before the rising edge of SCLK, the contents of the $\overline{PAE}$ and $\overline{PAF}$ offset registers are copied to a serial shift register. While $\overline{SREN}$ is maintained LOW, on each rising edge of SCLK, one bit of data is shifted out of this serial shift register through the SDO output pin. If programming of the $\overline{PAE}$/$\overline{PAF}$ offset registers is done via the JTAG port, this input must be tied HIGH.
$\overline{SWEN}$	Serial Write Enable	HSTL-LVTTL INPUT	On each rising edge of SCLK when $\overline{SWEN}$ is LOW, data from the FWFT/SI pin is serially loaded into the $\overline{PAE}$ and $\overline{PAF}$ registers. If programming of the $\overline{PAE}$/$\overline{PAF}$ offset registers is done via the JTAG port, this input must be tied HIGH.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Name	I/O Type	Description
TCK[3]	JTAG Clock	HSTL-LVTTL INPUT	Clock input for JTAG function. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data from TMS and TDI are sampled on the rising edge of TCK and outputs change on the falling edge of TCK. If the JTAG function is not used this signal needs to be tied to GND.
TDI[3]	JTAG Test Data Input	HSTL-LVTTL INPUT	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded via the TDI on the rising edge of TCK to either the Instruction Register, ID Register and Bypass Register. An internal pull-up resistor forces TDI HIGH if left unconnected.
TDO[3]	JTAG Test Data Output	HSTL-LVTTL OUTPUT	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded output via the TDO on the falling edge of TCK from either the Instruction Register, ID Register and Bypass Register. This output is high impedance except when shifting, while in SHIFT-DR and SHIFT-IR controller states.
TMS[3]	JTAG Mode Select	HSTL-LVTTL INPUT	TMS is a serial input pin. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pull-up resistor forces TMS HIGH if left unconnected.
$\overline{TRST}$[3]	JTAG Reset	HSTL-LVTTL INPUT	$\overline{TRST}$ is an asynchronous reset pin for the JTAG controller. The JTAG TAP controller does not automatically reset upon power-up, thus it must be reset by either this signal or by setting TMS= HIGH for five TCK cycles. If the TAP controller is not properly reset then the FIFO outputs will always be in high-impedance. If the JTAG function is used but the user does not want to use $\overline{TRST}$, then $\overline{TRST}$ can be tied with $\overline{MRS}$ to ensure proper FIFO operation. If the JTAG function is not used then this signal needs to be tied to GND. An internal pull-up resistor forces $\overline{TRST}$ HIGH if left unconnected.
WCLK0/1/2/3	Write Clock 0/1/2/3	HSTL-LVTTL INPUT	These are the clock inputs corresponding to each of the four FIFOs on the write port. If Dual mode is selected then WCLK1 and WCLK3 are not used and should be tied to GND. In SDR mode data will be written on the rising edge of WCLK when $\overline{WEN}$ and $\overline{WCS}$ are LOW at the rising edge of WCLK. In DDR mode data will be written on both rising and falling edge of WCLK when $\overline{WEN}$ and $\overline{WCS}$ are LOW at the rising edge of WCLK.
$\overline{WCS}$0/1/2/3	Write Chip Select	HSTL-LVTTL INPUT	These are the write chip select inputs corresponding to each of the four FIFOs on the write port. This pin can be regarded as a second write enable input, enabling/disabling write operations. $\overline{WCS}$ is only sampled on the rising edge of WCLK. If Dual mode is selected then $\overline{WCS}$1 and $\overline{WCS}$3 are not used and should be tied to VCC.
WDDR	Write Port DDR	CMOS[2] INPUT	During master reset, this pin selects the input port to operate in DDR or SDR format. If WDDR is HIGH, then a word is written on the rising and falling edge of the appropriate WCLK0, 1, 2 and 3 input. If WDDR is LOW, then a word is written only on the rising edge of the appropriate WCLK0, 1, 2 and 3 inputs.
$\overline{WEN}$0/1/2/3	Write Enable 0/1/2/3	HSTL-LVTTL INPUT	These are the write enable inputs corresponding to each of the four FIFOs on the write port. In SDR, when this signal (and $\overline{WCS}$) are LOW data on the databus will be written into the FIFO memory on every rising edge of WCLK. In DDR mode, data will be written on both rising and falling edges of WCLK. Note in DDR mode the $\overline{WEN}$ and $\overline{WCS}$ are only sampled on the rising edge of WCLK. New data will always begin writing from the rising edge, not the falling edge of WCLK. If Dual mode is selected then $\overline{WEN}$1 and $\overline{WEN}$3 are not used and should be tied to VCC.
VCC	+2.5V Supply	Power	These are VCC core power supply pins and must all be connected to a +2.5V supply rail.
VDDQ	Output Rail Voltage	Power	This pin should be tied to the desired voltage rail for providing to the output drivers. Nominally 1.5V or 1.8V for HSTL, 2.5V for LVTTL.
GND	Ground Pin	Ground	These ground pins are for the core device and must be connected to the GND rail.
Vref	Reference voltage	Power	This is a Voltage Reference input and must be connected to a voltage level determined in the Voltage Recommended DC Operating Conditions section. This provides the reference voltage when using HSTL class inputs. If HSTL class inputs are not being used, this pin must be connected to GND.

NOTES:
1. All unused outputs may be left floating.
2. All CMOS pins should remain unchanged. CMOS format means that the pin is intended to be tied directly to VCC or GND and these particular pins are not tested for VIH or VIL.
3. These pins are for the JTAG port. Please refer to pages 27-31 and Figures 7-9.

QUAD/DUAL I/O USAGE SUMMARY

SET-UP, CONFIGURATION & RESET PINS

Regardless of the mode of operation, (Quad or Dual), the following inputs must be always be used. These inputs must be set-up with respect to master reset as they are latched during this time.

WDDR – Write Port DDR/SDR selection
RDDR – Read Port DDR/SDR selection
MD – Mode Selection
OW – Output width
IW – Input Width
FSEL[1:0] – Flag offset default values
IOSEL – I/O Level Selection
PFM – Programmable Flag Mode
FWFT/SI – First word Fall Through or IDT Standard mode

SERIAL PORT

The following pins are used when user programming of the Programmable Flag offsets is required:

SCLK – Serial Clock
$\overline{SWEN}$ – Serial Write Enable
$\overline{SREN}$ – Serial Read Enable
FWFT/SI – Serial Data In
SDO – Serial Data Out

QUAD MODE

The following inputs/ outputs should be used when Mux mode is selected by the user:

INPUTS:
WCLK0, WCLK1, WCLK2, WCLK3 – Four write port clocks
$\overline{WEN}$0, $\overline{WEN}$1, $\overline{WEN}$2, $\overline{WEN}$3 – Four write port enables
$\overline{WCS}$0, $\overline{WCS}$1, $\overline{WCS}$2, $\overline{WCS}$3 – Four write port chip selects
RCLK0, RCLK1, RCLK2, RCLK3 – Four read port clocks
$\overline{REN}$0, $\overline{REN}$1, $\overline{REN}$2, $\overline{REN}$3 – Four read port enables
$\overline{RCS}$0, $\overline{RCS}$1, $\overline{RCS}$2, $\overline{RCS}$3, – Four read port chip selects
$\overline{OE}$0, $\overline{OE}$1, $\overline{OE}$2, $\overline{OE}$3 – Four read port output enables

OUTPUTS:
ERCLK0, ERCLK1, ERCLK2, ERCLK3 – Four read port echo read clocks
$\overline{EREN}$0, $\overline{EREN}$1, $\overline{EREN}$2, $\overline{EREN}$3 – Four read port echo read enables
$\overline{EF}$0/$\overline{OR}$0, $\overline{EF}$1/$\overline{OR}$1, $\overline{EF}$2/$\overline{OR}$2, $\overline{EF}$3/$\overline{OR}$3 – Four read port Empty/Output Ready Flags
$\overline{FF}$0/$\overline{IR}$0, $\overline{FF}$1/$\overline{IR}$1, $\overline{FF}$2/$\overline{IR}$2, $\overline{FF}$3/$\overline{IR}$3 – Four write port full/ input ready flags
$\overline{PAE}$0, $\overline{PAE}$1, $\overline{PAE}$2, $\overline{PAE}$3 – Four read port programmable almost empty flags
$\overline{PAF}$0, $\overline{PAF}$1, $\overline{PAF}$2, $\overline{PAF}$3 – Four write port programmable almost empty flags

DUAL MODE

The following inputs/ outputs should be used when Mux mode is selected by the user:

INPUTS:
WCLK0, WCLK2 – Two write port clocks
$\overline{WEN}$0, $\overline{WEN}$2 – Two write port enables
$\overline{WCS}$0, $\overline{WCS}$2 – Two write port chip selects
RCLK0, RCLK2 – Two read port clocks
$\overline{REN}$0, $\overline{REN}$2 – Two read port enables
$\overline{RCS}$0, $\overline{RCS}$2 – Two read port chip selects
$\overline{OE}$0, $\overline{OE}$2 – Two read port output enables

OUTPUTS:
ERCLK0, ERCLK2 – Two read port echo read clock outputs
$\overline{EREN}$0, $\overline{EREN}$2 – Two read port echo read enable outputs
$\overline{EF}$0/$\overline{OR}$0, $\overline{EF}$2/$\overline{OR}$2 – Two read port empty/output ready flags
$\overline{FF}$0/$\overline{IR}$0, $\overline{FF}$2/$\overline{IR}$2 – Two write port Full/ Input Ready Flags
$\overline{PAE}$0, $\overline{PAE}$2 – Two read port programmable almost empty flags
$\overline{PAF}$0, $\overline{PAF}$2 – Two write port programmable almost full flags

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l & Ind'l	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +3.6(2)	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA
T_J	Maximum Junction Temperature	+150	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Compliant with JEDEC JESD8-5. V_{CC} terminal only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2,3)	Input Capacitance	V_{IN} = 0V	10(3)	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:

1. With output deselected, ($\overline{OE} \geq V_{IH}$).
2. Characterized values, not currently tested.
3. C_{IN} for Vref is 20pF.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage relative to GND		2.375	2.5	2.625	V
V_{DDQ}	Output supply voltage	—LVTTL	2.375	2.5	2.625	V
		— eHSTL	1.7	1.8	1.9	V
		— HSTL	1.4	1.5	1.6	V
V_{REF}(1)	Voltage reference input	— eHSTL	0.8	0.9	1.0	V
		— HSTL	0.68	0.75	0.9	V
V_{IH}	Input high voltage	—LVTTL	1.7	—	3.45	V
		— eHSTL	V_{REF}+0.2	—	V_{DDQ}+0.3	V
		— HSTL	V_{REF}+0.2	—	V_{DDQ}+0.3	V
V_{IL}	Input low voltage	—LVTTL	-0.3	—	0.7	V
		— eHSTL	-0.3	—	V_{REF}-0.2	V
		— HSTL	-0.3	—	V_{REF}-0.2	V
T_A	Operating temperature (Commercial)		0	—	+70	°C
T_A	Operating temperature (Industrial)		-40	—	+85	°C

NOTES:

1. V_{REF} is only required for HSTL or eHSTL inputs. V_{REF} should be tied LOW for LVTTL operation.
2. GND = Ground.

DC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 2.5V ± 0.125V, T_A = -40°C to +85°C)

Symbol	Parameter		Min.	Max.	Unit
I_{LI}	Input Leakage Current		–10	+10	µA
I_{LO}	Output Leakage Current		–10	+10	µA
I_{CC3}(2,3)	JTAG Input Leakage Current		—	-16	mA
V_{OH}(1)	Output Logic "1" Voltage,	I_{OH} = –8 mA @LVTTL I_{OH} = –8 mA @eHSTL I_{OH} = –8 mA @HSTL	V_{DDQ}-0.4 V_{DDQ}-0.4 V_{DDQ}-0.4	— — —	V V V
V_{OL}	Output Logic "0" Voltage,	I_{OL} = 8 mA @LVTTL I_{OL} = 8 mA @eHSTL I_{OL} = 8 mA @HSTL	— — —	0.4 0.4 0.4	V V V
I_{CC1}(2,3,4)	Active V_{CC} Current (Quad mode) (See Note 7 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	250(7) 350(7) 350(7)	mA mA mA
I_{CC2}(2,3,4)	Active V_{CC} Current (Dual mode) (See Note 8 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	180(7) 295(7) 295(7)	mA mA mA
I_{DDQ1}(2,3,5)	Active V_{DDQ} Current (Quad mode) (See Note 7 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	50 40 40	mA mA mA
I_{DDQ2}(2,3,5)	Active V_{DDQ} Current (Dual mode) (See Note 8 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	35 20 20	mA mA mA
I_{SB1}(2,3,4)	Standby V_{CC} Current (Quad mode) (See Note 9 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	110(7) 240(7) 240(7)	mA mA mA
I_{SB2}(2,3,4)	Standby V_{CC} Current (Dual mode) (See Note 10 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	100(7) 185(7) 185(7)	mA mA mA
I_{SB3}(2,3,5)	Standby V_{DDQ} Current (Quad mode) (See Note 9 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	40 35 35	mA mA mA
I_{SB4}(2,3,5)	Standby V_{DDQ} Current (Dual mode) (See Note 10 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	30 15 15	mA mA mA
I_{PD1}(3,4)	Power Down V_{CC} Current (Quad mode) (See Note 11 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	15(7) 30(7) 30(7)	mA mA mA
I_{PD2}(3,4)	Power Down V_{CC} Current (Dual mode) (See Note 12 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	15(7) 30(7) 30(7)	mA mA mA
I_{PD3}(3,5)	Power Down V_{DDQ} Current (Quad mode) (See Note 11 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	0.5 0.5 0.5	mA mA mA
I_{PD4}(3,5)	Power Down V_{DDQ} Current (Dual mode) (See Note 12 for test conditions)	--LVTTL -- eHSTL -- HSTL	— — —	0.2 0.2 0.2	mA mA mA

NOTES:

1. Outputs are not 3.3V tolerant.
2. All WCLKs and RCLKs toggling at 20MHz. Data inputs toggling at 10MHz.
3. V_{CC} = 2.5V, $\overline{OE}$0-3 = HIGH.
4. Typical I_{CC1} calculation: for LVTTL I/O: I_{CC1} (Quad mode) = 11.25 x fs
   I_{CC1} (Dual mode) = 7.74 x fs
   for HSTL I/O: I_{CC1} (Quad mode) = 158 + (11.25 x fs)
   I_{CC1} (Dual mode) = 115 + (7.74 x fs)

   where fs = WCLK = RCLK frequency (in MHz)

NOTES CONTINUED ON PAGE 13.

5. Typical I_{DDQ} calculation: With data outputs in High-Impedance: I_{DDQ} (Quad mode) = 0.8 x fs
   I_{DDQ} (Dual mode) = 0.3 x fs
   With data outputs in Low-Impedance: I_{DDQ} (Quad mode and Dual mode) = $\frac{C_L \times V_{DDQ} \times fs \times N}{2000}$
   where fs = WCLK = RCLK frequency (in MHz). C_L = capacitance load (pF), N= Number of outputs switching.
6. Total Power consumed: PT = [(V_{CC} x I_{CC}) + (V_{DDQ} x I_{DDQ})].
7. Maximum value tested wtih RCLK = WCLK = 20MHz at 85°C. Maximum value may differ depending on V_{CC} and temperature.
8. $\overline{WEN}$0-3 = $\overline{REN}$0-3 = LOW, $\overline{WCS}$0-3 = $\overline{RCS}$0-3 = LOW, $\overline{PD}$ = HIGH.
9. $\overline{WEN}$0,2 = $\overline{REN}$0,2 = LOW, $\overline{WCS}$0,2 = $\overline{RCS}$0,2 = LOW, $\overline{PD}$ = HIGH.
10. $\overline{WEN}$0-3 = $\overline{REN}$0-3 = HIGH, $\overline{WCS}$0-3 = $\overline{RCS}$0-3 = HIGH, $\overline{PD}$ = HIGH.
11. $\overline{WEN}$0,2 = $\overline{REN}$0,2 = HIGH, $\overline{WCS}$0,2 = $\overline{RCS}$0,2 = HIGH, $\overline{PD}$ = HIGH.
12. $\overline{WEN}$0-3 = $\overline{REN}$0-3 = HIGH, $\overline{WCS}$0-3 = $\overline{RCS}$0-3 = HIGH, $\overline{PD}$ = LOW.
13. $\overline{WEN}$0,2 = $\overline{REN}$0,2 = HIGH, $\overline{WCS}$0,2 = $\overline{RCS}$0,2 = HIGH, $\overline{PD}$ = LOW.

AC ELECTRICAL CHARACTERISTICS(1)

(Commercial: V_{CC} = 2.5V ± 0.15V, T_A = 0°C to +70°C;Industrial: V_{CC} = 2.5V ± 0.15V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

Symbol	Parameter	Commerical IDT72T54242L5 IDT72T54252L5 IDT72T54262L5		Com'l & Ind'l IDT72T54242L6-7 IDT72T54252L6-7 IDT72T54262L6-7		Unit
		Min.	Max.	Min.	Max.	
f_{S1}	Clock Cycle Frequency (WCLK & RCLK) SDR	—	200	—	150	MHz
f_{S2}	Clock Cycle Frequency (WCLK & RCLK) DDR	—	100	—	75	MHz
t_A	Data Access Time	0.6	3.6	0.6	3.8	ns
t_{CLK1}	Clock Cycle Time SDR	5	—	6.7	—	ns
t_{CLK2}	Clock Cycle Time DDR	10	—	13	—	ns
t_{CLKH1}	Clock High Time SDR	2.3	—	2.8	—	ns
t_{CLKH2}	Clock High Time DDR	4.5	—	6.0	—	ns
t_{CLKL1}	Clock Low Time SDR	2.3	—	2.8	—	ns
t_{CLKL2}	Clock Low Time DDR	4.5	—	6.0	—	ns
t_{DS}	Data Setup Time	1.5	—	2.0	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	ns
t_{ENS}	Enable Setup Time	1.5	—	2.0	—	ns
t_{ENH}	Enable Hold Time	0.5	—	0.5	—	ns
f_C	Clock Cycle Frequency (SCLK)	—	10	—	10	MHz
t_{ASO}	Serial Output Data Access Time	—	20	—	20	ns
t_{SCLK}	Serial Clock Cycle	100	—	100	—	ns
t_{SCKH}	Serial Clock High	45	—	45	—	ns
t_{SCKL}	Serial Clock Low	45	—	45	—	ns
t_{SDS}	Serial Data In Setup	15	—	15	—	ns
t_{SDH}	Serial Data In Hold	5	—	5	—	ns
t_{SENS}	Serial Enable Setup	5	—	5	—	ns
t_{SENH}	Serial Enable Hold	5	—	5	—	ns
t_{RS}(3)	Reset Pulse Width	200	—	200	—	ns
t_{RSS}	Reset Setup Time	15	—	15	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	ns
t_{RSF}	Reset to Flag and Output Time	—	12	—	15	ns
t_{OLZ} ($\overline{OE}$ - Qn)	Output Enable to Output in Low-Impedance	0.6	3.6	0.8	3.8	ns
t_{OHZ}	Output Enable to Output in High-Impedance	0.6	3.6	0.8	3.8	ns
t_{OE}	Output Enable to Data Output Valid	0.6	3.6	0.8	3.8	ns
t_{RCSLZ}	RCLK to Active from High-Impedance	—	3.6	—	3.8	ns
t_{RCSHZ}	RCLK to High-Impedance	—	3.6	—	3.8	ns
t_{PDLZ}	Power Down to Output Low-Impedance	—	19.4	—	19.6	ns
t_{PDHZ}	Power Down to Output High-Impedance	—	13.5	—	13.7	ns
t_{PDL}	Power Down LOW	—	19.4	—	19.6	ns
t_{PDH}	Power Down HIGH	1	—	1	—	µs
t_{WFF}	Write Clock to $\overline{FF}$ or $\overline{IR}$	—	3.6	—	3.8	ns
t_{REF}	Read Clock to $\overline{EF}$ or $\overline{OR}$	—	3.6	—	3.8	ns
t_{PAFS}	Write Clock to Synchronous Programmable Almost-Full Flag	—	3.6	—	3.8	ns
t_{PAES}	Read Clock to Synchronous Programmable Almost-Empty Flag	—	3.6	—	3.8	ns
t_{PAFA}	Write Clock to Asynchronous Programmable Almost-Full Flag	—	10	—	12	ns
t_{PAEA}	Read Clock to Asynchronous Programmable Almost-Empty Flag	—	10	—	12	ns
t_{ERCLK}	RCLK to Echo RCLK Output	—	4.0	—	4.3	ns
t_{CLKEN}	RCLK to Echo $\overline{REN}$ Output	—	3.6	—	3.8	ns
t_{SKEW1}	SKEW time between RCLK and WCLK for $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$ for SDR inputs and outputs	4	—	5	—	ns
t_{SKEW2}	SKEW time between RCLK and WCLK for $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$ in for DDR inputs and outputs	5	—	6	—	ns
t_{SKEW3}	SKEW time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$	5	—	6	—	ns

NOTES:

1. With exception to clock cycle frequency, these parameters apply to both DDR and SDR modes of operation.
2. All AC timings apply to both IDT Standard mode and FWFT mode in both Quad and Dual mode.
3. Pulse width less than the minimum value is not allowed.
4. Values guaranteed by design, not currently tested.
5. Industrial temperature range product for the 6-7ns speed grade is available as a standard device. All other speed grades available by special order.

HSTL
1.5V AC TEST CONDITIONS

Input Pulse Levels	0.25 to 1.25V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.75V
Output Reference Levels	0.75V

NOTES:
1. V_{DDQ} = 1.5V.
2. V_{REF} = 0.75V.

AC TEST LOADS

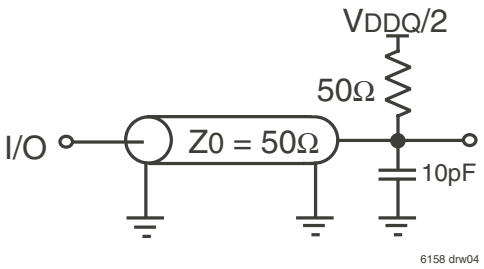


Figure 2a. AC Test Load

EXTENDED HSTL
1.8V AC TEST CONDITIONS

Input Pulse Levels	0.4 to 1.4V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.9V
Output Reference Levels	0.9V

NOTES:
1. V_{DDQ} = 1.8V.
2. V_{REF} = 0.9V.

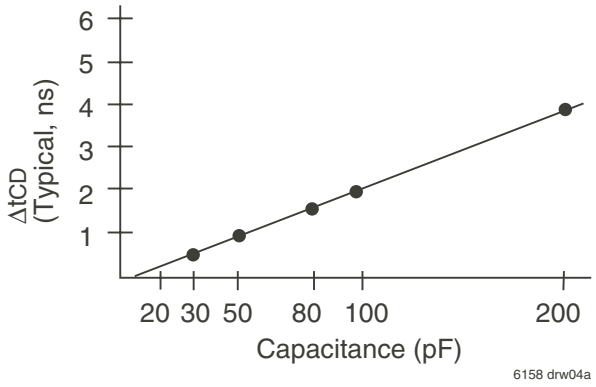


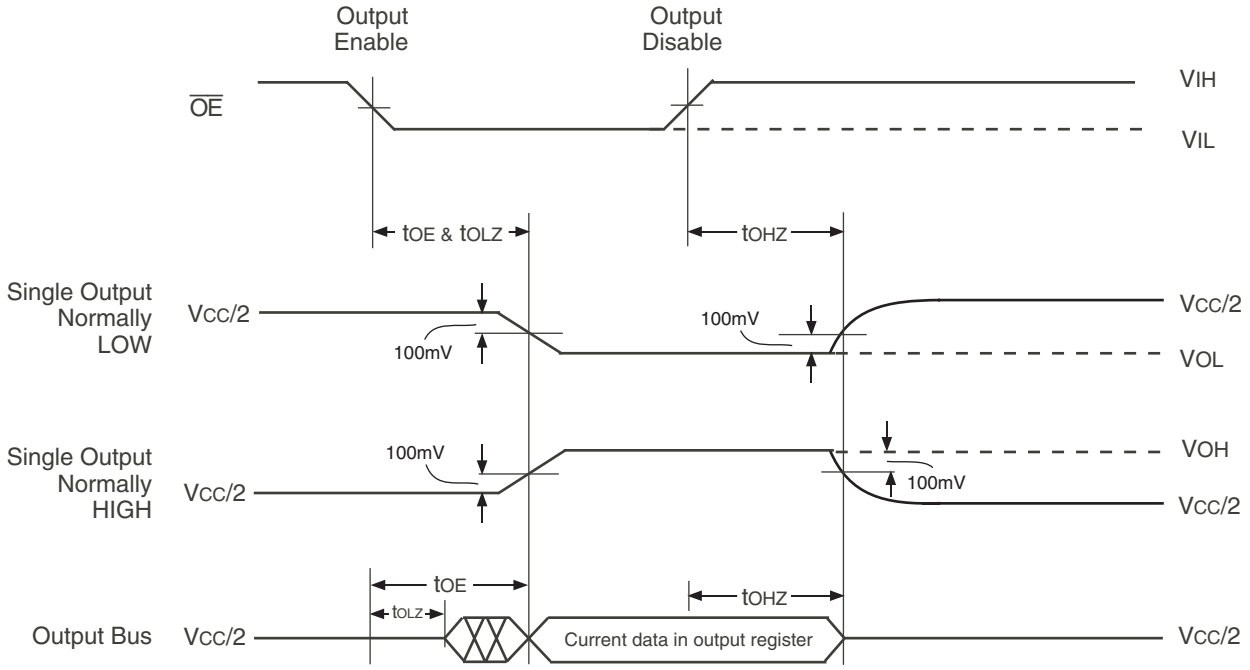
Figure 2b. Lumped Capacitive Load, Typical Derating

LVTTL
2.5V AC TEST CONDITIONS

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	1ns
Input Timing Reference Levels	1.25V
Output Reference Levels	1.25V

NOTE:
1. For LVTTL, V_{CC} = V_{DDQ} = 2.5V.

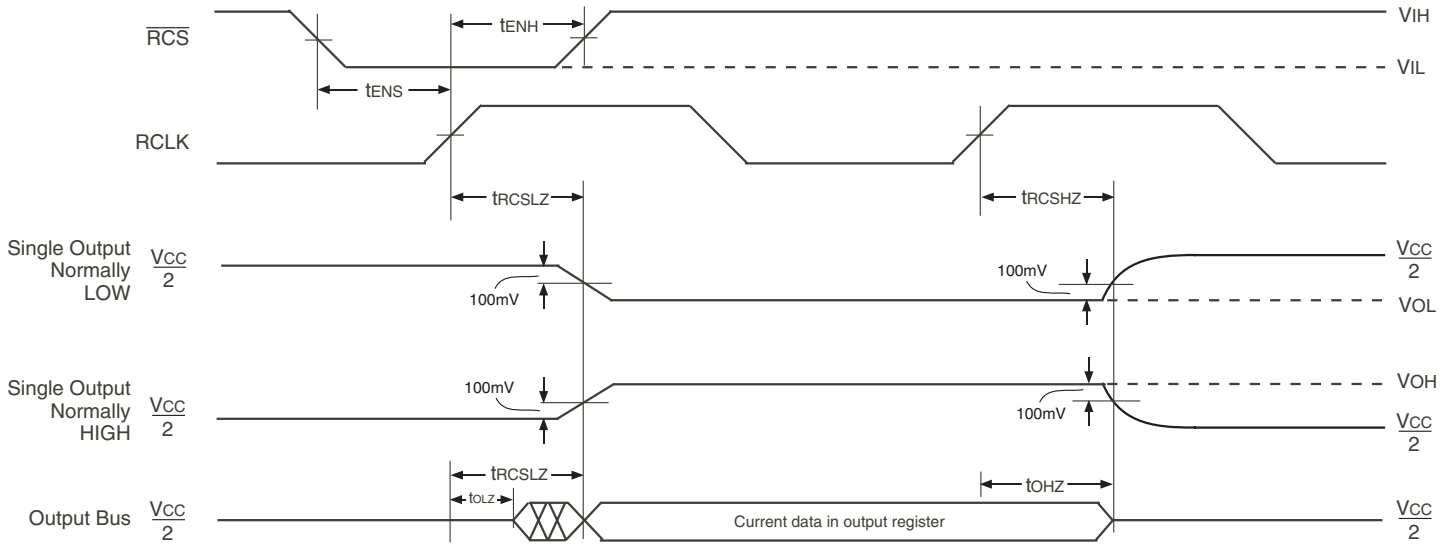
OUTPUT ENABLE & DISABLE TIMING



NOTES:
1. $\overline{REN}$ is HIGH.
2. $\overline{RCS}$ is LOW.

6158 drw05

READ CHIP SELECT ENABLE & DISABLE TIMING



6158 drw06

NOTES:
1. $\overline{REN}$ is HIGH.
2. $\overline{OE}$ is LOW.

FUNCTIONAL DESCRIPTION

MASTER RESET & DEVICE CONFIGURATION

During Master Reset the device configuration and settings are determined, this includes the following:

1. Quad or Dual mode
2. IDT Standard or First Word Fall Through (FWFT) flag timing mode
3. Single or Double Data Rates on both the Write and Read ports
4. Programmable flag mode, synchronous or asynchronous timing
5. Write and Read Port Bus Widths, x10 or x20 (in Dual mode only)
6. Default Offsets for the programmable flags, 7, 63, 127, or 1023
7. LVTTL or HSTL I/O selection

The state of the configuration inputs during master reset will determine which of the above modes are selected. A master reset comprises of pulsing the $\overline{MRS}$ input pin from high to low for a period of time (t_{RS}) with the configuration inputs held in their respective states. Table 1 summarizes the configuration modes available during master reset. They are described as follows:

Quad or Dual mode. This mode is selected using the MD input. If during master reset, MD is HIGH then Quad mode is selected, if MD is LOW then Dual mode is selected. In Quad mode four independent FIFOs are available, while in Dual mode two independent FIFOs are available.

IDT Standard or FWFT mode. The two available flag timing modes are selected using the FWFT/SI input. If FWFT/SI is LOW during master reset then IDT Standard mode is selected, if it is high then FWFT mode is selected. The timing modes are described later in this section.

Single Data Rate (SDR) or Double Data Rate (DDR). The input/output data rates are port selectable. This is a versatile feature that allows the user to select either SDR or DDR on the write ports and/or read ports of all FIFOs using the WDDR and RDDR inputs. If WDDR is LOW during master reset then the write ports of all FIFOs will function in SDR mode; if it is high then the write ports will be DDR mode. If RDDR is LOW during master reset then the read ports of all FIFOs will function in SDR mode; if it is high then the read port will be DDR mode. This feature is described in the Signal Descriptions section.

Programmable Almost Empty/Full Flags. These flags can operate in either synchronous or asynchronous timing mode. If the programmable flag input, PFM is HIGH during master reset then all programmable flags will operate in a synchronous manner, meaning the $\overline{PAE}$ flags are double buffered and updated based on the rising edge of its respective read clocks. The $\overline{PAF}$ flags are also double buffered and updated based on the rising edge of its respective write clocks. If it is LOW then all programmable flags will operate in an asynchronous manner, meaning the $\overline{PAE}$ and $\overline{PAF}$ flags are not double buffered and will update through the internal counter after a nominal delay. This feature is described in the Signal Descriptions section.

Selectable Bus Width. In Dual mode, the bus width can be selected on the read and write ports using the IW and OW inputs. If IW is LOW then the write ports will be 10 bits wide, if IW is HIGH then the write ports will be 20 bits wide. If OW is LOW then the read ports will be 10 bits wide, if OW is HIGH then the read ports will be 20 bits wide. Note in Quad mode the inputs and outputs are always 10 bits wide regardless of the state of these pins. This feature is described in the Signal Descriptions section.

Programmable Flag Offset Values. These offset values can be user programmed or they can be set to one of four default values during a master reset. For default programming, the state of the FSEL[1:0] inputs during master reset will determine the value. Table 2, Default Programmable offsets lists the four offset values and how to select them. For programming the offset values to a specific number, use the serial programming signals (SCLK, $\overline{SWEN}$, $\overline{SREN}$, FWFT/SI) to load the value into the offset register. You may also use the JTAG port on this device to load the offset value. Keep in mind that you must disable the serial programming signals if you plan to use the JTAG port for loading the offset values. To disable the serial programming signals, tie SCLK, $\overline{SWEN}$, $\overline{SREN}$, and FWFT/SI to V_{CC}. A thorough explanation of the serial and JTAG programming of the flag offset values is provided in the "Serial Write and Reading of Offset Registers" section.

I/O Level Selection. The I/Os can be selected for either 2.5V LVTTL levels or 1.5V HSTL / 1.8V eHSTL levels. The state of the IOSEL input will determine which I/O level will be selected. If IOSEL is HIGH then the applicable I/Os will be 1.5V HSTL or 1.8V eHSTL, depending on the voltage level applied to V_{DDQ} and V_{REF}. For HSTL, VDDQ and V_{REF} = 1.5V and for eHSTL VDDQ and V_{REF} = 1.8V. If IOSEL is LOW then the applicable I/Os will be 2.5V LVTTL. As noted in the Pin Description section, IOSEL is a CMOS input and must be tied to either V_{CC} or GND for proper operation.

TABLE 1 — DEVICE CONFIGURATION

PINS	VALUES	CONFIGURATION
MD	0 1	Dual mode Quad mode
FWFT/SI	0 1	IDT Standard mode FWFT mode
WDDR	0 1	Single Data Rate write port Double Data Rate write port
RDDR	0 1	Single Data Rate read port Double Data Rate read port
PFM	0 1	Asynchronous operation of $\overline{PAE}$ and $\overline{PAF}$ outputs Synchronous operation of $\overline{PAE}$ and $\overline{PAF}$ outputs
IW	0 1	Write port is 10 bits wide Write port is 20 bits wide in dual mode, 10 bits wider in Dual mode
OW	0 1	Read port is 10 bits wide Read port is 20 bits wide in dual mode, 10 bits wider in Dual mode
FSEL[1:0]	00 01 10 11	Programmable flag registers offset value = 7 Programmable flag registers offset value = 63 Programmable flag registers offset value = 127 Programmable flag registers offset value = 1023
IOSEL	0 1	All applicable I/Os (except CMOS) are LVTTL All applicable I/Os (except CMOS) are HSTL/eHSTL

TABLE 2 — DEFAULT PROGRAMMABLE FLAG OFFSETS

IDT72T54242
IDT72T54252
IDT72T54262

FSEL1	FSEL0	Offsets n,m
0	0	7
0	1	63
1	0	127
1	1	1023

NOTES:
1. In default programming, the offset value selected applies to all internal FIFOs.
2. To program different offset values for each FIFO, serial programming must be used.
3. n is the offset value for $\overline{PAE}$, m is the offset value for $\overline{PAF}$.

SERIAL WRITING AND READING OF OFFSET REGISTERS

The offset registers can be loaded with a default value or they can be user programmed with a specific value. One of four default values are loaded based on the state of the FSEL[1:0] inputs. The flag offset values can be programmed either through the dedicated serial programming port or the JTAG port. The dedicated serial port can be used to load or read the contents of the offset registers. The offset registers are programmed and read sequentially through a series of shift registers. Each bit in the serial input will shift through the offset registers and program each FIFOs offset registers.

The serial read and write operations are performed by the dedicated SCLK, FWFT/SI, $\overline{SWEN}$, $\overline{SREN}$ and SDO pins. The total number of bits required per device are listed in Figure 3, *Programmable Flag Offset Programming Methods*. These bits account for all four $\overline{PAE}$/$\overline{PAF}$ offset registers in the device. To write to the offset registers, set the serial write enable signal active (LOW), and on each rising edge of SCLK one bit from the FWFT/SI pin is serially shifted into the flag offset register chain. Once the complete number of bits has been programmed into all four registers, the programming sequence is complete. The programming sequence is listed in Figure 3. To read the values from the offset registers, set the serial read enable active (LOW). Then on each rising edge of SCLK, one bit is shifted out to the serial data output. The serial read enable must be kept LOW throughout the entire read operation. To stop reading the offset register, disable the serial read enable (HIGH). There is a setup time for reading the offset registers, as the offset register data for each FIFO is temporarily stored in a scan chain. When data has been completely read out of the offset registers, any additional read operations to the offset register will result in zeros as the output data.

Reading and writing the offset registers can also be accomplished using the JTAG port. To write to the offset registers using JTAG, set the instructional register to the offset write command (Hex Value = 0x0008). The JTAG port will load data into each of the offset registers in a similar fashion as the serial programming described above. To read the values from the offset registers, set the instructional register to the offset read command (Hex Value = 0x0007). The TDO of the JTAG port will output data in a similar fashion as the serial programming described above.

The number of bits required to load the offset registers is dependent on the size of the device selected and the width of the I/Os selected. Each offset register requires 15 bits, 16 bits or 17 bits for the IDT72T54242/72T54252/72T54262 devices respectively. So a total of 120 bits, 128 bits or 136 bits will need to be loaded into each offset register chain for the IDT72T54242/72T54252/72T54262 devices respectively. If Dual mode is selected, only two of the four offset register will need to be programmed ($\overline{PAE}$/$\overline{PAF}$2, $\overline{PAE}$/$\overline{PAF}$0). Therefore, the total number of bits required will be half of its Quad mode operation. See Figure 4, *Offset Register Serial Bit Sequence* for a mapping of the serial bits to each offset registers.

JTAG Programming Instruction Code	Serial Programming		IDT Part Number	Quad Mode	Dual Mode[4] (IW/OW = x10)	Dual Mode (IW/OW = x20)
	$\overline{SWEN}$	$\overline{SREN}$				
0008 (Hex)	0	1	IDT72T54242 IDT72T54252 IDT72T54262	120 128 136	60 64 68	56 60 64
0007 (Hex)	1	0	IDT72T54242 IDT72T54252 IDT72T54262	120 128 136	60 64 68	56 60 64

6158 drw07

PROGRAMMING INSTRUCTIONS:

JTAG Programming

1. Load JTAG Instruction code in "JTAG Timing Specifications" section.
2. Use rising edge of TCK to clock in the required bits from the TD2 input or to clock out from the TDO output pin.

Serial Programming

1. Set $\overline{SWEN}$ and $\overline{SREN}$ as shown above.
2. If reading, $\overline{SREN}$ LOW will clock data out of the SDO pin on every rising TCK edge. If writing, $\overline{SWEN}$ LOW will clock in data from the FWFT/SI pin.

NOTES:

1. The programming methods apply to both IDT Standard mode and FWFT mode.
2. The number of bits indicated are for all four $\overline{PAE}$/$\overline{PAF}$ offset registers.
3. $\overline{SWEN}$ = 0, and $\overline{SREN}$ = 0 simultaneously are not allowed.
4. In Dual mode (IW/OW = x10), the total number of bits required will be half since only two FIFOs are active.
5. Parallel programming is not available.

Figure 3. Programmable Flag Offset Programming Methods

TIMING MODES: IDT STANDARD vs FIRST WORD FALL THROUGH (FWFT) MODE

The IDT72T54242/72T54252/72T54262 support two different timing modes of operation: IDT Standard mode and First Word Fall Through (FWFT) mode. The selection of which mode will be used is determined during master reset, by the state of the FWFT input.

During master reset, if the FWFT pin is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or not there are any words present in the FIFO. It also uses the Full Flag ($\overline{FF}$) to indicate whether or not the FIFO has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable ($\overline{REN}$), Read Chip Select ($\overline{RCS}$), and RCLK.

If the FWFT pin is HIGH during master reset, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data at the data outputs. It also uses Input Ready ($\overline{IR}$) to indicate whether or not the FIFO has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to output bus after three RCLK rising edges. Applying $\overline{REN}$ = LOW is not necessary, although having $\overline{RCS}$ = 0 at the previous rising RCLK is necessary to keep the output from being in high-impedance. However, subsequent words must be accessed using Read Enable ($\overline{REN}$), Read Chip Select ($\overline{RCS}$), and RCLK. Various signals in both inputs and outputs operate differently depending on which timing mode is in effect. The timing mode selected affects all internal FIFOs and are not programmed individually.

IDT STANDARD MODE

In this mode, the status flags $\overline{FF}$, $\overline{PAF}$, $\overline{PAE}$, and $\overline{EF}$ operate in the manner outlined in Table 3, *Status Flags for IDT Standard Mode*. To write data into the FIFO, Write Enable ($\overline{WEN}$), and Write Chip Select ($\overline{WCS}$) must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of the Write Clock (WCLK). After the first write is performed, the Empty Flag ($\overline{EF}$) will go HIGH. Subsequent writes will continue to fill up the FIFO. The Programmable Almost-Empty flag ($\overline{PAE}$) will go HIGH after n + 1 words have been loaded into the FIFO, where "n" is the empty offset value. The default settings for these values are listed in Table 2. This parameter is also user programmable as described in the Serial Writing and Reading of Offset Registers section.

Continuing to write data into the FIFO without performing read operations will cause the Programmable Almost-Full flag ($\overline{PAF}$) to go LOW. Again, if no reads are performed, the $\overline{PAF}$ will go LOW after (32,768-m) writes for the IDT72T54242, (65,536-m) writes for the IDT72T54252, and (131,072-m) writes for the IDT72T54262. In x20 dual mode, $\overline{PAF}$ will go LOW after (16,384-m) writes for the IDT72T54242, (32,768-m) writes for the IDT72T54252, and (65,536-m) writes for the IDT72T54262. The offset "m" is the full offset value. The default setting for these values are listed in Table 3, *Status Flags for IDT Standard Mode*. This parameter is also user programmable. See the section on Serial Writing and Reading of Offset Registers for details.

When the FIFO is full, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{FF}$ will go LOW after D writes to the FIFO, where D = 32,768 writes for the IDT72T54242, 65,536 writes for the IDT72T54252, and 131,072 writes for the IDT72T54262. In x20 dual mode, $\overline{FF}$ will go LOW after 16,384 writes for the IDT72T54242, 32,768 writes for the IDT72T54252, and 65,536 writes for the IDT72T54262.

If the FIFO is full, the first read operation will cause $\overline{FF}$ to go HIGH. Subsequent read operations will cause $\overline{PAF}$ to go HIGH at the conditions described in Table 3, *Status Flags for IDT Standard Mode*. If further read operations occur without write operations, $\overline{PAE}$ will go LOW when there are n words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, the $\overline{EF}$ will go LOW inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty, but $\overline{RCS}$ will continue to determine whether or not the output is in high-impedance.

When configured in IDT Standard mode, the $\overline{EF}$ and $\overline{FF}$ outputs are double register-buffered outputs. IDT Standard mode is available when the device is configured in either Single Data Rate or Double Data Rate mode. Relevant timing diagrams for IDT Standard mode can be found in Figure 10, 11, 12, 13, 14, 15, 16, 17, 18 and 23.

	IDT72T54242 Quad mode	IDT72T54252 Quad mode	IDT72T54262 Quad mode	IDT72T54242 Dual mode IW/OW = x20	IDT72T54242 Dual mode IW/OW = x10 or IDT72T54252 IW/OW = x20	IDT72T54252 Dual mode IW/OW = x10 or IDT72T54262 IW/OW = x20	IDT72T54262 Dual mode IW/OW = x10	Offset Register
Serial Bits	1 - 15	1 - 16	1 - 17	—	—	—	—	$\overline{PAE}3$ (1)
	16 - 30	17 - 32	18 - 34	—	—	—	—	$\overline{PAF}3$ (1)
	31 - 45	33 - 48	35 - 51	1 - 14	1 - 15	1 - 16	1 - 17	$\overline{PAE}2$
	46 - 60	49 - 64	52 - 68	15 - 28	16 - 30	17 - 32	18 - 34	$\overline{PAF}2$
	61 - 75	65 - 80	69 - 85	—	—	—	—	$\overline{PAE}1$ (1)
	76 - 90	81 - 96	86 - 102	—	—	—	—	$\overline{PAF}1$ (1)
	91 - 105	97 - 112	103 - 119	29 - 42	31 - 45	33 - 48	35 - 51	$\overline{PAE}0$
	106 - 120	113 - 128	120 - 136	43 - 56	46 - 60	49 - 64	52 - 68	$\overline{PAF}0$

6158 drw08

NOTES:
1. These registers are not used in Dual mode. They are not programmed or read in the serial chain.
2. In all modes, the higher numbered bit is the MSB. For example, in the IDT72T54242 in Quad mode, the first bit is the LSB for $\overline{PAE}3$.

Figure 4. Offset Registers Serial Bit Sequence

FIRST WORD FALL THROUGH MODE (FWFT)

In this mode, the status flags $\overline{OR}$, $\overline{IR}$, $\overline{PAE}$, and $\overline{PAF}$ operate in the manner outlined in Table 4, *Status Flags for FWFT Mode*. To write data into to the FIFO, $\overline{WEN}$, and $\overline{WCS}$ must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of WCLK. After the first write is performed, the Output Ready ($\overline{OR}$) flag will go LOW. Subsequent writes will continue to fill up the FIFO. $\overline{PAE}$ will go HIGH after n + 2 words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are listed in Table 4, *Status Flags for FWFT Mode*. This parameter is also user programmable as described in the Serial Writing and Reading of Offset Registers section.

Continuing to write data into the FIFO without performing read operations will cause the Programmable Almost-Full flag ($\overline{PAF}$) to go LOW. Again, if no reads are performed, the $\overline{PAF}$ will go LOW after (32,769-m) writes for the IDT72T54242, (65,537-m) writes for the IDT72T54252, and (131,073-m) writes for the IDT72T54262. In x20 dual mode, $\overline{PAF}$ will go LOW after (16,385-m) writes for the IDT72T54242, (32,769-m) writes for the IDT72T54252, and (65,537-m) writes for the IDT72T54262. The offset "m" is the full offset value. The default setting for these values are listed in Table 4, *Status Flags for FWFT Mode*. This parameter is also user programmable. See the section on serial writing and reading of offset registers for details.

When the FIFO is full, the Input Ready ($\overline{IR}$) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{IR}$ will go LOW after D writes to the FIFO, where D = 32,769 writes for the IDT72T54242, 65,537 writes for the IDT72T54252, and 131,073 writes for the IDT72T54262. In x20 dual mode, $\overline{FF}$ will go LOW after 16,385 writes for the IDT72T54242, 32,769 writes for the IDT72T54252, and 65,537 writes for the IDT72T54262.

If the FIFO is full, the first read operation will cause $\overline{IR}$ to go HIGH. Subsequent read operations will cause $\overline{PAF}$ to go HIGH at the conditions described in Table 4, *Status Flags for FWFT Mode*. If further read operations occur without write operations, $\overline{PAE}$ will go LOW when there are n words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, the $\overline{OR}$ will go HIGH inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty, but $\overline{RCS}$ will continue to determine whether or not the output is in high-impedance.

When configured in FWFT mode, the $\overline{OR}$ flag output is triple register-buffered and the $\overline{IR}$ flag output is double register-buffered. Relevant timing diagrams for FWFT mode can be found in Figure 19, 20, 21, 22 and 24.

TABLE 3 — STATUS FLAGS FOR IDT STANDARD MODE

Number of Words in FIFO	IDT72T54242 Dual mode IW/OW = x20	IDT72T54242 Quad mode or Dual mode IW/OW = x10 or IDT72T54252 Dual mode IW/OW = x20	IDT72T54252 Quad mode or Dual mode IW/OW = x10 or IDT72T54262 Dual mode IW/OW = x20	IDT72T54262 Quad mode or Dual mode IW/OW = x10	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	0	0	H	H	L	L
1 to n	1 to n	1 to n	1 to n	1 to n	H	H	L	H
16,384 - (m) to 16,383	32,768 - (m) to 32,767	65,536 - (m) to 65,535	131,072 - (m) to 131,071	H	L	H	H
16,384	32,768	65,536	131,072	L	L	H	H

NOTE:
1. See Table 2 for values for n, m. Values n,m may be different for each FIFO.

TABLE 4 — STATUS FLAGS FOR FWFT MODE

Number of Words in FIFO	IDT72T54242 Dual mode IW/OW = x20	IDT72T54242 Quad mode or Dual mode IW/OW = x10 or IDT72T54252 Dual mode IW/OW = x20	IDT72T54252 Quad mode or Dual mode IW/OW = x10 or IDT72T54262 Dual mode IW/OW = x20	IDT72T54262 Quad mode or Dual mode IW/OW = x10	$\overline{IR}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{OR}$
0	0	0	0	L	H	L	H
1 to n+1	1 to n+1	1 to n+1	1 to n+1	L	H	L	L
16,385 - (m) to 16,384	32,769 - (m) to 32,768	65,537 - (m) to 65,536	131,073 - (m) to 131,072	L	L	H	L
16,385	32,769	65,537	131,073	H	L	H	L

6158 drw09

NOTE:
1. See Table 2 for values for n, m. Values n,m may be different for each FIFO.

SELECTABLE MODES

This device is capable of operating in two different modes: Quad mode or Dual mode. In the Quad mode there are four independent FIFOs available, with the input and output bus widths set to 10 bits wide for each FIFO. A total of eight independent clock inputs are available– four RCLKs and four WCLKs. Each FIFO has independent read and write controls, output enable controls, as well as individual status flags $\overline{EF}/\overline{OR}$, $\overline{FF}/\overline{IR}$, $\overline{PAE}$, and $\overline{PAF}$. Also available are echo outputs ERCLK and $\overline{EREN}$ for each individual FIFO to aid high-speed operation where synchronizing data is critical.

In the Dual mode there are two independent FIFOs available, with the input and output bus widths each selectable between x10 or x20. Bus-matching is available in this mode, allowing for more flexibility. A total of four independent clock inputs are available, two RCLKs and two WCLKs. Each FIFO has independent read and write controls– output enable controls, as well as individual status flags $\overline{EF}/\overline{OR}$, $\overline{FF}/\overline{IR}$, $\overline{PAE}$, and $\overline{PAF}$. Also available are echo outputs ERCLK and $\overline{EREN}$ for each individual FIFO to aid high-speed operation where synchronizing data is critical.

HSTL/LVTTL I/O

The inputs and outputs of this device can be configured for either LVTTL or HSTL/eHSTL operation. If the IOSEL pin is HIGH during master reset, then all applicable LVTTL or HSTL signals will be configured for HSTL/eHSTL operating voltage levels. To select between HSTL or eHSTL V_{REF} must be driven to 1.5V or 1.8V respectively. Typically a logic HIGH in HSTL would be V_{REF} + 0.2V and a logic LOW would be V_{REF} – 0.2V.

If the IOSEL pin is LOW during master reset, then all applicable LVTTL or HSTL signals will be configured for LVTTL operating voltage levels. In this configuration V_{REF} must be set to GND. Table 5 illustrates which pins are and are not associated with this feature. Note that all "Static Pins" must be tied to V_{CC} or GND. These pins are LVTTL only and are purely device configuration pins. Note the IOSEL pin should be tied HIGH or LOW and cannot toggle before and after master reset.

BUS MATCHING

In the Dual mode operation, the write and read port have bus-matching capability such that the input and output busses can each be either 10 bits or 20 bits wide. The bus width of both the input and output port is determined during master reset using the input (IW) and output (OW) widths setup pins. The selected port width is applied to both FIFO ports, such that both FIFOs will be configured for either x10 or x20 bus widths. When writing or reading data from a FIFO the number of memory locations available to be read will depend on the bus width selected and the density of the device.

If the write/read ports are 10 bits wide, this provides the user with a FIFO depth of 32,768 x 10 for the IDT72T54242, 65,536 x 10 for the IDT72T54252, or 131,072 x 10 for the IDT72T54262. If the write/read ports are 20 bits wide, this provides the user with a FIFO depth of 16,384 x 20 for the IDT72T54242, 32,768 x 20 for the IDT72T54252, or 65,536 x 20 for the IDT72T54262. The FIFO depths will always have a fixed density of 327,680 bits for the IDT72T54242, 655,360 bits for the IDT72T54252 and 1,310,072 bits for the IDT72T54262 regardless of bus-width configuration on the write/read port. When the device is operating in double data rate, the word is twice as large as in single data rate since one word consists of both the rising and falling edge of clock. Therefore in DDR, the FIFO depths will be half of what it is mentioned above. For instance, if the write/read port is 10 bits wide, the depth of each FIFO is 16,384 x 10 for the IDT72T54242, 32,768 x 10 for the IDT72T54252, or 65,536 x 10 for the IDT72T54262. See Figure 5, *Bus-Matching in Dual mode* for more information.

TABLE 5 — I/O VOLTAGE LEVEL ASSOCIATIONS

LVTTL/HSTL/eHSTL SELECT					STATIC CMOS SIGNALS
Write Port	**Read Port**	**JTAG**	**Signal Pins**	**Serial Clock Port**	**Static Pins**
D[39:0]	Q[39:0]	TCK	FSEL[1:0]	SCLK	IOSEL
WCLK0/1/2/3	RCLK0/1/2/3	$\overline{TRST}$	$\overline{PD}$	$\overline{SREN}$	IW
$\overline{WEN}$0/1/2/3	$\overline{REN}$0/1/2/3	TMS	$\overline{MRS}$	$\overline{SWEN}$	OW
$\overline{WCS}$0/1/2/3	$\overline{RCS}$0/1/2/3	TDI	$\overline{PRS}$0/1/2/3	FWFT/SI	MD
$\overline{FF}/\overline{IR}$0/1/2/3	$\overline{EF}/\overline{OR}$0/1/2/3	TDO	FWFT/SI	SDO	PFM
$\overline{PAF}$0/1/2/3	$\overline{OE}$0/1/2/3				RDDR
	$\overline{PAE}$0/1/2/3				WDDR
	ERCLK0/1/2/3				
	$\overline{EREN}$0/1/2/3				

NOTE:
1. In Dual mode, not all available signals will be used. Signals with a designation of 1 and 3 are not used.

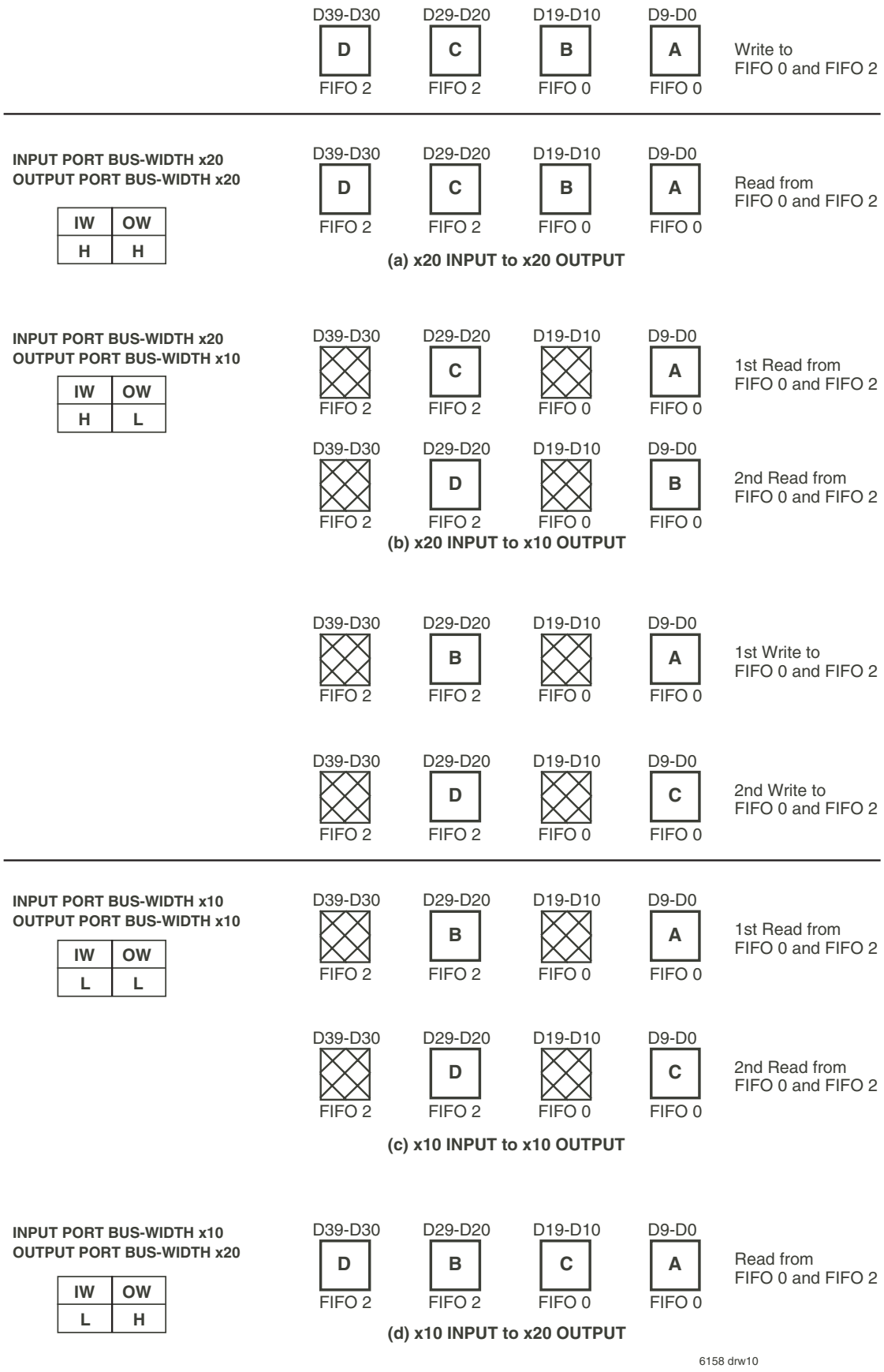


Figure 5. Bus-Matching in Dual mode

SIGNAL DESCRIPTIONS

INPUTS:

DATA INPUT BUS (D[39:0])

The data input busses are 10 bits wide in Quad mode and 20 or 10-bits wide in Dual mode. In Quad mode, D[9:0] are data inputs for FIFO0, D[19:10] are for FIFO1, D[29:20] are for FIFO2, and D[39:30] are for FIFO3. In Dual mode, D[19:0] are data inputs for FIFO0 and D[39:20] are for FIFO2 for the 20-bit wide data bus. D[9:0] are data inputs for FIFO0 and D[29:20] are data inputs for FIFO2 for the 10-bit wide data bus.

MASTER RESET ($\overline{MRS}$)

There is a single master reset available for all internal FIFOs in this device. A master reset is initiated whenever the $\overline{MRS}$ input is taken to a LOW state. This operation sets the internal read and write pointers of all FIFOs to the first location in memory. The programmable almost empty flag will go LOW and the almost full flags will go HIGH.

If FWFT/SI signal is LOW during master reset then IDT Standard mode is selected. This mode utilizes the empty and full status flags from the $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$ dual-purpose pin. During master reset, all empty flags will be set to LOW and all full flags will be set to HIGH.

If FWFT/SI signal is HIGH during master reset, then the First Word Fall Through mode is selected. This mode utilizes the input read and output ready status flags from the $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$ dual-purpose pin. During master reset, all input ready flags will be set to LOW and all output ready flags will be set to HIGH.

All device configuration pins such as MD, OW, IW, WDDR, RDDR, IOSEL, PFM, FSEL[1:0] and FWFT/SI need to be defined before the master reset cycle. During a master reset the output registers are initialized to all zeros. If the output enables are LOW during master reset, then the output bus will be LOW. If the output enable(s) are HIGH during master reset, then the output bus will be in high-impedance. $\overline{RCS}$ has no affect on the data outputs during master reset. If the output width OW is configured to x10 in Dual mode, then the unused outputs Q[19:10] and Q[39:30] will be in high-impedance. A master reset is required after power up before a write operation to any FIFO can take place. Master reset is an asynchronous signal and thus the read and write clocks can be free-running or idle during master reset. See Figure 10, *Master Reset Timing*, for the associated timing diagram.

PARTIAL RESET ($\overline{PRS}$0/1/2/3)

A partial reset is a means by which the user can reset both the read and write pointers of each individual FIFO inside the device without changing the FIFO's configuration. There are four dedicated partial reset signals (two in Dual mode) that each correspond to an individual FIFO. There are no restrictions as to when partial reset can be performed in either operating modes.

During partial reset, the internal read and write pointers are set to the first location in memory, $\overline{PAE}$ goes LOW and $\overline{PAF}$ goes HIGH. Whichever timing mode was active at the time of Partial Reset will remain active after Partial Reset. If IDT Standard Mode is active, then $\overline{FF}$ will go HIGH and $\overline{EF}$ will go LOW. If the First Word Fall Through mode is active, then $\overline{OR}$ will go HIGH and $\overline{IR}$ will go LOW.

Following Partial Reset, all values held in the offset registers remain unchanged. The output registers are initialized to all zeros. All other configurations set up during master reset remain unchanged. $\overline{PRS}$ is an asynchronous signal. See Figure 11, *Partial Reset Timing*, for the associated timing diagram.

FIRST WORD FALL THROUGH/SERIAL IN (FWFT/SI)

This is a dual purpose pin. During master reset, the state of the FWFT/SI input determines whether the device will operate in IDT Standard mode or First Word Fall Through (FWFT) mode.

If FWFT/SI is LOW before the falling edge of master reset, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or not there are any words present in the FIFOs' memory. It also uses the Full Flag ($\overline{FF}$) to indicate whether or not the FIFOs' memory has any free space for writing. In IDT Standard mode, every word read from the FIFOs, including the first, must be requested using the Read Enable ($\overline{REN}$), Read Chip Select ($\overline{RCS}$) and RCLK.

If FWFT/SI is HIGH before the falling edge of master reset, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data in the output register. It also uses Input Ready ($\overline{IR}$) to indicate whether or not the FIFO's memory has any free space for writing. In other words, they are the inverse of the empty and full flags. In the FWFT mode, the first word written to an empty FIFO goes directly to data outputs after three RCLK rising edges, provided that the first RCLK meets the t_{SKEW} parameter. There may be a one RCLK cycle delay if t_{SKEW} is not met. $\overline{REN}$ and $\overline{RCS}$ do not need to be enabled. Subsequent words must be accessed using the $\overline{REN}$, $\overline{RCS}$, and RCLK.

The state of the FWFT/SI input must be kept at the present state for the minimum of the reset recovery time (t_{RSR}) after master reset. After this time, the FWFT/SI acts as a serial input for loading $\overline{PAE}$ and $\overline{PAF}$ offsets into the programmable offset registers. The serial input is used in conjunction with SCLK, $\overline{SWEN}$, $\overline{SREN}$, and SDO to access the offset registers. Serial programming using the FWFT/SI pin functions the same way in both IDT Standard and FWFT modes.

WRITE CLOCK (WCLK0/1/2/3)

There are a possible total of four write clocks (or two in Dual mode) available in this device depending on the mode selected, each corresponding to the individual FIFOs in memory. A write can be initiated on the rising (or falling) edge of the WCLK input. If the write double data rate (WDDR) mode pin is tied HIGH, data will be written on both the rising and falling edge of WCLK0/1/2/3, provided that $\overline{WEN}$0/1/2/3 and $\overline{WCS}$0/1/2/3 are enabled on the rising edge of WCLK 0/1/2/3. If WDDR is tied LOW, data will be written only on the rising edge of WCLK0/1/2/3 provided that $\overline{WEN}$0/1/2/3 and $\overline{WCS}$ 0/1/2/3 are enabled. Each write clock is completely independent from the others.

Data setup and hold times must be met with respect to the LOW-to-HIGH (and HIGH-to-LOW in DDR) transition of the write clock. It is permissible to stop the write clocks, for asynchronous operations. Note that while the write clocks are idle, the $\overline{FF}$0/1/2/3 and $\overline{PAF}$0/1/2/3 flags will not be updated unless the port is operating in asynchronous timing mode (PFM=0). The write clocks can be independent or coincident with one another. In Dual mode, the unused clocks (WCLK1 and WCLK3) should be tied to GND.

WRITE ENABLE ($\overline{WEN}$0/1/2/3)

There are a total of four write enables (or two in Dual mode) available in this device depending on the mode selected, one for each individual FIFO. When the write enable input is LOW on the rising edge of WCLK in single data rate mode, data is loaded on the rising edge of every WCLK cycle, provided the device is not full and the write chip select ($\overline{WCS}$) is enabled. The setup and hold times are referenced with respect to the rising edge of WCLK only. When the write enable input is LOW on the rising edge of WCLK in double data rate, data is loaded into any of the FIFOs on the rising and falling edge of every WCLK cycle, provided the device is not full and the write chip select ($\overline{WCS}$) is enabled on the

rising edge of WCLK. In this mode, the data setup and hold times are referenced with respect to the rising and falling edge of WCLK. Note that $\overline{WEN}$ and $\overline{WCS}$ are sampled only on the rising edge of WCLK in either data rates.

Data is stored in the FIFOs' memory sequentially and independently of any ongoing read operation. When the write enables or write chip selects are HIGH, no new data is written into the corresponding FIFO on each WCLK cycle. Each write enable operates independently of the others. In Dual mode, the unused write enables ($\overline{WEN}$1 and $\overline{WEN}$3) should be tied to VCC.

WRITE CHIP SELECT ($\overline{WCS}$0/1/2/3)

There are a total of four write chip selects (or two in Dual mode) available in this device depending on the mode selected, one for each individual FIFO. The write chip selects disables all data bus inputs if it is held HIGH. To perform normal write operations, the write chip select must be enabled, (held LOW). The four write chip selects are completely independent of one another. When the write chip select is LOW on the rising edge of WCLK in single data rate mode, data is loaded on the rising edge of every WCLK cycle, provided the device is not full and the write enable ($\overline{WEN}$) of the corresponding FIFO is LOW.

When the write chip select is LOW on the rising edge of WCLK in double data rate mode, data is loaded into any of the FIFOs on the rising and falling edge of every WCLK cycle, provided the device is not full and the write enable ($\overline{WEN}$) of the corresponding FIFO is LOW on the rising clock edge.

When the write chip select is HIGH on the rising edge of WCLK in single data rate mode, the write port is disabled and no words are written into the FIFO memory, on the rising edge of WCLK, even if $\overline{WEN}$ is LOW. If the write chip select is HIGH on the rising edge of WCLK in double data rate mode, the write port is disabled and no words are written into the FIFO memory on the rising or falling edge of WCLK, even if $\overline{WEN}$ is LOW. Note that $\overline{WCS}$ is sampled on the rising edge of WCLK only in either data rate. In Dual mode, the unused write chip selects ($\overline{WCS}$1 and $\overline{WCS}$3) should be tied to VCC.

WRITE DOUBLE DATA RATE (WDDR)

When the write double data rate (WDDR) pin is HIGH, the write port will be set to double data rate mode. In this mode, all write operations are based on the rising and falling edge of the write clocks, provided that write enables and write chip selects are LOW for the rising clock edges. In double data rate the write enable signals are sampled with respect to the rising edge of write clock only, and a word will be written to both the rising and falling edge of write clock regardless of whether or not write enable is active on the falling edge of write clock.

When WDDR is LOW, the write port will be set to single data rate mode. In this mode, all write operations are based on only the rising edge of the write clocks, provided that write enables and write chip selects are LOW during the rising edge of write clock. This pin should be tied HIGH or LOW and cannot toggle.

READ CLOCK (RCLK0/1/2/3)

There are a total of four read clocks (or two in Dual mode) available in this device depending on the mode selected, each corresponding to the individual FIFOs in memory. A read can be initiated on the rising (or falling) edge of the RCLK input. If the read double data rate (RDDR) mode pin is tied HIGH, data will be read on both the rising and falling edge of RCLK0/1/2/3, provided that $\overline{REN}$0/1/2/3 and $\overline{RCS}$0/1/2/3 are enabled on the rising edge of RCLK0/1/2/3. If RDDR is tied LOW, data will be read only on the rising edge of RCLK0/1/2/3 provided that $\overline{REN}$0/1/2/3 and $\overline{RCS}$0/1/2/3 are enabled. Each read clock is completely independent from the others.

There is an associated data access time (t_A) for the data to be read out of the FIFOs. It is permissible to stop the read clocks. Note that while the read clocks are idle, the $\overline{EF}$/0/1/2/3 and $\overline{PAE}$0/1/2/3 flags will not be updated unless the part is operating in asynchronous timing mode (PFM=0). The write and read clocks can be independent or coincident. In Dual mode, the unused clocks (RCLK1 and RCLK3) should be tied to GND.

READ ENABLE ($\overline{REN}$0/1/2/3)

There are a total of four read enables (or two in Dual mode) available in this device depending on the mode selected, one for each individual FIFOs. When the read enable input is LOW on the rising edge of RCLK in single data rate mode, data will be read on the rising edge of every RCLK cycle, provided the device is not empty and the read chip select ($\overline{RCS}$) is enabled. The associated data access time (t_A) is referenced with respect to the rising edge of RCLK. When the read enable input is LOW on the rising edge of WCLK in double data rate mode, data will be read on the rising and falling edge of every RCLK cycle, provided the device is not empty and $\overline{RCS}$ is enabled. In this mode, the data access times are referenced with respect to the rising and falling edges of RCLK. Note that $\overline{REN}$, and $\overline{RCS}$ are sampled only on the rising edge of RCLK in either data rate.

Data read from the FIFO's memory sequentially and independently of any ongoing write operation. When the read enables or read chip selects are HIGH, no new data is read on each RCLK cycle. Each read enable operates independently of the others.

To prevent reading from an empty FIFO in the IDT Standard mode, the empty flag of each FIFO will go LOW with respect to RCLK, when the total number of words in the FIFO has been read, thus inhibiting further read operations. Upon the completion of a valid write cycle, the empty flag will go HIGH with respect to RCLK two cycles later, thus allowing another read to occur similarly, for FWFT mode, the output ready flag of each FIFO will go HIGH with respect to RCLK when the total number of words in the FIFO has been read out. In Dual mode, the unused read enables ($\overline{REN}$1 and $\overline{REN}$3) should be tied to VCC.

READ CHIP SELECT ($\overline{RCS}$0/1/2/3)

There are a total of four read chip selects (or two in Dual mode) available in this device, each corresponding to an individual FIFO. The read chip select inputs provide synchronous control of the read port. When the read chip select is held LOW, the next rising edge of the corresponding RCLK will enable the output bus. When the read chip select goes HIGH, the next rising edge of RCLK will send the output bus into high-impedance and prevent that RCLK from initiating a read, regardless of the state of $\overline{REN}$. During a master or partial reset the read chip select input has no effect on the output bus– output enable is the only input that provides high-impedance control of the output bus. If output enable is LOW, the data outputs will be active regardless of read chip select until the first rising edge of RCLK after a reset is complete. Afterwards if read chip select is HIGH the data outputs will go to high-impedance. Each read chip select is completely independent of the others.

The read chip select inputs do not affect the updating of the flags. For example, when the first word is written to any/all empty FIFOs, the empty flags will still go from LOW to HIGH based on a rising edge of the RCLK, regardless of the state of the read chip select inputs. Also, when operating the FIFO in FWFT mode the first word written to any/all empty FIFOs will still be clocked through to the output bus on the third rising edge of RCLK, regardless of the state of read chip select inputs, assuming that the t_{SKEW} parameter is met. For this reason the user should pay extra attention to the read chip selects when a data word is written to any/all empty FIFOs in FWFT mode. If the read chip select inputs are HIGH when an empty FIFO is written into, the first word will fall through to the output register but will not be available on the outputs because they are in high-impedance. The user must enable read chip select on the rising edge of RCLK while disabling $\overline{REN}$ to access this first word. In Dual mode, the unused read

chip selects ($\overline{RCS}$1 and $\overline{RCS}$3) should be tied to VCC. Refer to Figures 23 and 24, *Read Cycle and Read Chip Select* for the associated timing diagrams.

READ DOUBLE DATA RATE (RDDR)

When the read double data rate (RDDR) pin tied HIGH, the read port will be set to double data rate mode. In this mode, all read operations are based on the rising and falling edge of the read clocks, provided that read enables and read chip selects are LOW. In double data rate the read enable signals are sampled with respect to the rising edge of read clock only, and a word will be read from both the rising and falling edge of read clock regardless of whether or not read enable and read chip select are active on the falling edge of read clock.

When RDDR is tied LOW, the read port will be set to single data rate mode. In this mode, all read operations are based on only the rising edge of the read clocks, provided that read enables and read chip selects are LOW during the rising edge of read clock. This pin should be tied HIGH or LOW and cannot toggle before or after master reset.

OUTPUT ENABLE ($\overline{OE}$0/1/2/3)

There are total of four asynchronous output enables (two in Dual mode) available in this device, each corresponding to an individual FIFO in memory. When the output enable inputs are LOW, the output bus of each individual FIFO becomes active and drives the data currently in the output register. When the output enable inputs are HIGH, the output bus of each individual FIFO goes into high-impedance. During master or partial reset the output enable is the only input that can place the output data bus into high-impedance. During reset the read chip select input has no effect on the output data bus. Each output enable input is completely independent from the others. In Dual mode, the unused output enables ($\overline{OE}$1 and $\overline{OE}$3) should be tied to VCC.

I/O SELECT (IOSEL)

The inputs and outputs of this device can be configured for either LVTTL or HSTL/eHSTL operation. If the IOSEL pin is HIGH during master reset, then all applicable LVTTL or HSTL signals will be configured for HSTL/eHSTL operating voltage levels. To select between HSTL or eHSTL VREF must be driven to 1.5V or 1.8V respectively. If the IOSEL pin is LOW during master reset, then all applicable LVTTL or HSTL programmable pins will be configured for LVTTL operating voltage levels. In this configuration VREF should be set to GND. This pin should be tied HIGH or LOW and cannot toggle before or after master reset. Please refer to table 5 for a list of LVTTL/HSTL/eHSTL programmable pins.

POWER DOWN (PD)

This device has a power down feature intended for reducing power consumption for HSTL/eHSTL configured inputs when the device is idle for a long period of time. By entering the power down state certain inputs can be disabled, thereby significantly reducing the power consumption of the part. All $\overline{WEN}$ and $\overline{REN}$ signals must be disabled for a minimum of four WCLK and RCLK cycles before activating the power down signal. The power down signal is asynchronous and needs to be held LOW throughout the desired power down time. During power down, the following conditions for the inputs/outputs signals are:

- All data in FIFO(s) memory are retained.
- All data inputs become inactive.
- All write and read pointers maintain their last value before power down.
- All enables, chip selects, and clock input pins become inactive.
- All data outputs become inactive and enter high-impedance state.
- All flag outputs will maintain their current states before power down.
- All programmable flag offsets maintain their values.
- All echo clocks and enables will become inactive and enter high-impedance state.
- The serial programming and JTAG port will become inactive and enter high-impedance state.
- All setup and configuration CMOS static inputs are not affected, as these pins are tied to a known value and do not toggle during operation.

All internal counters, registers, and flags will remain unchanged and maintain their current state prior to power down. Clock inputs can be continuous and free-running during power down, but will have no affect on the part. However, it is recommended that the clock inputs be low when the power down is active. To exit power down state and resume normal operations, disable the power down signal by bringing it HIGH. There must be a minimum of 1µs waiting period before read and write operations can resume. The device will continue from where it had stopped and no form of reset is required after exiting power down state. The power down feature does not provide any power savings when the inputs are configured for LVTTL operation. However, it will reduce the current for I/Os that are not tied directly to VCC or GND. See Figure 35, *Power Down Operation,* for the associated timing diagram.

SERIAL CLOCK (SCLK)

The serial clock is used to load and read data in the programmable offset registers. Data from the serial input signal (FWFT/SI) can be loaded into the offset registers on the rising edge of SCLK provided that the serial write enable ($\overline{SWEN}$) signal is LOW. Data can be read from the offset registers via the serial data output (SDO) signal on the rising edge of SCLK provided that $\overline{SREN}$ is LOW. The serial clock can operate at a maximum frequency of 10MHz.

SERIAL WRITE ENABLE ($\overline{SWEN}$)

The serial write enable input is an enable used for serial programming of the programmable offset registers. It is used in conjunction with the serial input (FWFT/SI) and serial clock (SCLK) when programming the offset registers. When the serial write enable is LOW, data at the serial input is loaded into the offset register, one bit for each LOW-to-HIGH transition of SCLK. When serial write enable is HIGH, the offset registers retain the previous settings and no offsets are loaded. Serial write enable functions the same way in both Standard IDT and FWFT modes. See Figure 29, *Loading of Programmable Flag Registers,* for the timing diagram.

SERIAL READ ENABLE ($\overline{SREN}$)

The serial read enable input is an enable used for reading the value of the programmable offset registers. It is used in conjunction with the serial data output (SDO) and serial clock (SCLK) when reading the offset registers. When the serial read enable is LOW, data at the serial data output can be read from the offset register, one bit for each LOW-to-HIGH transition of SCLK. When serial read enable is HIGH, the reading of the offset registers will stop. Whenever serial read enable ($\overline{SREN}$) is activated (LOW) values in the offset registers are copied directly into a serial scan out register. $\overline{SREN}$ must be kept LOW in order to read the entire contents of the scan out register. If at any point $\overline{SREN}$ is toggled HIGH, another copy function from the offset register to the serial scan out register will occur the next time $\overline{SREN}$ is enabled (LOW). Serial read enable functions the same way in both IDT Standard and FWFT modes. See Figure 30, *Reading of Programmable Flag Registers,* for the timing diagram.

OUTPUTS:

DATA OUTPUT BUS (Q[39:0])

The data output busses are 10 bits wide in Quad mode and 20 or 10-bits wide in Dual mode. In Quad mode, Q[9:0] are data outputs for FIFO0, Q[19:10] are for FIFO1, Q[29:20] are for FIFO2, and Q[39:30] are for FIFO3. In Dual mode, Q[19:0] are data outputs for FIFO0 and Q[39:20] are for FIFO2 for the 20-bit wide data bus. Q[9:0] are data outputs for FIFO0 and Q[29:20] are data outputs for FIFO2 for the 10-bit wide data bus.

EMPTY/OUTPUT READY FLAG ($\overline{EF}$/0/1/2/3)

There are four empty/output ready flags (two in Dual mode) available in this device, each corresponding to the individual FIFOs in memory. This is a dual-purpose pin whose function is determined based on the state of the FWFT/SI pin during master reset. In the IDT Standard mode, the empty flags are selected. When an individual FIFO is empty, its empty flag will go LOW, inhibiting further read operations from that FIFO. When the empty flag is HIGH, the individual FIFO is not empty and valid read operations can be performed. See Figure 18, *Read Cycle, Output Enable and Empty Flag Timing*, for the relevant timing information. Also see Table 3, *Status Flags for IDT Standard Mode* for the truth table of the empty flags.

In FWFT mode, the output ready flags are selected. Output ready flags ($\overline{OR}$) go LOW at the same time that the first word written to an empty FIFO appears on the outputs, which is a minimum of two read clock cycles provided the RCLK and WCLK meets the t_{SKEW} parameter (See Table 6 - T_{SKEW} Measurement). $\overline{OR}$ stays LOW after the RCLK LOW-to- HIGH transitions that shifts the last word from the FIFO memory to the outputs. $\overline{OR}$ goes HIGH when another read operation is performed, indicating the last word was read. The previous data stays at the outputs, further data reads are inhibited until $\overline{OR}$ goes LOW again and a new word appears on the bus. See Figure 22, *Read Timing and Output Ready Flag* , for the relevant timing information. Also see Table 4, *Status Flags for FWFT Mode* for the truth table of the empty flags. To prevent reading in the FWFT mode, the output ready flag of each FIFO will go HIGH with respect to RCLK, when the total number of words has been read out of the FIFO, thus inhibiting further read operations. Upon the completion of a valid write cycle, the output ready flag will go LOW with respect to RCLK three cycles later, thus indicating another read has occurred.

The empty/output ready flags are synchronous and updated on the rising edge of RCLK. In IDT Standard mode, the flags are double register-buffered outputs. In FWFT mode, the flags are triple register-buffered outputs. Each empty flag operates independently of the others and always indicates the respective FIFO's status.

FULL/INPUT READY FLAG ($\overline{FF}$/$\overline{IR}$/0/1/2/3)

There are four full/input ready flags (two in Dual mode) available in this device, each corresponding to the individual FIFOs in memory. This is a dual-purpose pin whose function is determined based on the state of the FWFT/SI pin during master reset. In the IDT Standard mode, the full flags are selected. When an individual FIFO is full, its full flags will go LOW after the rising edge of WCLK that wrote the last word, thus inhibiting further write operations to the FIFO. When the full flag is HIGH, the individual FIFO is not full and valid write operations can be performed. See Figure 11, *Write Cycle and Full Flag Timing* for the associated timing diagram. Also see Table 4, *Status Flags for FWFT Mode* for the truth table of the full flags.

In FWFT mode, the input ready flags are selected. Input ready flags go LOW when there is adequate memory space in the FIFOs for writing in data. The input ready flags go HIGH after the rising edge of WCLK that wrote the last word, when there are no free spaces available for writing in data. See Figure 16, *Write Cycle and Output Ready Timing* , for the associated timing information. Also see Table 4, *Status Flags for FWFT Mode* for the truth table of the full flags. The input ready status not only measures the contents of the FIFOs memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to make $\overline{IR}$ LOW is one greater than needed to assert $\overline{FF}$ in IDT Standard mode.

$\overline{FF}$/$\overline{IR}$ is synchronous and updated on the rising edge of WCLK. $\overline{FF}$/$\overline{IR}$ are double register-buffered outputs. Each flag operates independently of the others. To prevent data overflow in the IDT Standard mode, the full flag of each FIFO will go LOW with respect to WCLK, when the maximum number of words has been written into the FIFO, thus inhibiting further write operations. Upon the completion of a valid read cycle, the full flag will go HIGH with respect to WCLK two cycles later, thus allowing another write to occur.

To prevent data overflow in the FWFT mode, the input ready flag of each FIFO will go HIGH with respect to WCLK, when the maximum number of words has been written into the FIFO, thus inhibiting further write operations. Upon the completion of a valid read cycle, the input ready flag will go LOW with respect to WCLK two cycles later, thus allowing another write to occur.

PROGRAMMABLE ALMOST EMPTY FLAG ($\overline{PAE}$0/1/2/3)

There are four programmable almost empty flags (two in Dual mode) available in this device, each corresponding to an individual FIFO in memory. The programmable almost empty flag is an additional status flag that notifies the user when the FIFO memory is near empty. The user may utilize this feature as an early indicator as to when the FIFO will become empty. In IDT Standard mode, $\overline{PAE}$ will go LOW when there are n words or less in the FIFO. In FWFT mode, the $\overline{PAE}$ will go LOW when there are n-1 words or less in the FIFO. The offset "n" is the empty offset value. The default setting for this value is stated in Table 2. There are four internal FIFOs hence four $\overline{PAE}$ offset values, (n0, n1, n2, and n3).

There are two timing modes available for the $\overline{PAE}$ flags, selectable by the state of the Programmable Flag Mode (PFM) pin. If PFM is tied HIGH, then synchronous timing mode is selected. If PFM is tied LOW, then asynchronous timing mode is selected. In synchronous configuration, the $\overline{PAE}$ flag is updated on the rising edge of RCLK. In asynchronous $\overline{PAE}$ configuration, the $\overline{PAE}$ flag is asserted LOW on the LOW-to-HIGH transitions of the Read Clock (RCLK). $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transitions of the Write Clock (WCLK). See Figures 31 and 33, *Synchronous and Asynchronous Programmable Almost-Empty Flag Timing*, for the relevant timing information.

Each programmable almost empty flag operates independently of the others.

PROGRAMMABLE ALMOST FULL FLAG ($\overline{PAF}$0/1/2/3)

There are four programmable almost full flags (two in Dual mode) available in this device, each corresponding to the individual FIFOs in memory. The programmable almost full flag is an additional status flag that notifies the user when the FIFO memory is nearly full. The user may utilize this feature as an early indicator as to when the FIFO will not be able to accept any more data and thus prevent data from being dropped. In IDT Standard mode, if no reads are performed after master reset, $\overline{PAF}$ will go LOW after (D-m) (D meaning the density of the particular device) words are written to the FIFO. In FWFT mode, $\overline{PAF}$ will go LOW after (D+1-m) words are written to the FIFO. The offset "m" is the full offset value. The default setting for this value is stated in Table 2. There are four internal FIFOs hence four $\overline{PAF}$ offset values, (m0, m1, m2, and m3).

There are two timing modes available for the $\overline{PAF}$ flags, selectable by the state of the Programmable Flag Mode (PFM) pin. If PFM is tied HIGH, then synchronous timing mode is selected. If PFM is tied LOW, then asynchronous timing mode is selected. In synchronous configuration, the $\overline{PAF}$ flag is updated on the rising edge of WCLK. In asynchronous $\overline{PAF}$ configuration, the $\overline{PAF}$ flag

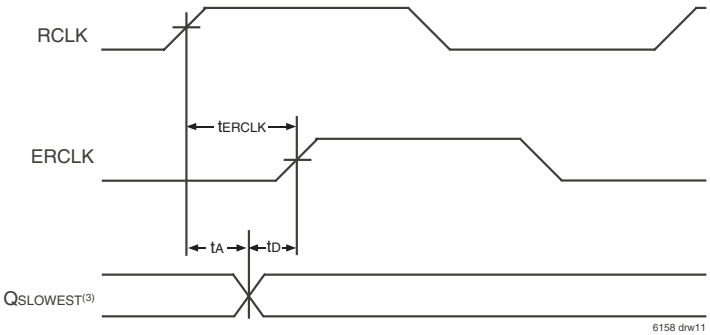
is asserted LOW on the LOW-to-HIGH transitions of the Write Clock (WCLK). $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transitions of the Read Clock (RCLK). See Figure 31 and 33, Synchronous and Asynchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT mode), for the relevant timing information.

Each programmable almost full flag operates independently of the others.

ECHO READ CLOCK (ERCLK0/1/2/3)

There are four echo read clock outputs (two in Dual mode) available in this device, each corresponding to their respective input read clocks in the FIFO. The echo read clock is a free-running clock output, that will always follow the RCLK input regardless of the read enables and read chip selects. The ERCLK output follows the RCLK input with an associated delay. This delay provides the user with a more effective read clock source when reading data from the output bus. This is especially helpful at high speeds when variables within the device may cause changes in the data access times. These variations in access time may be caused by ambient temperature, supply voltage, or device characteristics.

Any variations effecting the data access time will also have a corresponding effect on the echo read clock output produced by the FIFO, therefore the echo read clock output level transitions should always be at the same position in time relative to the data outputs. Note, that echo read clock is guaranteed by design to be slower than the slowest data outputs. Refer to Figure 6, *Echo Read Clock and Data Output Relationship*, Figures 25, 26, and 27 *Echo Read Clock and Read Enable Operation* for timing information. Each echo read clock output operate independently of the others and transitions with respect to the data outputs of its FIFO.



NOTES:
1. $\overline{REN}$ is LOW.
2. $t_{ERCLK} > t_A$, guaranteed by design.
3. Qslowest is the data output with the slowest access time, t_A.
4. Time, t_D is greater than zero, guaranteed by design.

Figure 6. Echo Read Clock and Data Output Relationship

TABLE 6 — TSKEW MEASUREMENT

Data Port Configuration	Status Flags	TSKEW Measurement	Datasheet Parameter
DDR Input to DDR Output	$\overline{EF}/\overline{OR}$	Negative Edge WCLK to Positive Edge RCLK	tSKEW2
	$\overline{FF}/\overline{IR}$	Negative Edge RCLK to Positive Edge WCLK	tSKEW2
	$\overline{PAE}$	Negative Edge WCLK to Positive Edge RCLK	tSKEW3
	$\overline{PAF}$	Negative Edge RCLK to Positive Edge WCLK	tSKEW3
DDR Input to SDR Output	$\overline{EF}/\overline{OR}$	Negative Edge WCLK to Positive Edge RCLK	tSKEW2
	$\overline{FF}/\overline{IR}$	Positive Edge RCLK to Positive Edge WCLK	tSKEW1
	$\overline{PAE}$	Negative Edge WCLK to Positive Edge RCLK	tSKEW3
	$\overline{PAF}$	Positive Edge RCLK to Positive Edge WCLK	tSKEW3
SDR Input to DDR Output	$\overline{EF}/\overline{OR}$	Positive Edge WCLK to Positive Edge RCLK	tSKEW1
	$\overline{FF}/\overline{IR}$	Negative Edge RCLK to Positive Edge WCLK	tSKEW2
	$\overline{PAE}$	Positive Edge WCLK to Positive Edge RCLK	tSKEW3
	$\overline{PAF}$	Negative Edge RCLK to Positive Edge WCLK	tSKEW3
SDR Input to SDR Output	$\overline{EF}/\overline{OR}$	Positive Edge WCLK to Positive Edge RCLK	tSKEW1
	$\overline{FF}/\overline{IR}$	Positive Edge RCLK to Positive Edge WCLK	tSKEW1
	$\overline{PAE}$	Positive Edge WCLK to Positive Edge RCLK	tSKEW3
	$\overline{PAF}$	Positive Edge RCLK to Positive Edge WCLK	tSKEW3

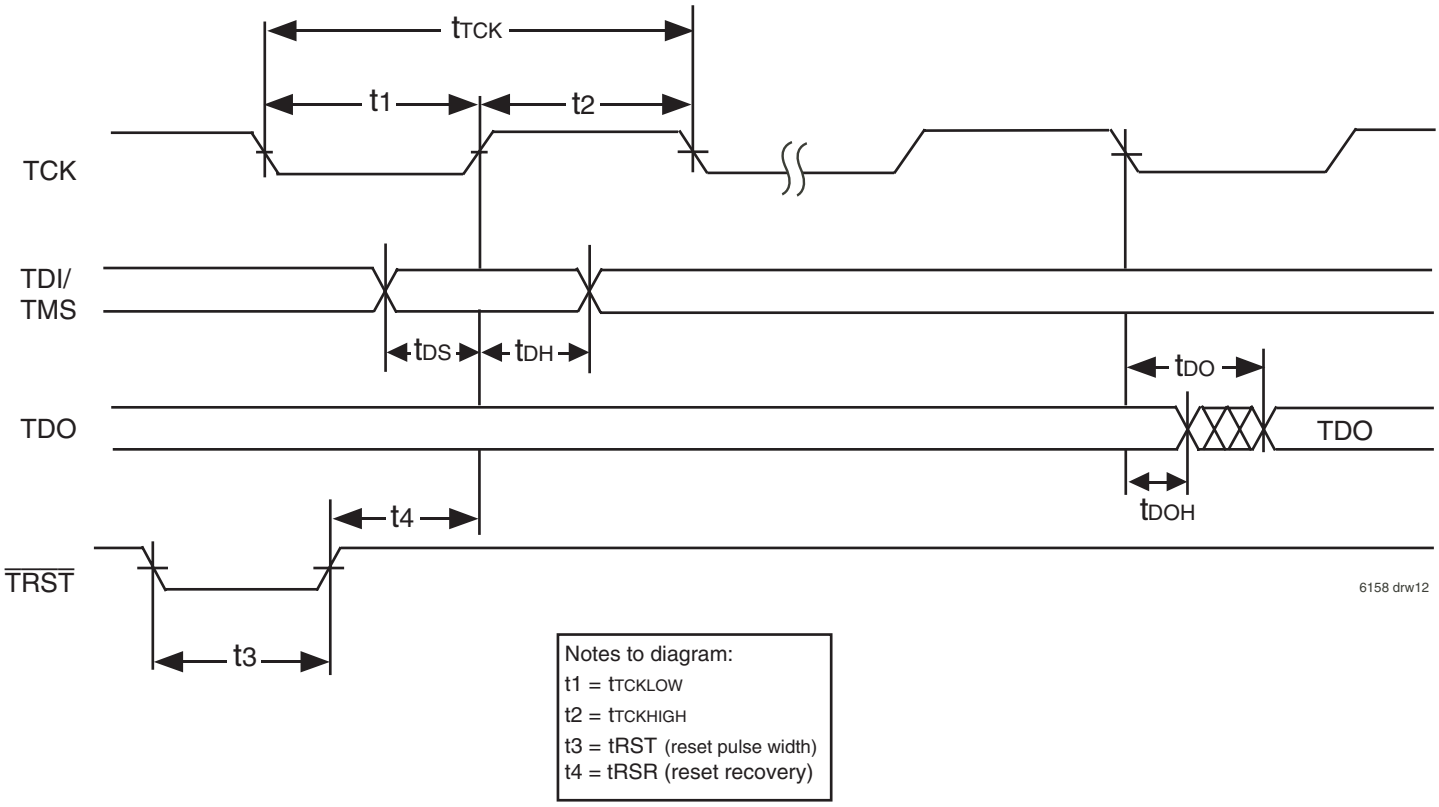


Figure 7. Standard JTAG Timing

SYSTEM INTERFACE PARAMETERS

Parameter	Symbol	Test Conditions	IDT72T54242 IDT72T54252 IDT72T54262		
			Min.	Max.	Units
Data Output	t_{DO}[1]		-	20	ns
Data Output Hold	t_{DOH}[1]		0	-	ns
Data Input	t_{DS}	trise=3ns	10	-	ns
	t_{DH}	tfall=3ns	10	-	

NOTE:
1. 50pf loading on external output signals.

JTAG AC ELECTRICAL CHARACTERISTICS

(Vcc = 2.5V ± 5%; Tcase = 0°C to +85°C)

Parameter	Symbol	Test Conditions	Min.	Max.	Units
JTAG Clock Input Period	tTCK	-	100	-	ns
JTAG Clock HIGH	tTCKHIGH	-	40	-	ns
JTAG Clock Low	tTCKLOW	-	40	-	ns
JTAG Reset	tRST	-	50	-	ns
JTAG Reset Recovery	tRSR	-	50	-	ns

JTAG TIMING SPECIFICATIONS (IEEE 1149.1 COMPLIANT)

The JTAG test port in this device is fully compliant with the IEEE Standard Test Access Port (IEEE 1149.1) specifications. Five additional pins (TDI, TDO, TMS, TCK and $\overline{TRST}$) are provided to support the JTAG boundary scan interface. Note that IDT provides appropriate Boundary Scan Description Language program files for these devices.

The Standard JTAG interface consists of five basic elements:

- *Test Access Port (TAP)*
- *TAP controller*
- *Instruction Register (IR)*
- *Data Register Port (DR)*
- *Bypass Register (BYR)*

The following sections provide a brief description of each element. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

The Figure below shows the standard Boundary-Scan Architecture

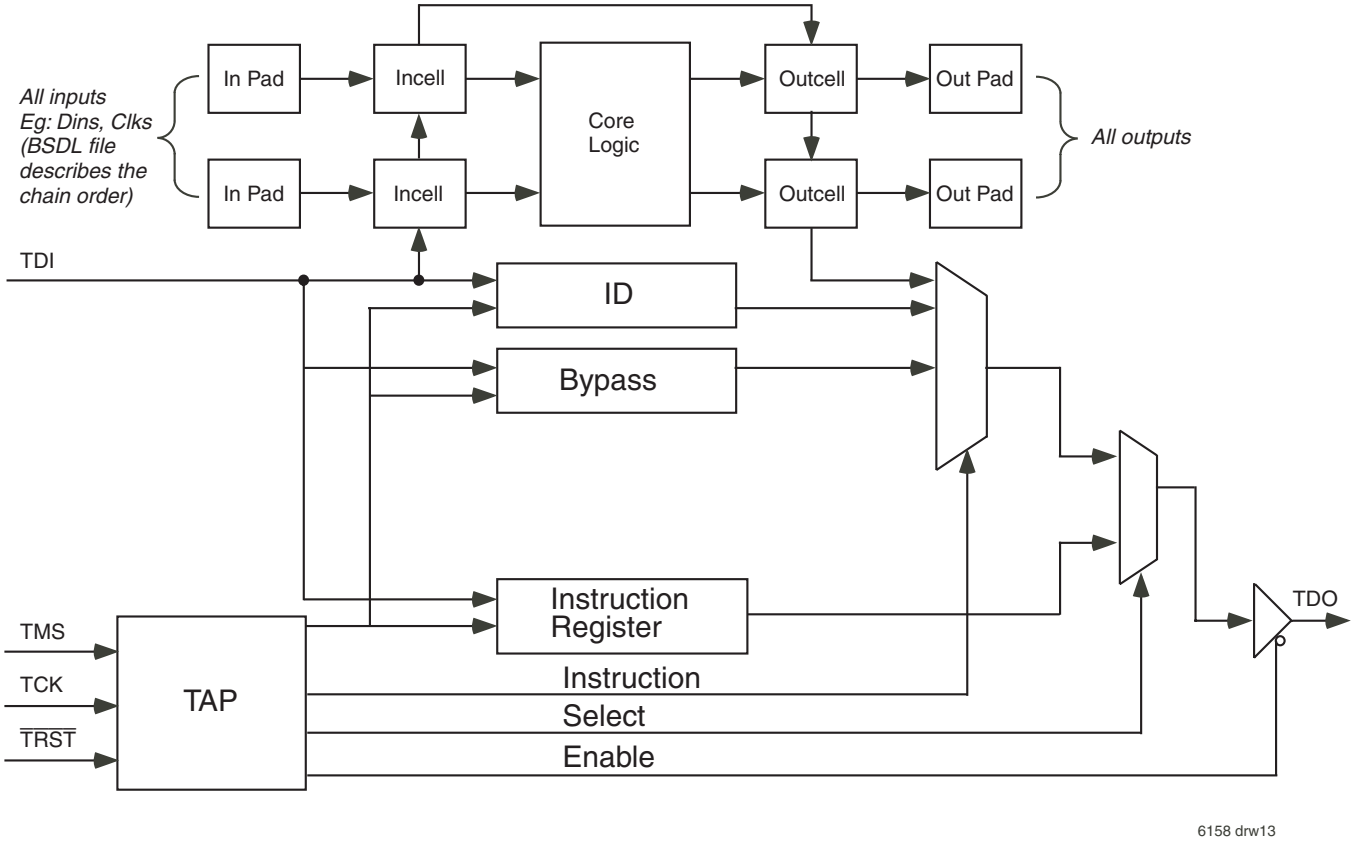


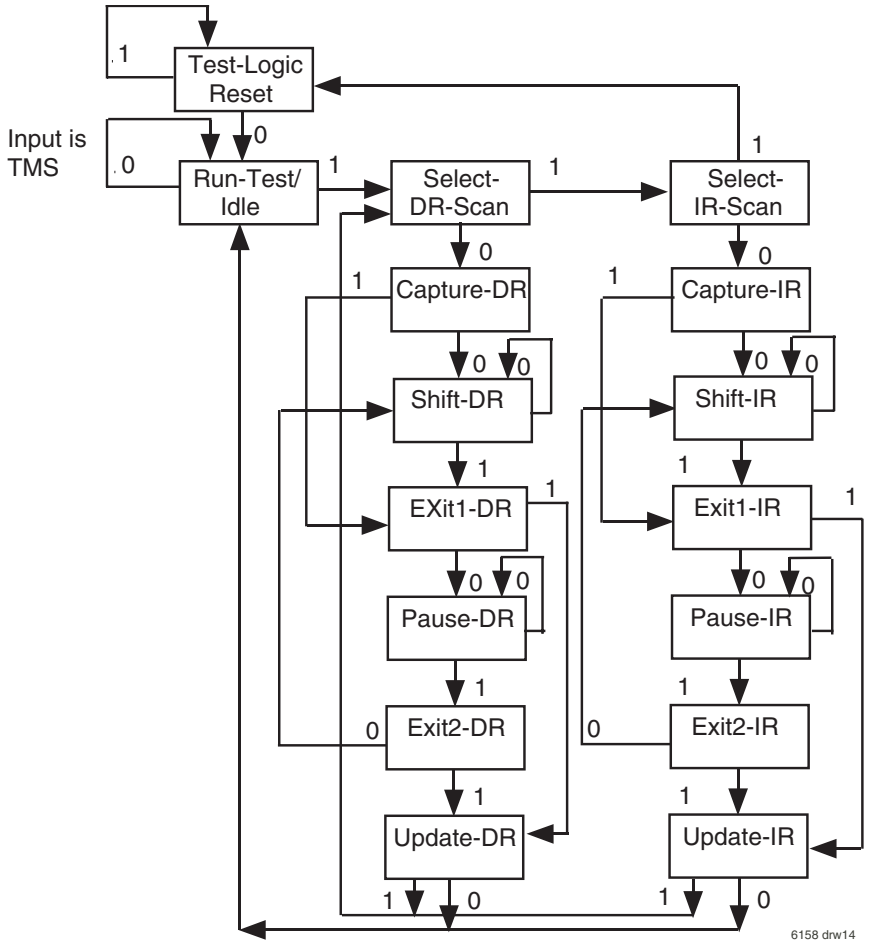
Figure 8. JTAG Architecture

TEST ACCESS PORT (TAP)

The TAP interface is a general-purpose port that provides access to the internal JTAG state machine. It consists of four input ports (TCLK, TMS, TDI, $\overline{TRST}$) and one output port (TDO).

THE TAP CONTROLLER

The TAP controller is a synchronous finite state machine that responds to TMS and TCLK signals to generate clock and control signals to the Instruction and Data Registers for capture and updating of data passed through the TDI serial input.



NOTES:
1. Five consecutive TCK cycles with TMS = 1 will reset the TAP.
2. TAP controller does not automatically reset upon power-up. The user must provide a reset to the TAP controller (either by $\overline{TRST}$ or TMS).
3. TAP controller must be reset before normal FIFO operations can begin.

Figure 9. TAP Controller State Diagram

Refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1) for the full state diagram

All state transitions within the TAP controller occur at the rising edge of the TCLK pulse. The TMS signal level (0 or 1) determines the state progression that occurs on each TCLK rising edge. The TAP controller takes precedence over the FIFO memory and must be reset after power up of the device. See $\overline{TRST}$ description for more details on TAP controller reset.

Test-Logic-Reset All test logic is disabled in this controller state enabling the normal operation of the IC. The TAP controller state machine is designed in such a way that, no matter what the initial state of the controller is, the Test-Logic-Reset state can be entered by holding TMS at high and pulsing TCK five times. This is the reason why the Test Reset (TRST) pin is optional.

Run-Test-Idle In this controller state, the test logic in the IC is active only if certain instructions are present. For example, if an instruction activates the self test, then it will be executed when the controller enters this state. The test logic in the IC is idles otherwise.

Select-DR-Scan This is a controller state where the decision to enter the Data Path or the Select-IR-Scan state is made.

Select-IR-Scan This is a controller state where the decision to enter the Instruction Path is made. The Controller can return to the Test-Logic-Reset state other wise.

Capture-IR In this controller state, the shift register bank in the Instruction Register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits are always required to be "01".

Shift-IR In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in to the instruction register.

Exit1-IR This is a controller state where a decision to enter either the Pause-IR state or Update-IR state is made.

Pause-IR This state is provided in order to allow the shifting of instruction register to be temporarily halted.

Exit2-DR This is a controller state where a decision to enter either the Shift-IR state or Update-IR state is made.

Update-IR In this controller state, the instruction in the instruction register is latched in to the latch bank of the Instruction Register on every falling edge of TCK. This instruction also becomes the current instruction once it is latched.

Capture-DR In this controller state, the data is parallel loaded in to the data registers selected by the current instruction on the rising edge of TCK.

Shift-DR, Exit1-DR, Pause-DR, Exit2-DR and Update-DR These controller states are similar to the Shift-IR, Exit1-IR, Pause-IR, Exit2-IR and Update-IR states in the Instruction path.

THE INSTRUCTION REGISTER

The Instruction register allows an instruction to be shifted in serially into the processor at the rising edge of TCLK.

The Instruction is used to select the test to be performed, or the test data register to be accessed, or both. The instruction shifted into the register is latched at the completion of the shifting process when the TAP controller is at Update-IR state.

The instruction register must contain 4 bit instruction register-based cells which can hold instruction data. These mandatory cells are located nearest the serial outputs they are the least significant bits.

TEST DATA REGISTER

The Test Data register contains three test data registers: the Test Bypass register, the Boundary Scan register and Device ID register.

These registers are connected in parallel between a common serial input and a common serial data output.

The following sections provide a brief description of each element. For a complete description, refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

Test Bypass Register

The register is used to allow test data to flow through the device from TDI to TDO. It contains a single stage shift register for a minimum length in serial path. When the bypass register is selected by an instruction, the shift register stage is set to a logic zero on the rising edge of TCLK when the TAP controller is in the Capture-DR state.

The operation of the bypass register should not have any effect on the operation of the device in response to the BYPASS instruction.

The Boundary-Scan Register

The Boundary Scan Register allows serial data TDI be loaded in to or read out of the processor input/output ports. The Boundary Scan Register is a part of the IEEE 1149.1-1990 Standard JTAG Implementation.

The Device Identification Register

The Device Identification Register is a Read Only 32-bit register used to specify the manufacturer, part number and version of the processor to be determined through the TAP in response to the IDCODE instruction.

IDT JEDEC ID number is 0xB3. This translates to 0x33 when the parity is dropped in the 11-bit Manufacturer ID field.

For the IDT72T54242/72T54252/72T54262, the Part Number field contains the following values:

Device	Part# Field
IDT72T54242	4C5 (hex)
IDT72T54252	4C6 (hex)
IDT72T54262	4C7 (hex)

31(MSB) 28	27 12	11 1	0(LSB)
Version (4 bits) 0X0	Part Number (16-bit)	Manufacturer ID (11-bit) 00B3 (hex)	1

IDT72T54242/252/262 JTAG Device Identification Register

JTAG INSTRUCTION REGISTER

The Instruction register allows instruction to be serially input into the device when the TAP controller is in the Shift-IR state. The instruction is decoded to perform the following:

- Select test data registers that may operate while the instruction is current. The other test data registers should not interfere with chip operation and the selected data register.
- Define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

The Instruction Register is a 4 bit field (i.e. IR3, IR2, IR1, IR0) to decode 16 different possible instructions. Instructions are decoded as follows.

Hex Value	Instruction	Function
0000	EXTEST	Test external pins
0001	SAMPLE/PRELOAD	Select boundary scan register
0002	IDCODE	Selects chip identification register
0003	CLAMP	Fix the output chains to scan chain values
0004	HI-IMPEDANCE	Puts all outputs in high-impedance state
0007	OFFSET READ	Read $\overline{PAE}$/$\overline{PAF}$ offset register values
0008	OFFSET WRITE	Write $\overline{PAE}$/$\overline{PAF}$ offset register values
000F	BYPASS	Select bypass register
	Private	Several combinations are private (for IDT internal use). Do not use codes other than those identified above.

JTAG Instruction Register Decoding

The following sections provide a brief description of each instruction. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

EXTEST

The required EXTEST instruction places the IC into an external boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register is accessed to drive test data off-chip via the boundary outputs and receive test data off-chip via the boundary inputs. As such, the EXTEST instruction is the workhorse of IEEE. Std 1149.1, providing for probe-less testing of solder-joint opens/shorts and of logic cluster function.

SAMPLE/PRELOAD

The required SAMPLE/PRELOAD instruction allows the IC to remain in a normal functional mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register can be accessed via a date scan operation, to take a sample of the functional data entering and leaving the IC. This instruction is also used to preload test data into the boundary-scan register before loading an EXTEST instruction.

IDCODE

The optional IDCODE instruction allows the IC to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO. The device identification register is a 32-bit shift register containing information regarding the IC manufacturer, device type, and version code. Accessing the device identification register does not interfere with the operation of the IC. Also, access to the device identification register should be immediately available, via a TAP data-scan operation, after power-up of the IC or after the TAP has been reset using the optional $\overline{TRST}$ pin or by otherwise moving to the Test-Logic-Reset state.

CLAMP

The optional CLAMP instruction sets the outputs of an IC to logic levels determined by the contents of the boundary-scan register and selects the one-bit bypass register to be connected between TDI and TDO. Before loading this instruction, the contents of the boundary-scan register can be preset with the SAMPLE/PRELOAD instruction. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the outputs.

HIGH-IMPEDANCE

The optional High-Impedance instruction sets all outputs (including two-state as well as three-state types) of an IC to a disabled (high-impedance) state and selects the one-bit bypass register to be connected between TDI and TDO. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the IC outputs.

OFFSET READ

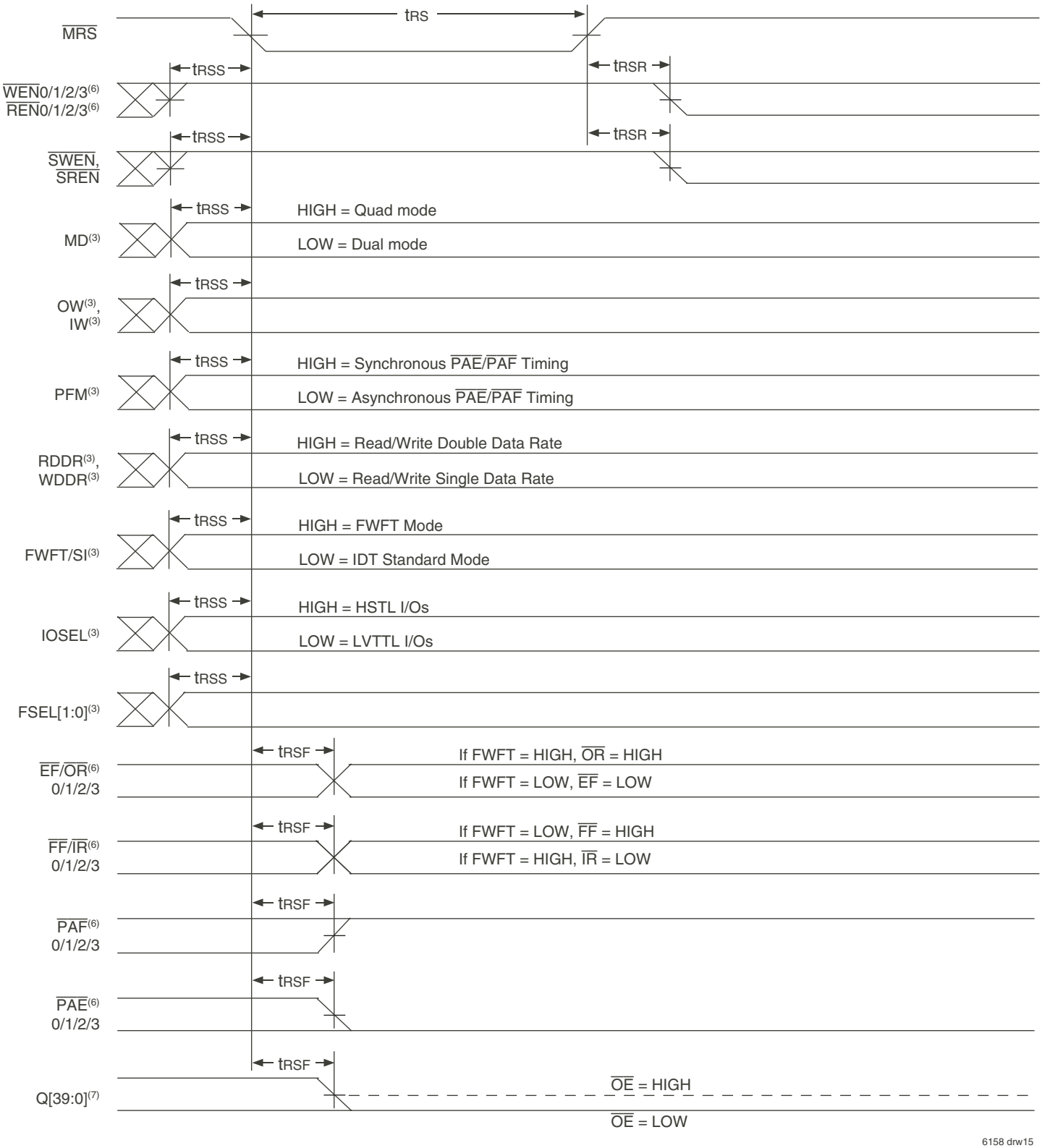
This instruction is an alternative to serial reading the offset registers for the $\overline{PAE}$/$\overline{PAF}$ flags. When reading the offset registers through this instruction, the dedicated serial programming signals must be disabled.

OFFSET WRITE

This instruction is an alternative to serial programming the offset registers for the $\overline{PAE}$/$\overline{PAF}$ flags. When writing the offset registers through this instruction, the dedicated serial programming signals must be disabled.

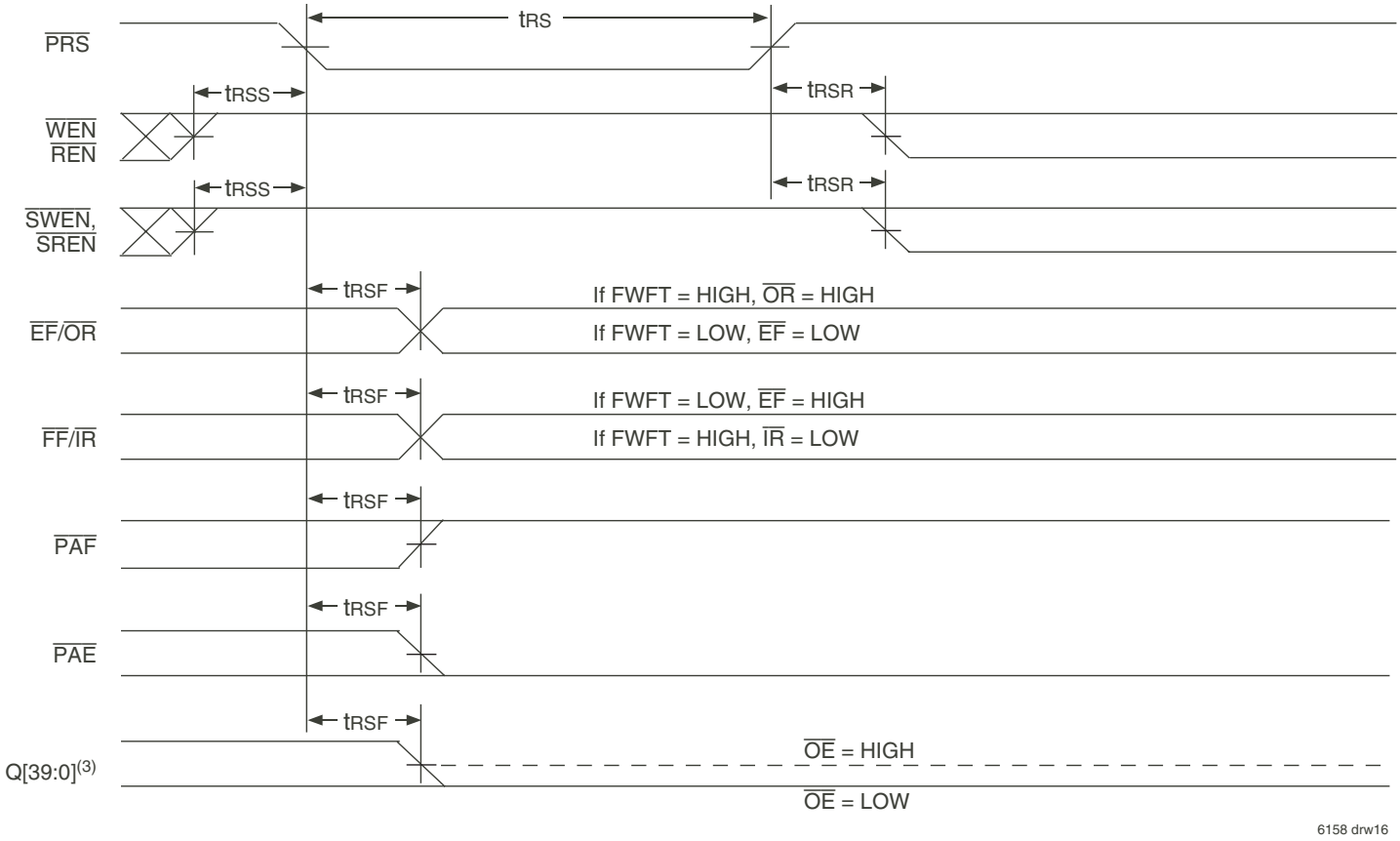
BYPASS

The required BYPASS instruction allows the IC to remain in a normal functional mode and selects the one-bit bypass register to be connected between TDI and TDO. The BYPASS instruction allows serial data to be transferred through the IC from TDI to TDO without affecting the operation of the IC.



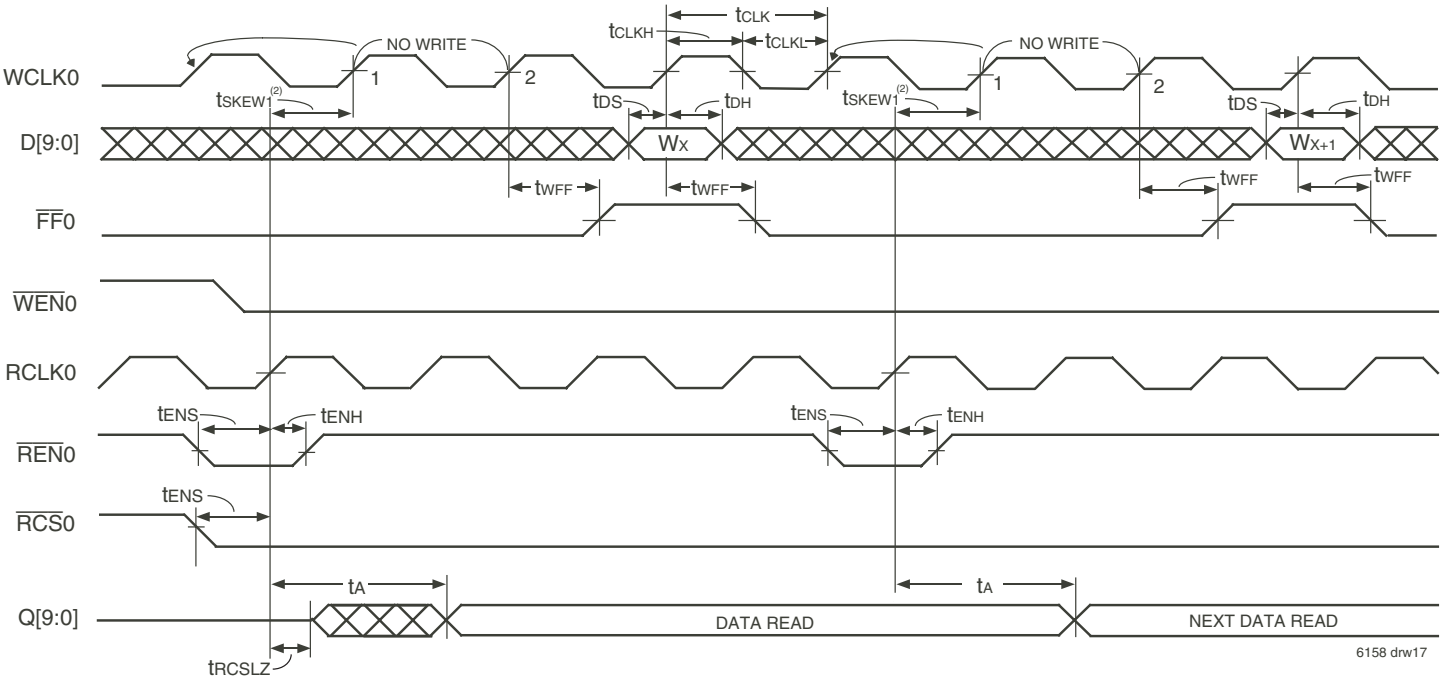
NOTES:
1. $\overline{OE}$ can be toggled during master reset. During master reset, the high-impedance control of the Qn data outputs are provided by $\overline{OE}$ only.
2. RCLK(s), WCLK(s) and SCLK(s) can be free running or idle.
3. The state of these pins are latched when the master reset pulse is LOW.
4. JTAG flag should not toggle during master reset.
5. $\overline{RCS}$ and $\overline{WCS}$ can be HIGH or LOW until the first rising edge of RCLK after master reset is complete.
6. If Dual mode is selected, only the signals designated with a "0" or "2" are used.
7. If Dual mode is selected, outputs Q[19:10] and Q[39:30] are not used if outputs are configured to x10.

Figure 10 . Master Reset Timing



NOTES:
1. This timing diagram shows the partial reset timing for a single FIFO. Each $\overline{PRS}$ is independent of the others.
2. During partial reset the high-impedance control of the Qn data outputs are provided by $\overline{OE}$ only, $\overline{RCS}$ can be HIGH or LOW until the first rising edge of RCLK after master reset.
3. If Dual mode is selected, outputs Q[19:10] and Q[39:30] are not used if outputs are configured to x10.

Figure 11. Partial Reset Timing

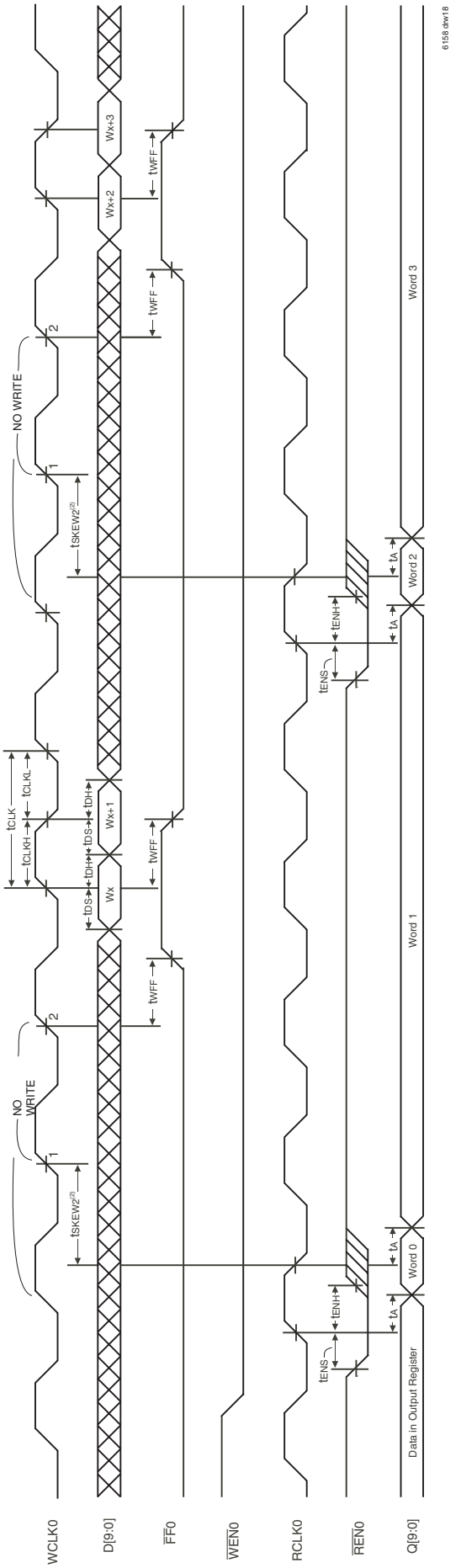


NOTES:

1. The timing diagram shown is for FIFO0. FIFO1-3 exhibits the same behavior.
2. t_{SKEW1} is the minimum time between a rising RCLK0 edge and a rising WCLK0 edge to guarantee that $\overline{FF}0$ will go HIGH (after one WCLK0 cycle plus t_{WFF}). If the time between the rising edge of the RCLK0 and the rising edge of the WCLK0 is less than t_{SKEW1}, then the $\overline{FF}0$ deassertion may be delayed one extra WCLK0 cycle. (See Table 6 - T_{SKEW} measurement).
3. $\overline{OE}0$ = LOW, and $\overline{WCS}0$ = LOW.
4. WCLK0 must be free running for $\overline{FF}0$ to update.
5.

MD	IW	OW	WDDR	RDDR	FWFT/SI
1	D/C	D/C	0	0	0

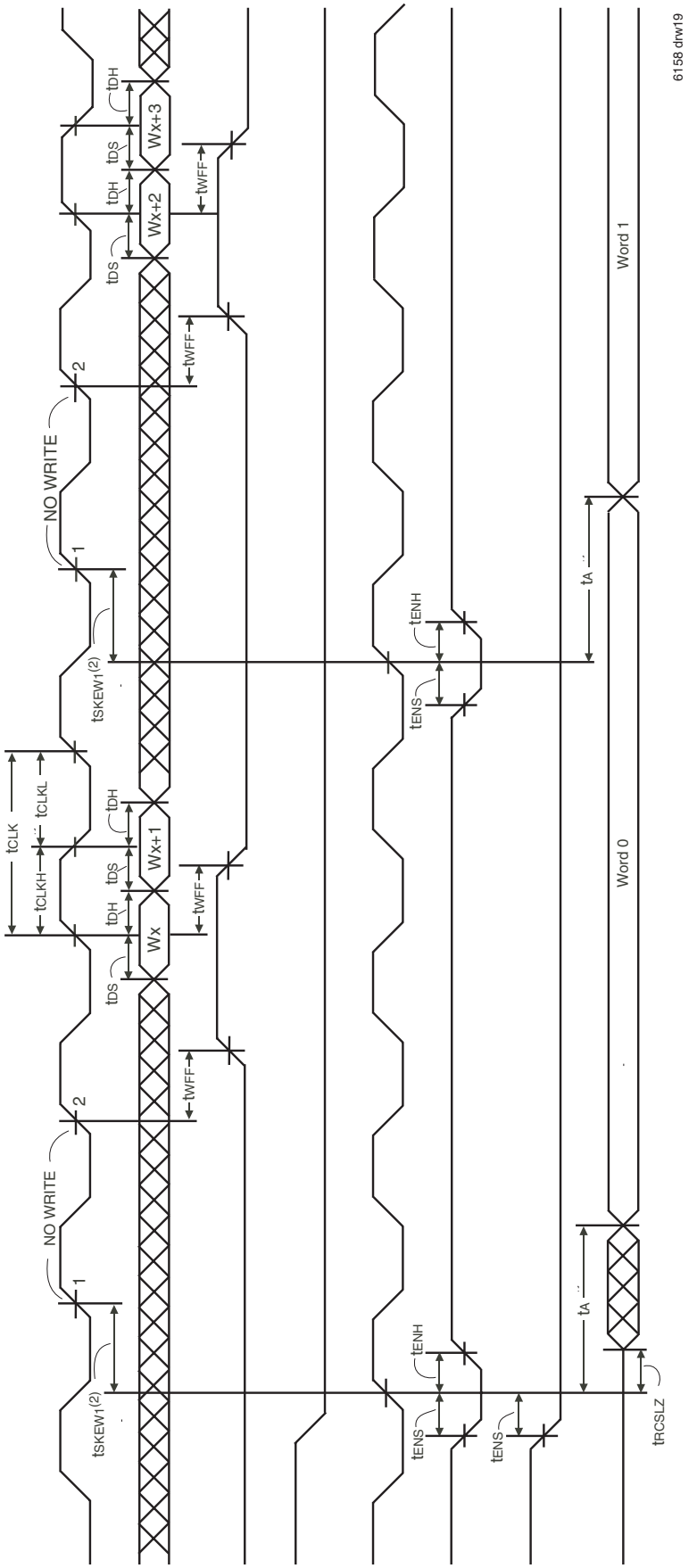
Figure 12. Write Cycle and Full Flag Timing (Quad mode, IDT Standard mode, SDR to SDR)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibits the same behavior.
2. t_{SKEW2} is the minimum time between a falling RCLK0 edge and a rising WCLK0 edge to guarantee that $\overline{FF}0$ will go HIGH (after one WCLK0 cycle plus t_{WFF}). If the time between the falling edge of the RCLK0 and the rising edge of WCLK0 is less than t_{SKEW2}, then $\overline{FF}0$ deassertion may be delayed one extra WCLK0 cycle. (See Table 6 - T_{SKEW} measurement).
3. $\overline{OE}0$ = LOW, $\overline{WCS}0$ = LOW, and $\overline{RCS}0$ = LOW.
4. WCLK0 must be free running for $\overline{FF}0$ to update.
5.

MD	W	OW	WDDR	RDDR	FWFT/SI
1	D/C	D/C	1	1	0

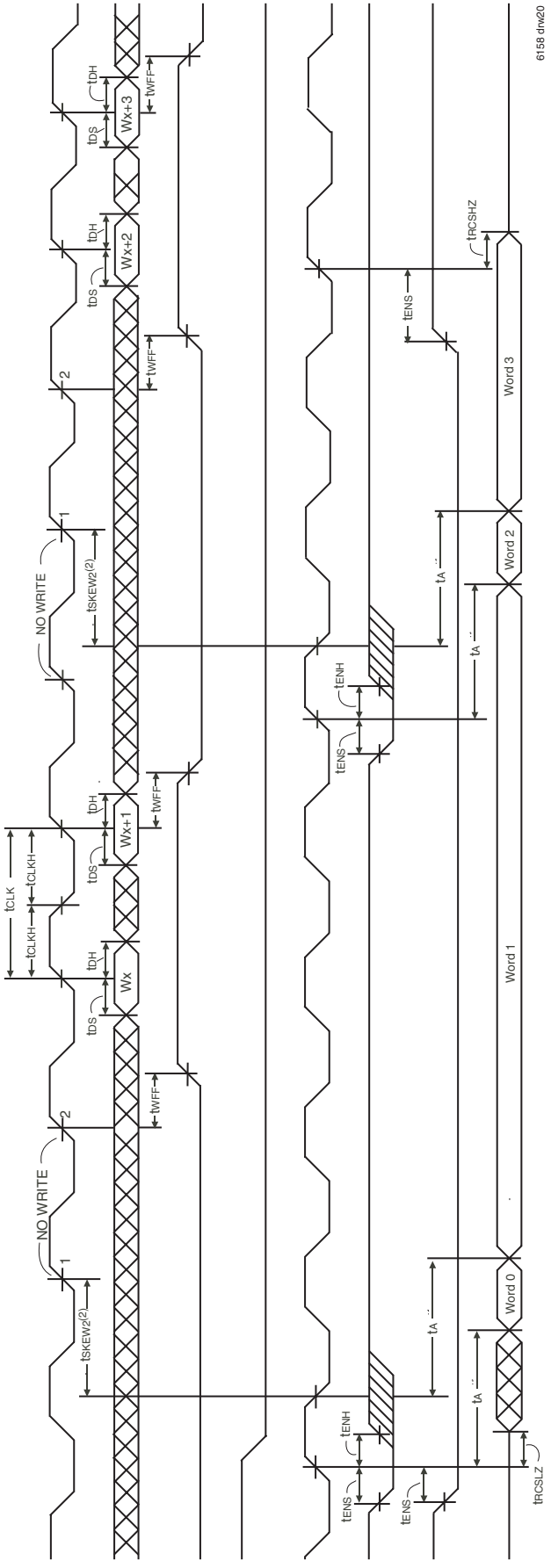
Figure 13. Write Cycle and Full Flag Timing (Quad mode, IDT Standard mode, DDR to DDR)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO 2 exhibit the same behavior.
2. t_{SKEW1} is the minimum time between a rising RCLK0 edge and a rising WCLK0 edge to guarantee that $\overline{FF}0$ will go HIGH (after one WCLK0 cycle plus t_{WFF}). If the time between the rising edge of the RCLK0 and the rising edge of the WCLK0 is less than t_{SKEW1}, then the $\overline{FF}0$ deassertion may be delayed one extra WCLK cycle. (See Table 6 - T_{SKEW} measurement).
4. $\overline{OE}0$ = LOW, and $\overline{WCS}0$ = LOW.
5. WCLK0 must be free running for $\overline{FF}0$ to update.
3.

MD	IW	OW	WDDR	RDDR	FWFT/SI
0	0	1	1	0	0

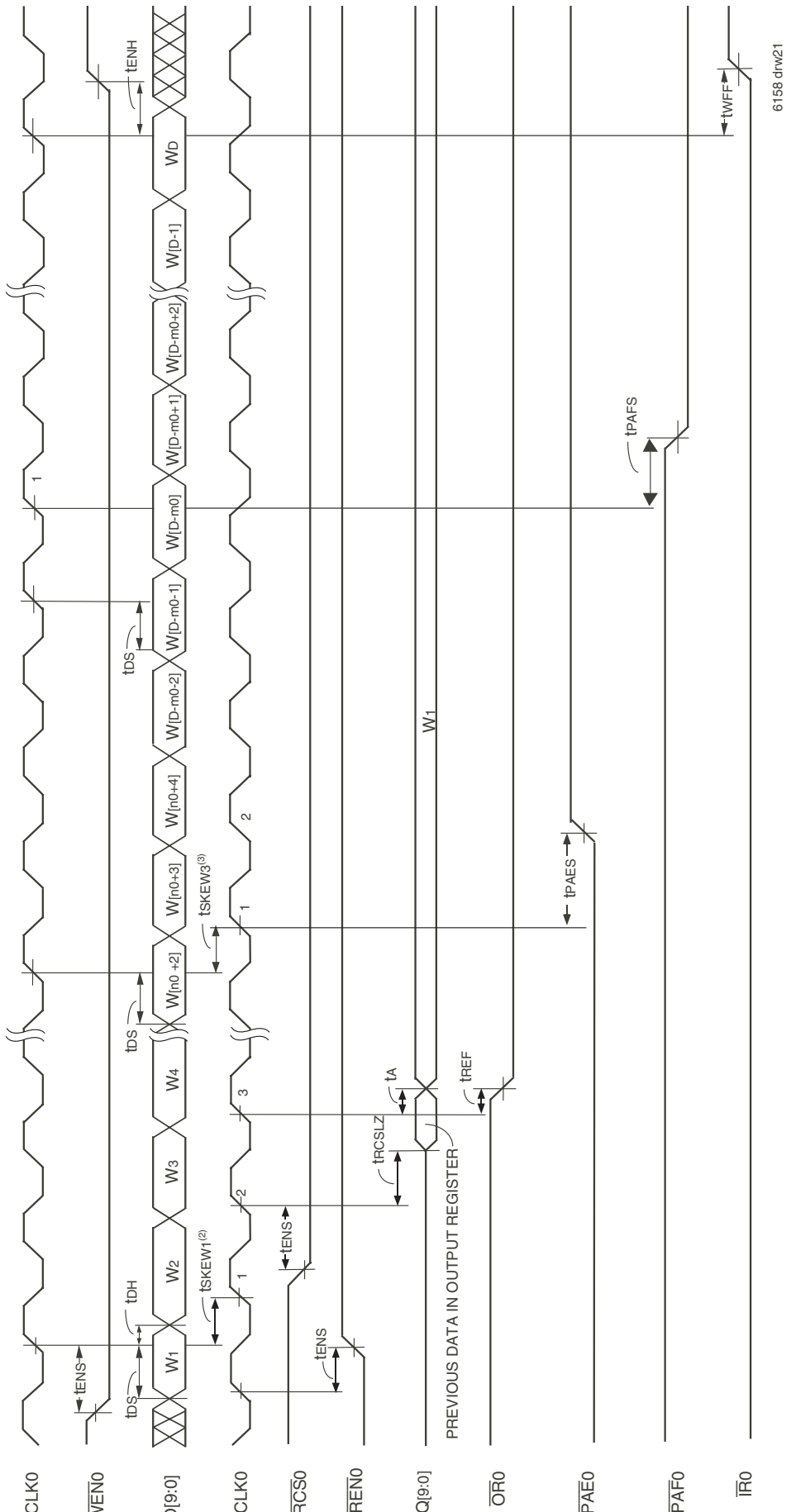
Figure 14. Write Cycle and Full Flag Timing (Dual mode, IDT Standard mode, DDR to SDR, x10 In to x20 Out)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO 2 exhibit the same behavior.
2. t_{SKEW2} is the minimum time between a falling RCLK0 edge and a rising WCLK0 edge to guarantee that $\overline{FF}0$ will go HIGH (after one WCLK0 cycle plus t_{WFF}). If the time between the falling edge of the RCLK0 and the rising edge of WCLK0 is less than t_{SKEW2}, then $\overline{FF}0$ deassertion may be delayed one extra WCLK0 cycle. (See Table 6 - T_{SKEW} measurement).
3. $\overline{OE}0$ = LOW, $\overline{WCS}0$ = LOW, and $\overline{RCS}0$ = LOW.
4. WCLK0 must be free running for $\overline{FF}0$ to update.
5.

MD	MW	OW	WDDR	RDDR	FWFT/SI
0	1	0	0	1	0

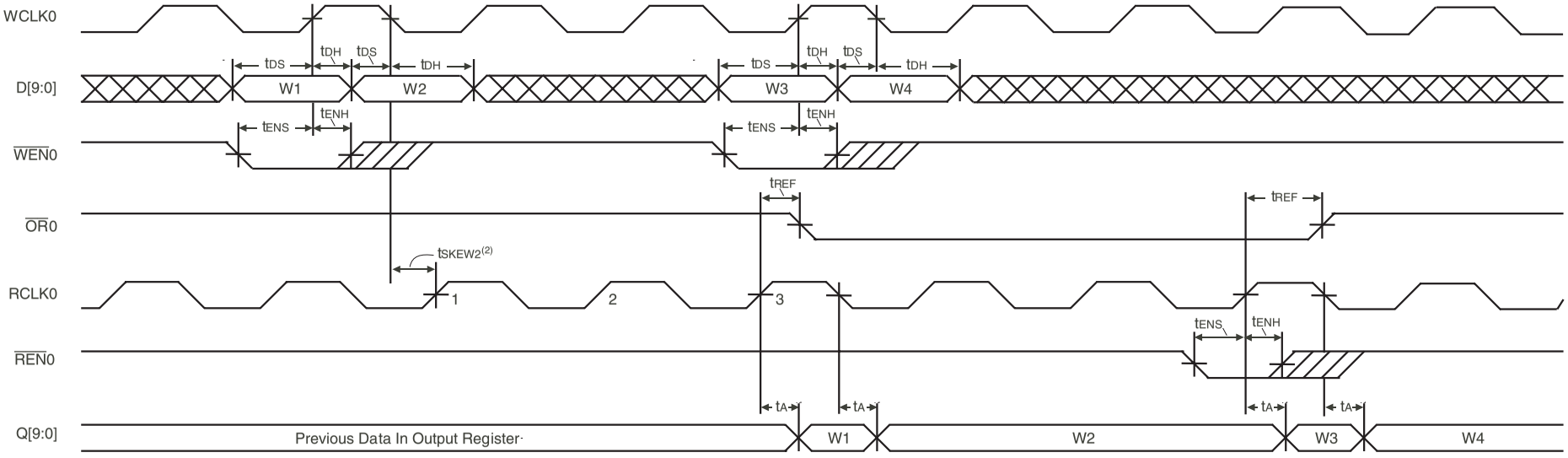
Figure 15. Write Cycle and Full Flag (Dual mode, IDT Standard mode, SDR to DDR, x20 In to x10 Out)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibits the same behavior.
2. t_{SKEW1} is the minimum time between a rising WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{OR}0$ will go LOW after two RCLK0 cycles plus t_{REF}. If the time between the rising edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW1}, then $\overline{OR}0$ assertion may be delayed one extra RCLK0 cycle. (See Table 6 - T_{SKEW} measurement).
3. t_{SKEW3} is the minimum time between a rising WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{PAE}0$ will go HIGH after one RCLK0 cycle plus t_{PAES}. If the time between the rising edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW3}, then the $\overline{PAE}0$ deassertion may be delayed one extra RCLK0 cycle. (See Table 6 - T_{SKEW} measurement).
4. n0 = $\overline{PAE}0$ offset, m0 = $\overline{PAF}0$ offset and D = maximum FIFO depth.
5. $\overline{OE}0$ = LOW, and $\overline{WCS}0$ = LOW.
6. First data word latency = t_{SKEW1} + 2*T_{RCLK} + t_{REF}.
7. WCLK0 must be free running for $\overline{OR}0$ to update.
8.

MD	IW	OW	WDDR	RDDR	PFM	FWFT/SI
1	D/C	D/C	0	0	1	1

Figure 16. Write Cycle and Output Ready Timing (Quad mode, FWFT mode, SDR to SDR)

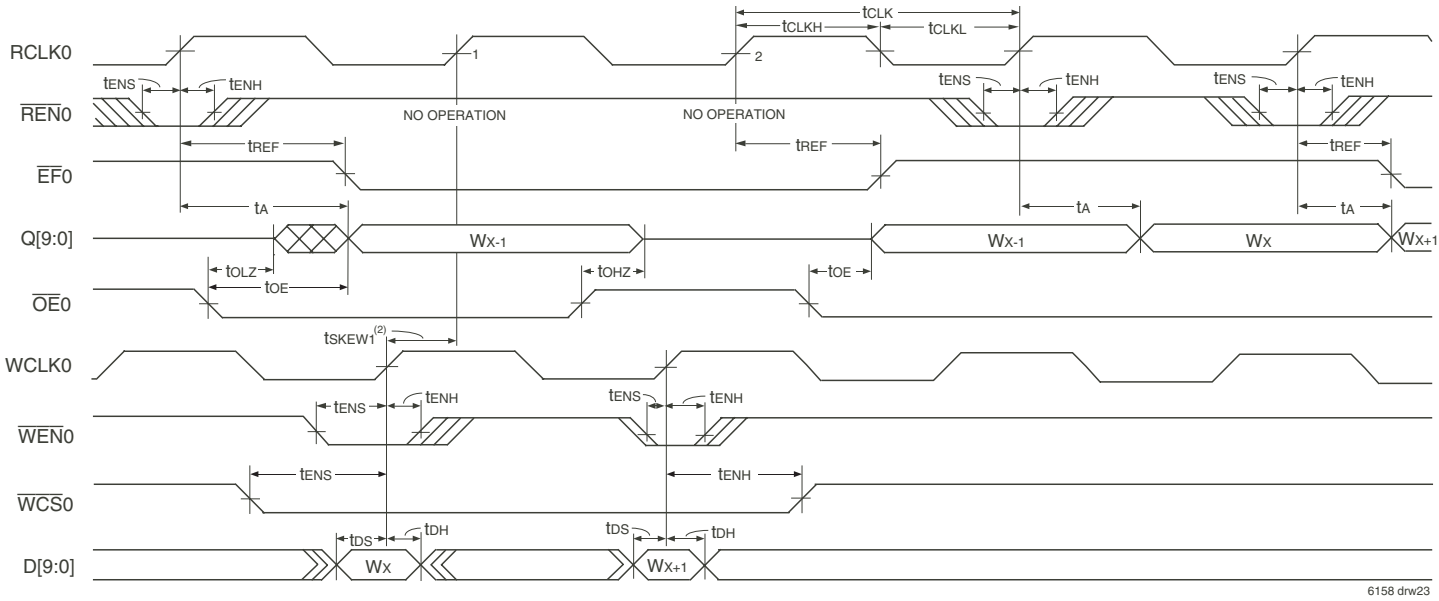


NOTES:

1. The timing diagram shown is for FIFO0. FIFO1-3 exhibits the same behavior.
2. t_{SKEW2} is the minimum time between a falling WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{OR}0$ will go LOW after two RCLK0 cycle plus t_{REF}. If the time between the falling edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW2}, then $\overline{OR}0$ assertion may be delayed one extra RCLK0 cycle. (See Table 6 - T_{SKEW} measurement).
3. $\overline{OE}0$ = LOW, $\overline{RCS}0$ = LOW, and $\overline{WCS}0$ = LOW.
4. First data word latency = t_{SKEW2} + 2*T_{RCLK} + t_{REF}.
5. WCLK0 must be free running for $\overline{OR}0$ to update.
6.

MD	IW	OW	WDDR	RDDR	FWFT/SI
1	D/C	D/C	1	1	1

Figure 17. Write Cycle and Output Ready Timing (Quad mode, FWFT mode, DDR to DDR)

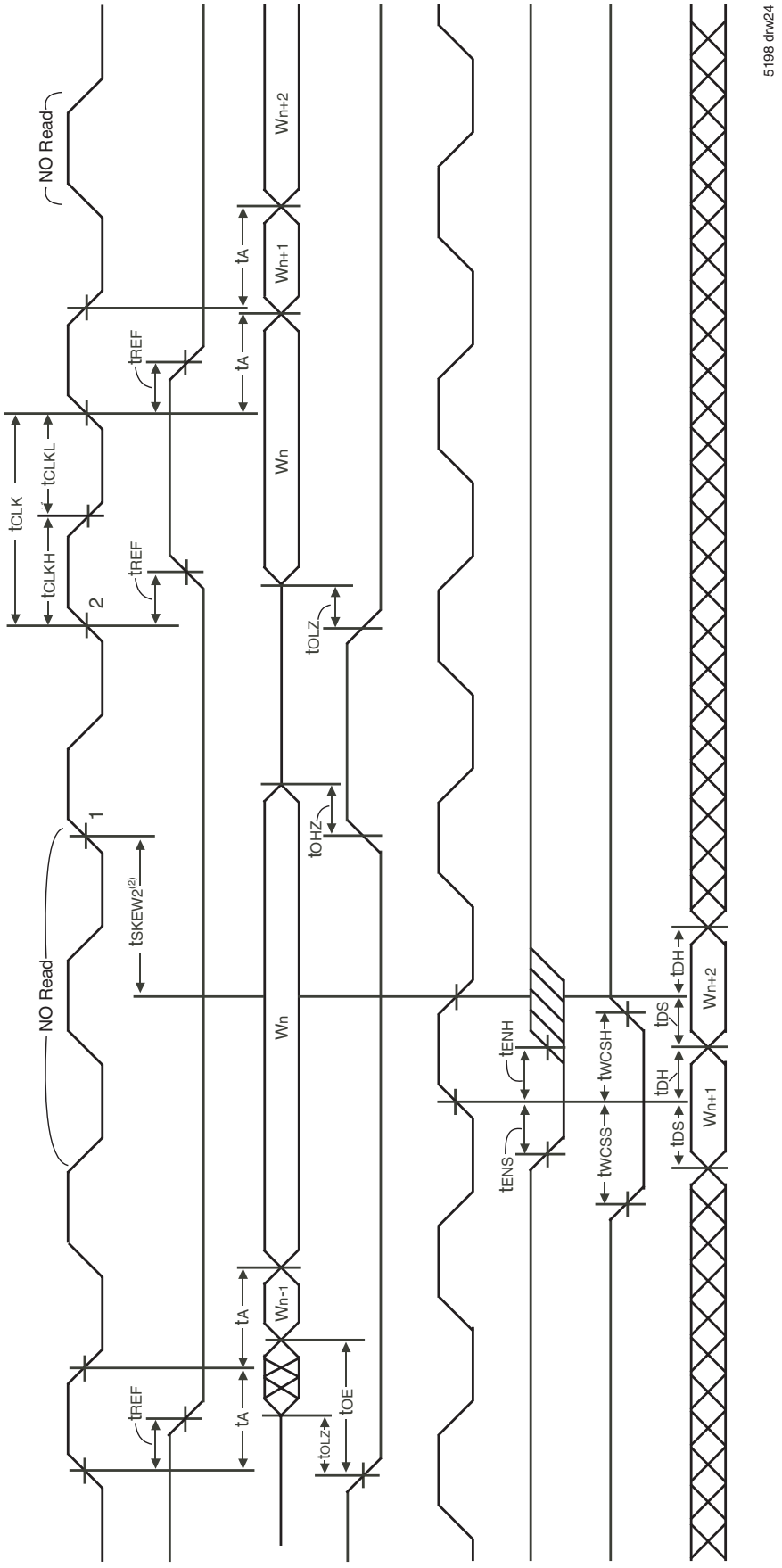


NOTES:

1. The timing diagram shown is for FIFO0. FIFO1-3 exhibits the same behavior.
2. t_{SKEW1} is the minimum time between a rising WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{EF}0$ will go HIGH (after one RCLK0 cycle plus t_{REF}). If the time between the rising edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW1}, then $\overline{EF}0$ deassertion may be delayed one extra RCLK0 cycle. (See Table 6 - T_{SKEW} measurement)..
3. First data word latency = t_{SKEW1} + 1*T_{RCLK} + t_{REF}.
4. $\overline{RCS}0$ = LOW.
5. RCLK0 must be free running for $\overline{EF}0$ to update.
6.

MD	IW	OW	WDDR	RDDR	FWFT/SI
1	D/C	D/C	0	0	0

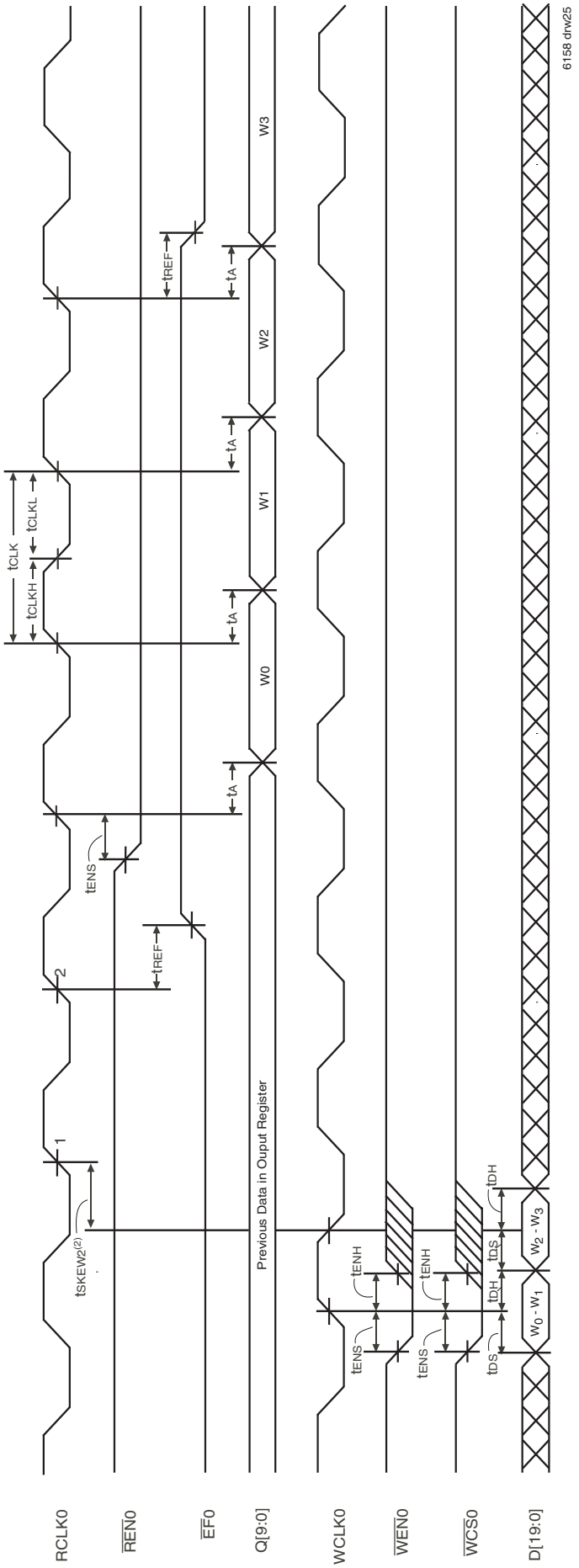
Figure 18. Read Cycle, Output Enable and Empty Flag Timing (Quad mode, IDT Standard mode, SDR to SDR)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibits the same behavior.
2. t_{SKEW2} is the minimum time between a falling WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{EF}0$ will go HIGH (after one RCLK0 cycle plus t_{REF}). If the time between the falling edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW2}, then $\overline{EF}0$ deassertion may be delayed one extra RCLK0 cycle. (See Table 6 - T_{SKEW} measurement)
3. $\overline{REN}0$ = LOW, and $\overline{RCS}0$ = LOW.
4. First data word latency = $t_{SKEW2} + 1*T_{RCLK} + t_{REF}$.
5. RCLK0 must be free running for $\overline{EF}0$ to update.
6.

MD	W	OW	WDDR	RDDR	FWFT/SI
1	D/C	D/C	1	1	0

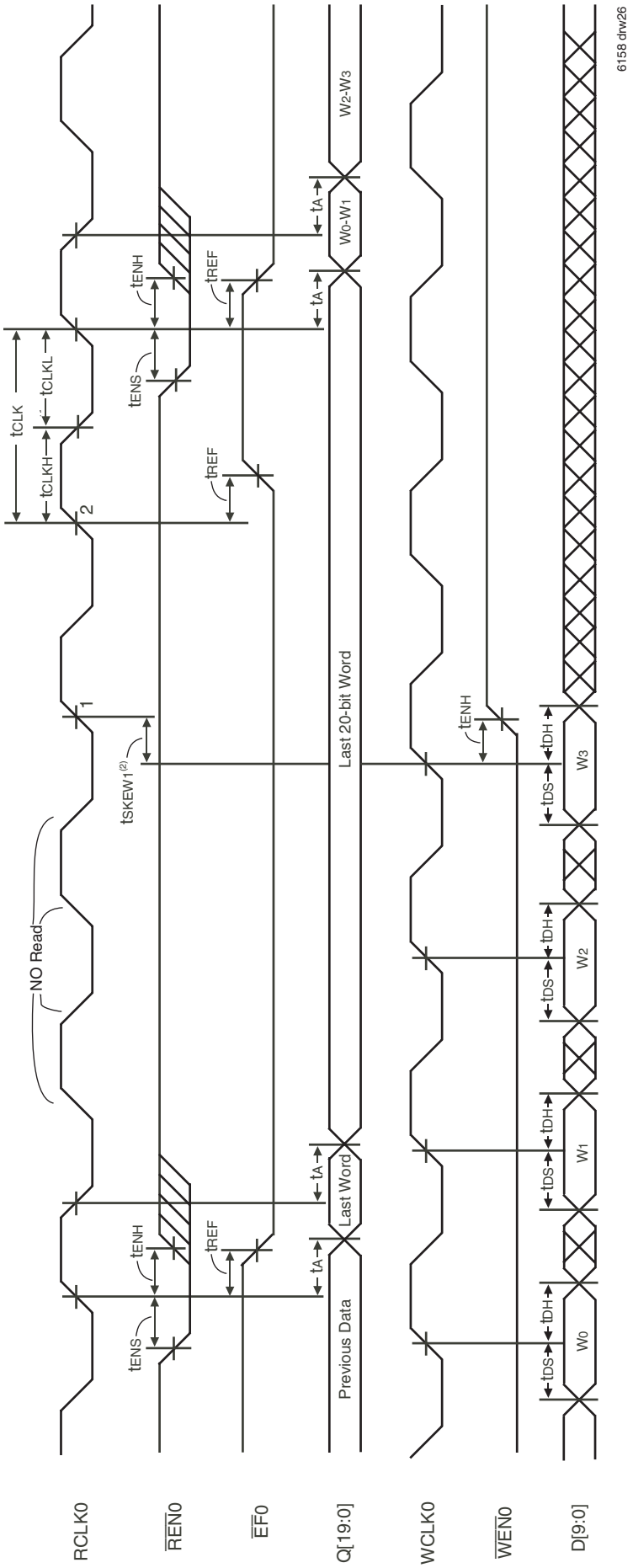
Figure 19. Read Cycle, Output Enable and Empty Flag Timing (Quad mode, IDT Standard mode, DDR to DDR)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO 2 exhibits the same behavior.
2. t_{SKEW2} is the minimum time between a falling WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{EF}0$ will go HIGH (after one RCLK0 cycle plus t_{REF}). If the time between the falling edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW2}, then $\overline{EF}0$ deassertion may be delayed one extra RCLK0 cycle. (See Table 6 - T_{SKEW} measurement).
3. $\overline{REN}0$ = LOW, and $\overline{RCS}0$ = LOW.
4. First data word latency = t_{SKEW1} + 1*T_{RCLK} + t_{REF}.
5. RCLK0 must be free running for $\overline{EF}0$ to update.
6.

MD	W	OW	WDDR	RDDR	FWFT/SI
0	1	0	1	0	0

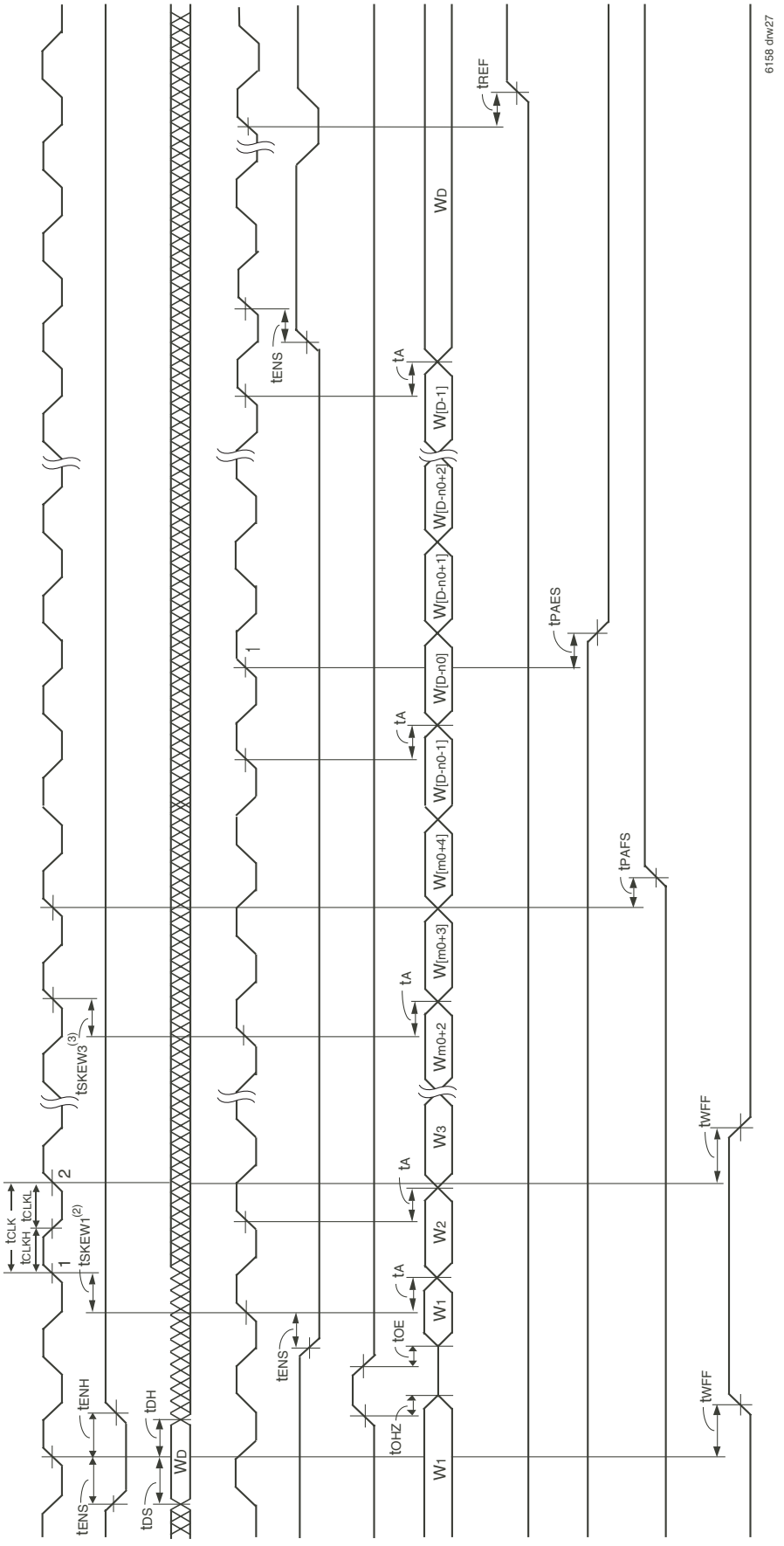
Figure 20. Read Cycle and Empty Flag Timing (Dual mode, IDT Standard mode, DDR to SDR, x20 In to x10 Out)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO 2 exhibits the same behavior.
2. t_{SKEW1} is the minimum time between a rising WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{EF}0$ will go HIGH (after one RCLK0 cycle plus t_{REF}). If the time between the rising edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW1}, then $\overline{EF}0$ deassertion may be delayed one extra RCLK0 cycle. (See Table 6 - T_{SKEW} measurement).
3. $\overline{OE}0$ = LOW, $\overline{RCS}0$ = LOW, and $\overline{WCS}0$ = LOW.
4. First data word latency = t_{SKEW1} + 1*T_{RCLK} + t_{REF}.
5. RCLK0 must be free running for $\overline{EF}0$ to update.
6.

MD	W	OW	WDDR	RDDR	FWFT/SI
0	0	1	0	1	0

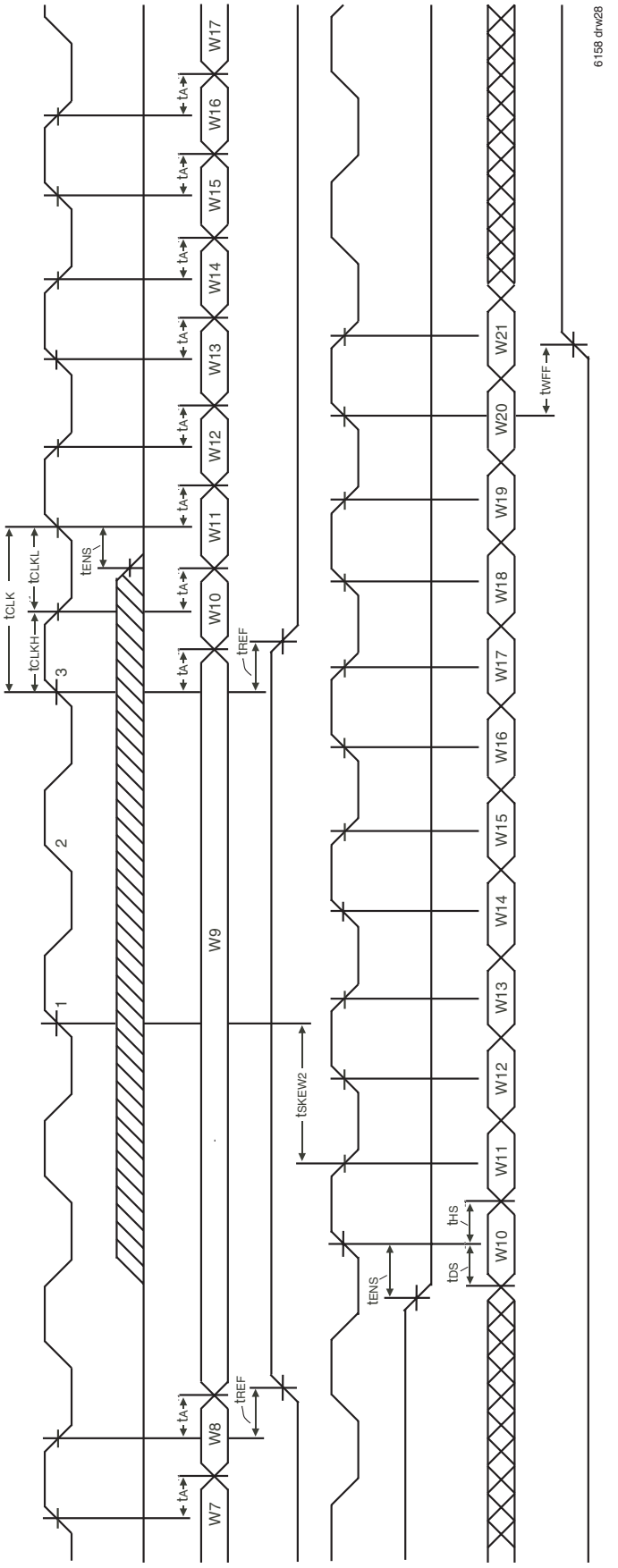
Figure 21. Read Cycle and Empty Flag Timing (Dual mode, IDT Standard mode, SDR to DDR, x10 In to x20 Out)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. t_{SKEW1} is the minimum time between a rising WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{OR}$0 will go LOW after two RCLK0 cycles plus t_{REF}. If the time between the rising edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW1}, then $\overline{OR}$0 assertion may be delayed one extra RCLK0 cycle.
3. t_{SKEW3} is the minimum time between a rising WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{PAE}$0 will go HIGH after one RCLK0 cycle plus t_{PAES}. If the time between the rising edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW3}, then the $\overline{PAE}$0 deassertion may be delayed one extra RCLK0 cycle.
4. $\overline{OE}$0 = LOW, and $\overline{WCS}$ = LOW.
5. n0 = $\overline{PAE}$0 offset, m0 = $\overline{PAF}$0 offset and D = maximum FIFO depth.
6. First data word latency = t_{SKEW1} + 2*T_{RCLK} + t_{REF}.
7.

MD	W	OW	WDDR	RDDR	FWFT/SI	PFM
1	D/C	D/C	0	0	1	1

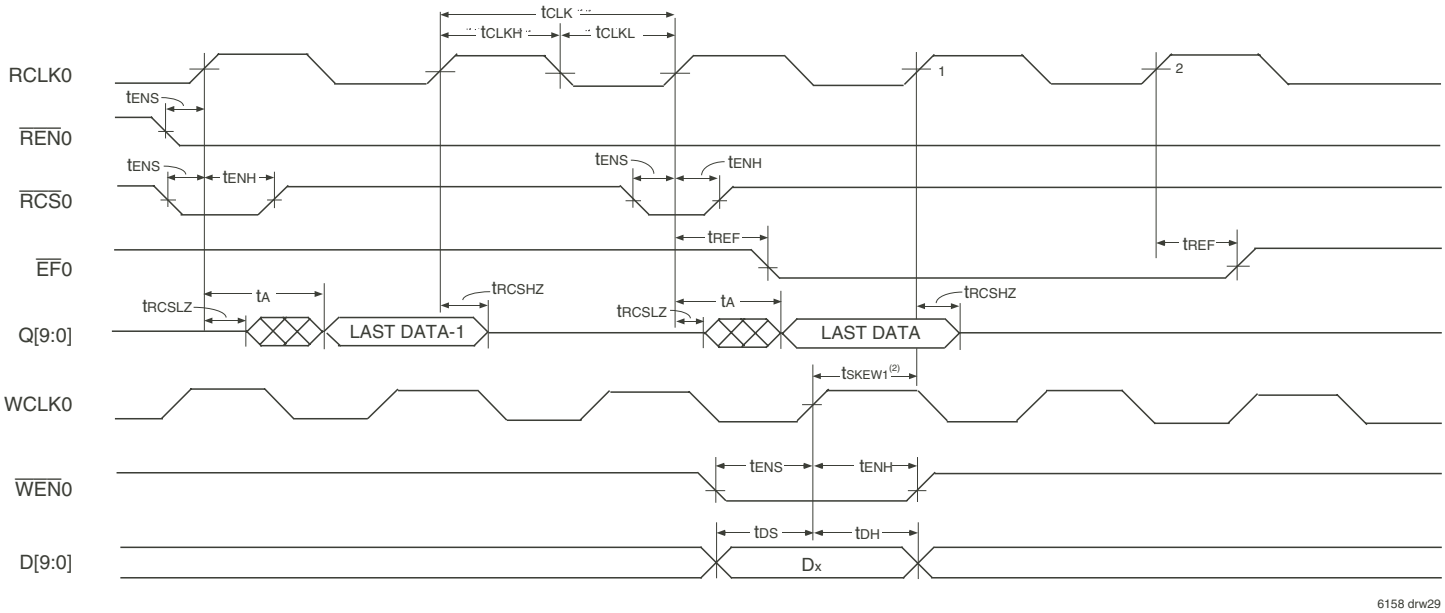
Figure 22. Read Timing and Output Ready Flag (Quad mode, FWFT mode, SDR to SDR)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. t_{SKEW2} is the minimum time between a falling WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{OR}0$ will go LOW after two RCLK0 cycles plus t_{REF}. If the time between the falling edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW2}, then $\overline{OR}0$ assertion may be delayed one extra RCLK0 cycle. (See Table 6 - T_{SKEW} measurement).
3. $\overline{OE}0$ = LOW.
4. RCLK0 must be free running for $\overline{OR}0$ to update.
5.

MD	W	OW	WDDR	RDDR	FWFT/SI
1	D/C	D/C	1	1	1

Figure 23. Read Timing and Output Ready Timing (Quad mode, FWFT mode, DDR to DDR)

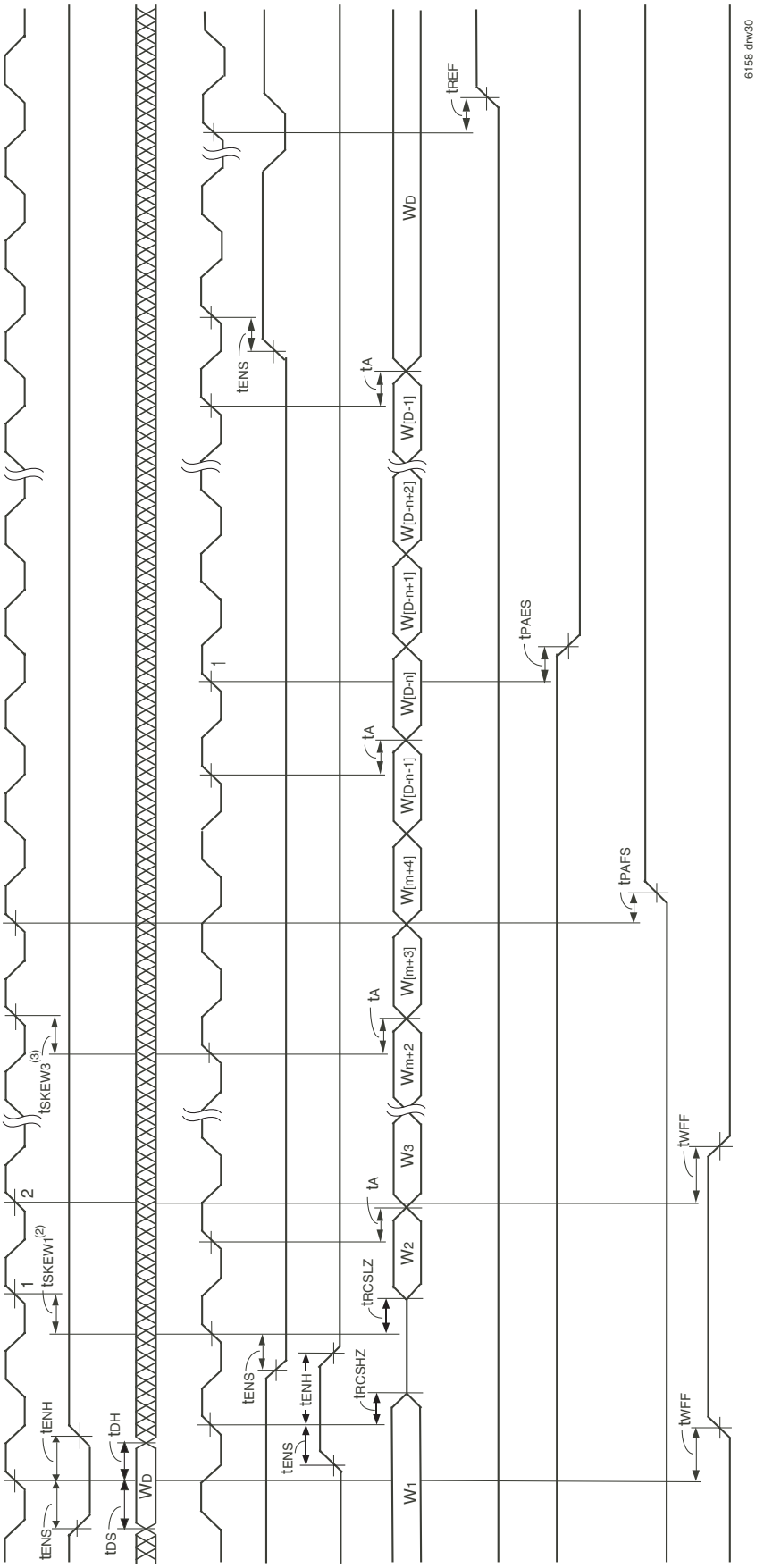


NOTES:

1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. t_{SKEW1} is the minimum time between a rising WCLK0 edge and a rising RCLK0 edge to guarantee that $\overline{EF}0$ will go HIGH (after one RCLK0 cycle plus t_{REF}). If the time between the rising edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW1}, then $\overline{EF}0$ deassertion may be delayed one extra RCLK0 cycle.
3. First data word latency = t_{SKEW1} + 1*T_{RCLK} + t_{REF}.
4. $\overline{OE}0$ = LOW.
5. RCLK0 must be free running for $\overline{EF}0$ to update.
6.

MD	IW	OW	WDDR	RDDR	FWFT/SI
1	D/C	D/C	0	0	0

Figure 24. Read Cycle and Read Chip Select (Quad mode, IDT Standard mode, SDR to SDR)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. t_{SKEW1} is the minimum time between a rising RCLK0 edge and a rising WCLK0 edge to guarantee that $\overline{IR}0$ will go LOW after one WCLK0 cycle plus t_{WFF}. If the time between the rising edge of RCLK0 and the rising edge of WCLK0 is less than t_{SKEW1}, then the $\overline{IR}0$ assertion may be delayed one extra WCLK0 cycle.
3. t_{SKEW3} is the minimum time between a rising RCLK0 edge and a rising WCLK0 edge to guarantee that $\overline{PAF}0$ will go HIGH after one WCLK0 cycle plus t_{PAFS}. If the time between the rising edge of RCLK0 and the rising edge of WCLK0 is less than t_{SKEW3}, then the $\overline{PAF}0$ deassertion may be delayed one extra WCLK0 cycle.
4. n0 = $\overline{PAE}0$ Offset, m0 = $\overline{PAF}0$ offset and D = maximum FIFO depth.
5. $\overline{OE}$ = LOW.
6. RCLK0 must be free running for $\overline{EF}0$ to update.
7.

MD	MW	OW	WDDR	RDDR	PFM	FWFT/SI
1	D/C	D/C	0	0	1	1

Figure 25. Read Cycle and Read Chip Select Timing (Quad mode, FWFT mode, SDR to SDR)

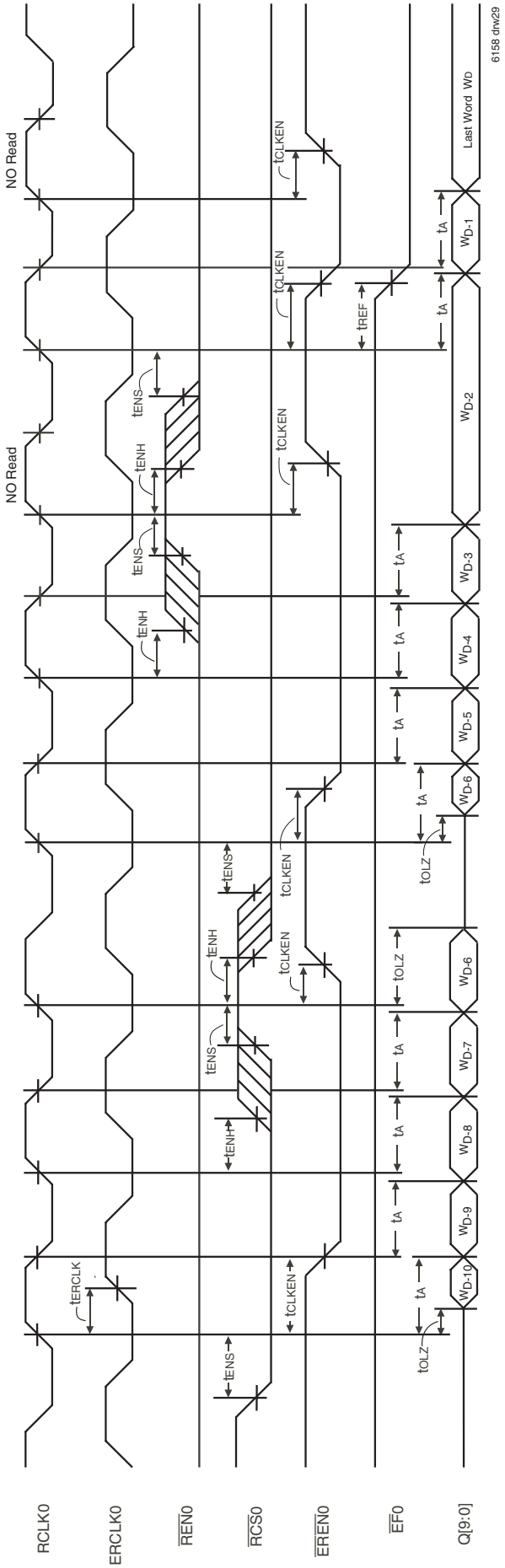
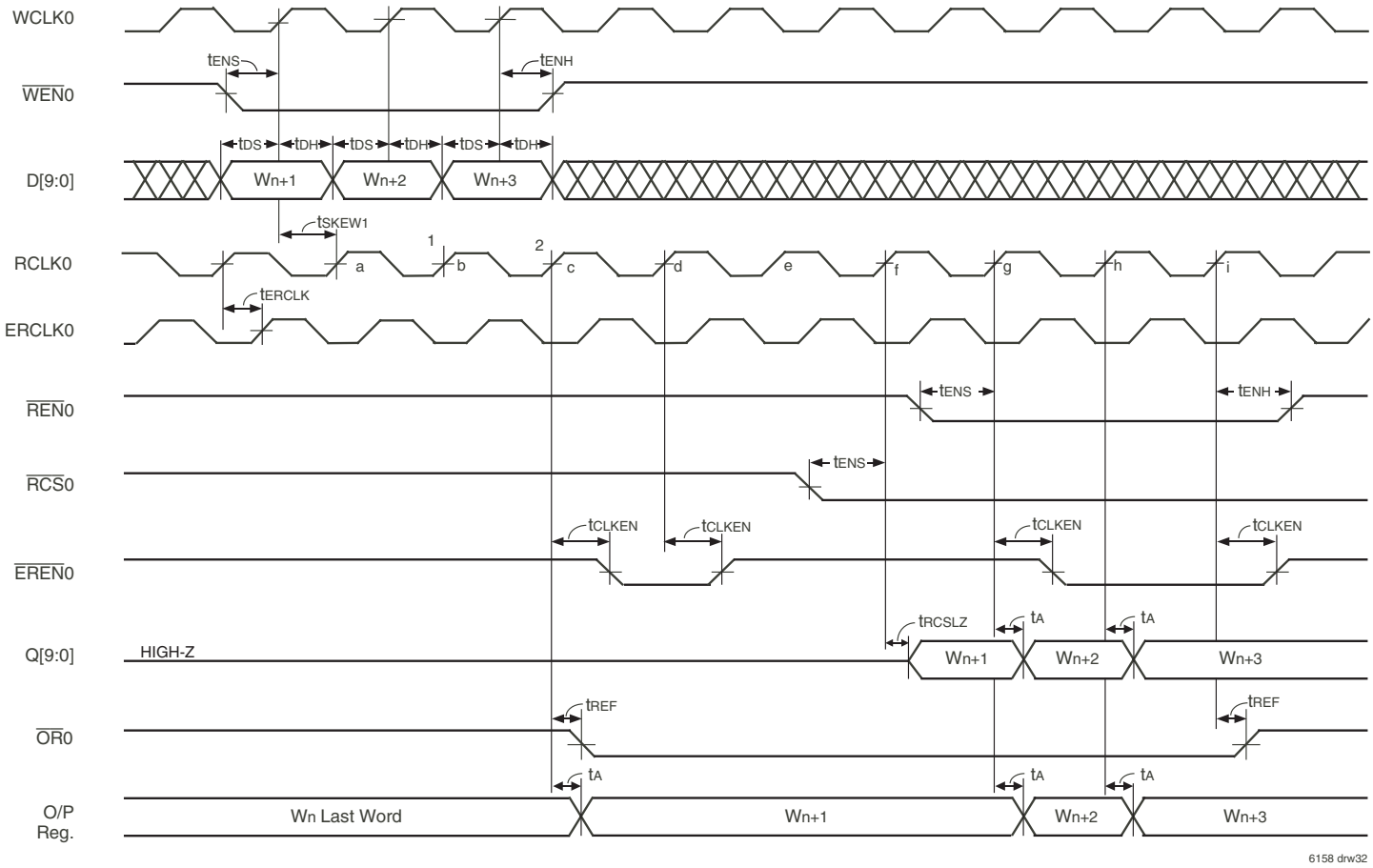


Figure 26. Echo Read Clock and Read Enable Operation (Quad mode, IDT Standard mode, DDR to DDR)

NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. The $\overline{EREN0}$ output is LOW if $\overline{RCS0}$ and $\overline{REN0}$ are LOW on the rising RCLK0 edge provided that the FIFO is not empty. If the FIFO is empty, $\overline{EREN0}$ will go HIGH to indicate that there is no new word available.
3. The $\overline{EREN0}$ output is synchronous to RCLK0.
4. $\overline{OE0}$ = LOW.
5.

MD	W	OW	WDDR	RDDR	FWFT/SI
1	D/C	D/C	1	1	0



NOTE:

1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. The O/P Register is the internal output register. Its contents are available on the Qn output bus only when $\overline{RCS0}$ and $\overline{OE0}$ are both active, LOW, that is the bus is not in High-Impedance state.
3. $\overline{OE0}$ is LOW.

Cycle:

a&b. At this point the FIFO is empty, $\overline{OR0}$ is HIGH.
$\overline{RCS0}$ and $\overline{REN0}$ are both disabled, the output bus is High-Impedance.

c. Word Wn+1 falls through to the output register, $\overline{OR0}$ goes active, LOW.
$\overline{RCS0}$ is HIGH, therefore the Qn outputs are High-Impedance. $\overline{EREN0}$ goes LOW to indicate that a new word has been placed on the output register.

d. $\overline{EREN0}$ goes HIGH, no new word has been placed on the output register on this cycle.

e. No Operation.

f. $\overline{RCS0}$ is LOW on this cycle, therefore the Qn outputs go to Low-Impedance and the contents of the output register (Wn+1) are made available.
NOTE: In FWFT mode is important to take $\overline{RCS0}$ active LOW at least one cycle ahead of $\overline{REN0}$, this ensures the word (Wn+1) currently in the output register is made available for at least one cycle.

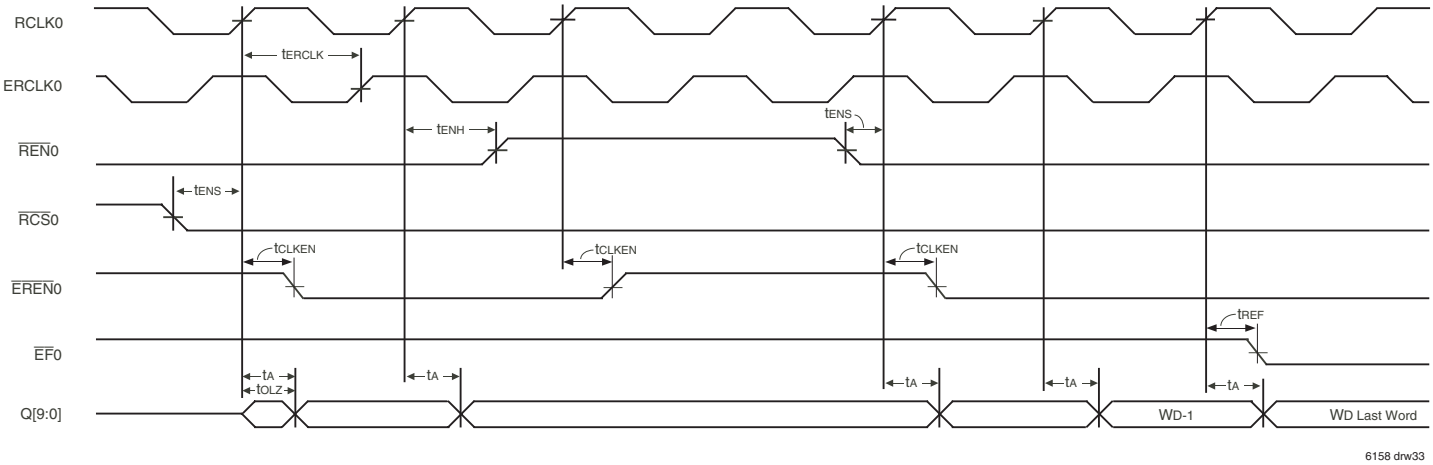
g. $\overline{REN0}$ goes active LOW, this reads out the second word, Wn+2.
$\overline{EREN0}$ goes active LOW to indicate a new word has been placed into the output register.

h. Word Wn+3 is read out, $\overline{EREN0}$ remains active, LOW indicating a new word has been read out.
NOTE: Wn+3 is the last word in the FIFO.

i. This is the next enabled read after the last word, Wn+3 has been read out. $\overline{OR0}$ flag goes HIGH and $\overline{EREN0}$ goes HIGH to indicate that there is no new word available.

4. $\overline{OE0}$ is LOW, WDDR = LOW, and RDDR = LOW.

Figure 27. Echo RCLK and Echo Read Enable Operation (Quad mode, FWFT mode, SDR to SDR)

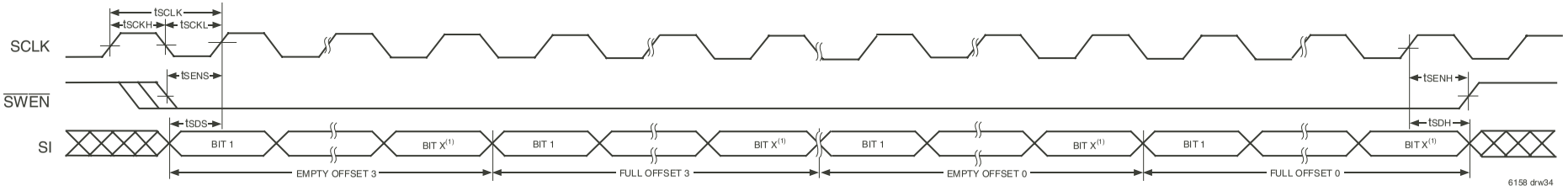


NOTES:

1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. The EREN0 output is LOW if RCS0 and REN0 are LOW on the rising RCLK0 edge provided that the FIFO is not empty. If the FIFO is empty, EREN0 will go HIGH to indicate that there is no new word available.
3. The EREN0 output is synchronous to RCLK0.
4. OE0 = LOW.
5.

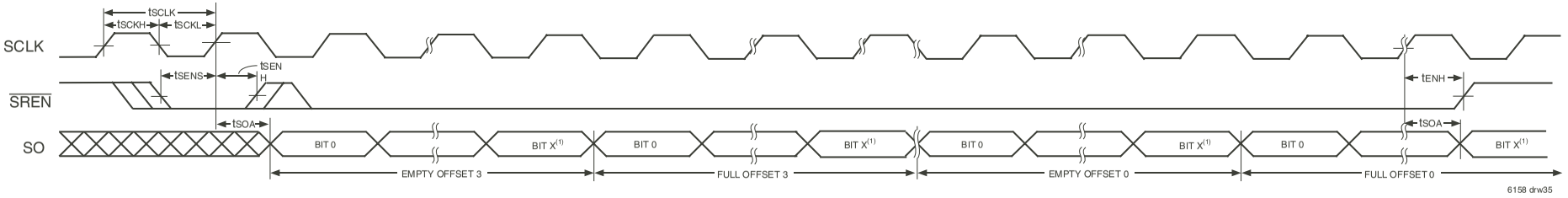
MD	IW	OW	WDDR	RDDR	FWFT/SI
1	D/C	D/C	0	0	0

Figure 28. Echo Read Clock and Read Enable Operation (Quad mode, IDT Standard mode, SDR to SDR)



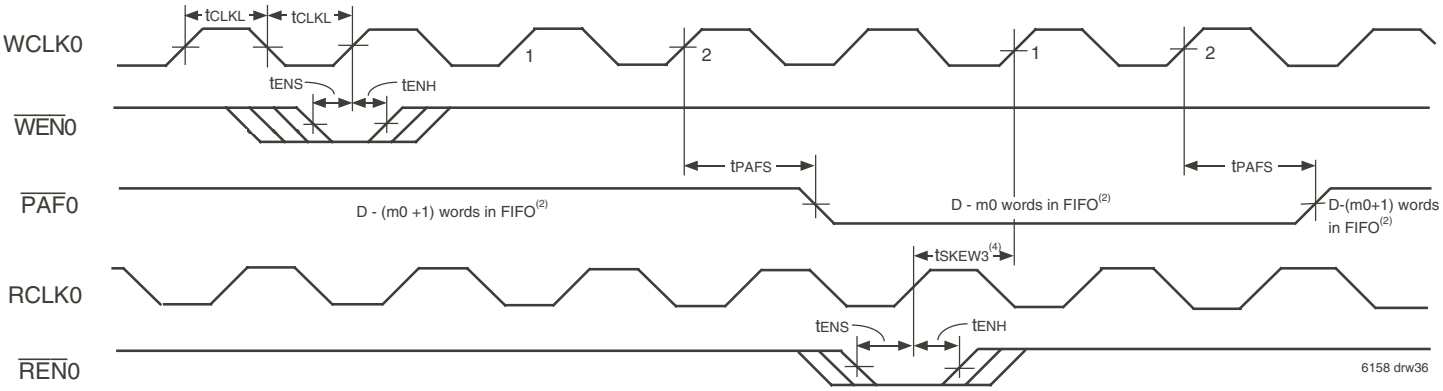
NOTES:
1. See Table 2 - Default Programming Flag Offsets for the values of x.
2. See Figure 4 - Offset Register Serial Bit Sequence for data sequence information.

Figure 29. Loading of Programmable Flag Registers (IDT Standard and FWFT modes)



NOTES:
1. See Table 2 - Default Programming Flag Offsets for the values of x.
2. See Figure 3 - Offset Register Serial Bit Sequence for data sequence information.

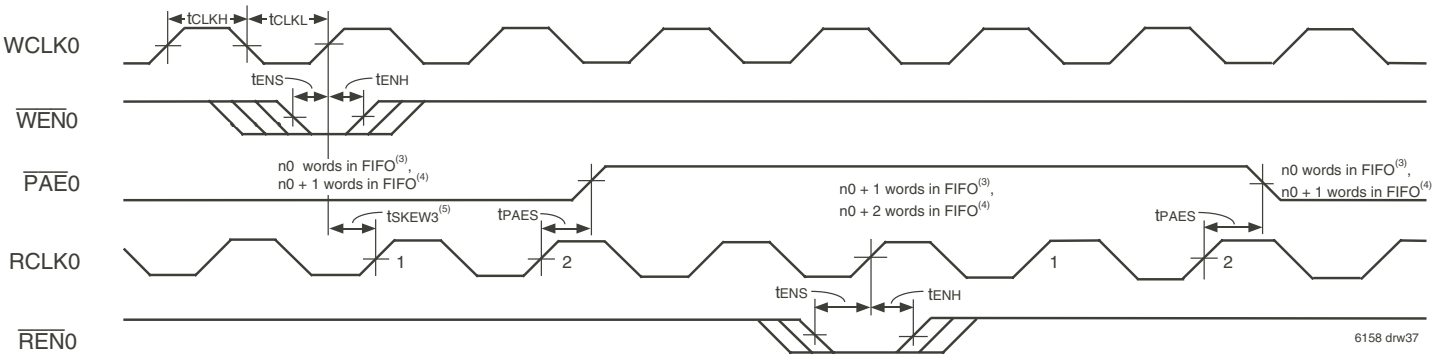
Figure 30. Reading of Programmable Flag Registers (IDT Standard and FWFT modes)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. m0 = PAF0 offset .
2. D = maximum FIFO depth. For density of FIFO with bus-matching, refer to the bus-matching section on page 19.
4. t_{SKEW3} is the minimum time between a rising RCLK0 edge and a rising WCLK0 edge to guarantee that PAF0 will go HIGH (after one WCLK0 cycle plus t_{PAFS}). If the time between the rising edge of RCLK0 and the rising edge of WCLK0 is less than t_{SKEW2}, then the PAF0 deassertion time may be delayed one extra WCLK0 cycle.
5. PAF0 is asserted and updated on the rising edge of WCLK0 only.
6. RCS0 = LOW, and WCS0 = LOW.
7.

MD	IW	OW	WDDR	RDDR	PFM
1	D/C	D/C	0	0	1

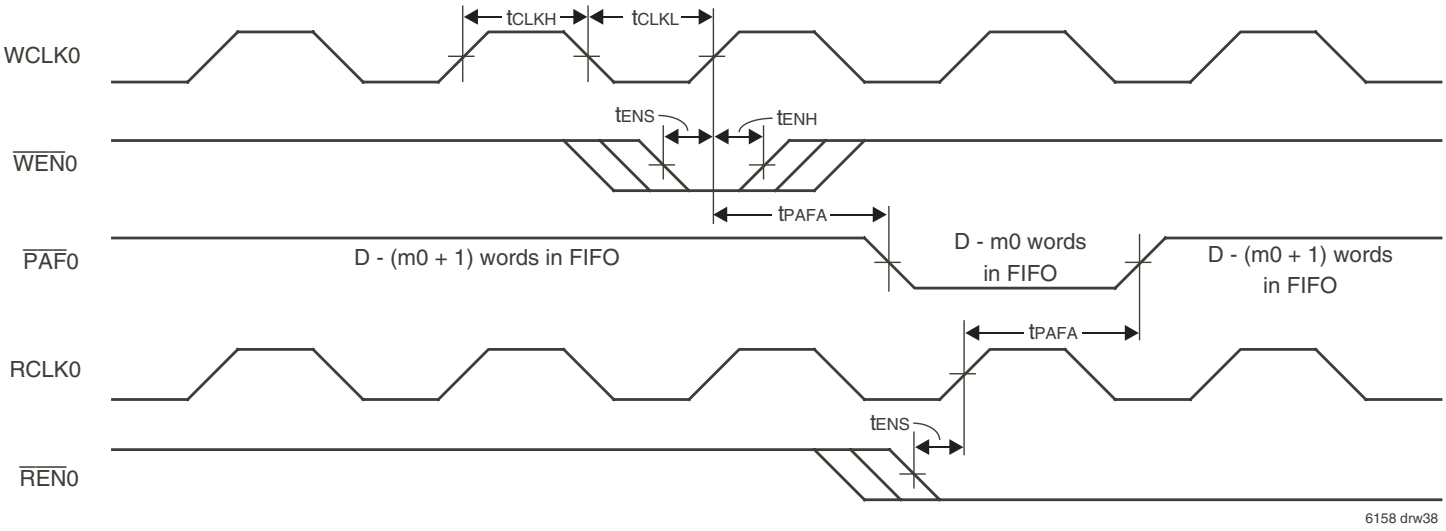
Figure 31. Synchronous Programmable Almost-Full Flag Timing (Quad mode, IDT Standard and FWFT mode, SDR to SDR)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. n0 = PAE0 offset.
3. For IDT Standard mode
4. For FWFT mode.
5. t_{SKEW3} is the minimum time between a rising WCLK0 edge and a rising RCLK0 edge to guarantee that PAE0 will go HIGH (after one RCLK0 cycle plus t_{PAES}). If the time between the rising edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW3}, then the PAE0 deassertion may be delayed one extra RCLK0 cycle.
6. PAE0 is asserted and updated on the rising edge of RCLK0 only.
7. RCS0 = LOW, and WCS0 = LOW.
8.

MD	IW	OW	WDDR	RDDR	PFM
1	D/C	D/C	0	0	1

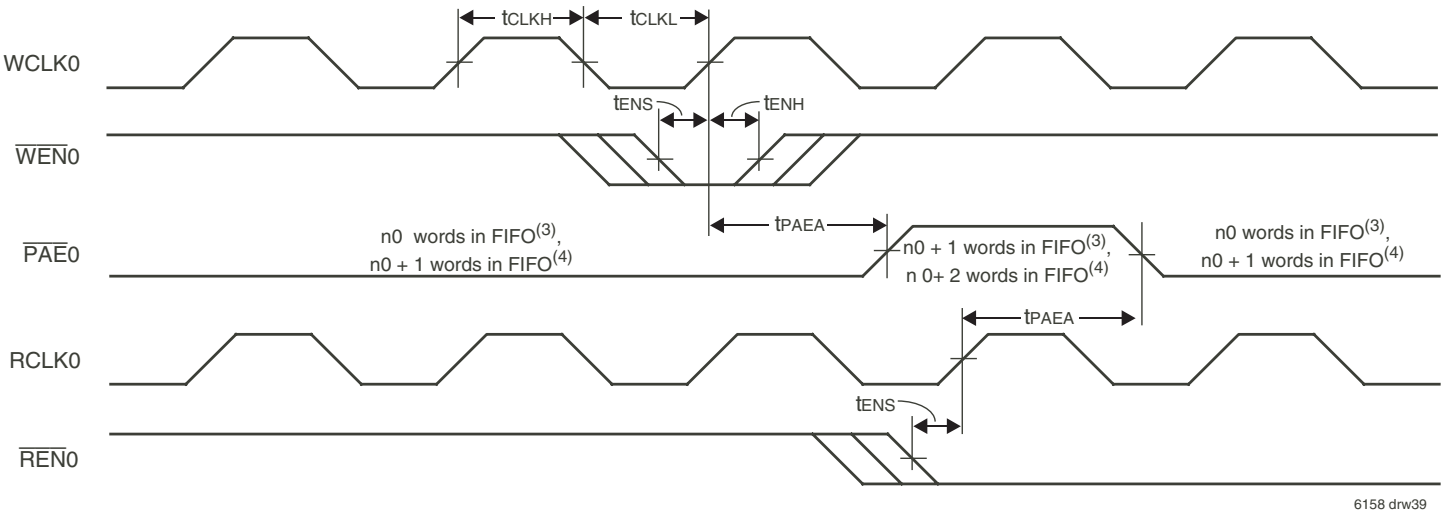
Figure 32. Synchronous Programmable Almost-Empty Flag Timing (Quad mode, IDT Standard and FWFT mode, SDR to SDR)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. m0 = $\overline{PAF}$0 offset.
3. D = maximum FIFO depth. For density of FIFO with bus-matching, refer to the bus-matching section on page 19.
4. $\overline{PAF}$0 is asserted to LOW on WCLK0 transition and reset to HIGH on RCLK0 transition.
5. $\overline{RCS}$0 = LOW, and $\overline{WCS}$0 = LOW.
6.

MD	IW	OW	WDDR	RDDR	PFM
1	D/C	D/C	0	0	0

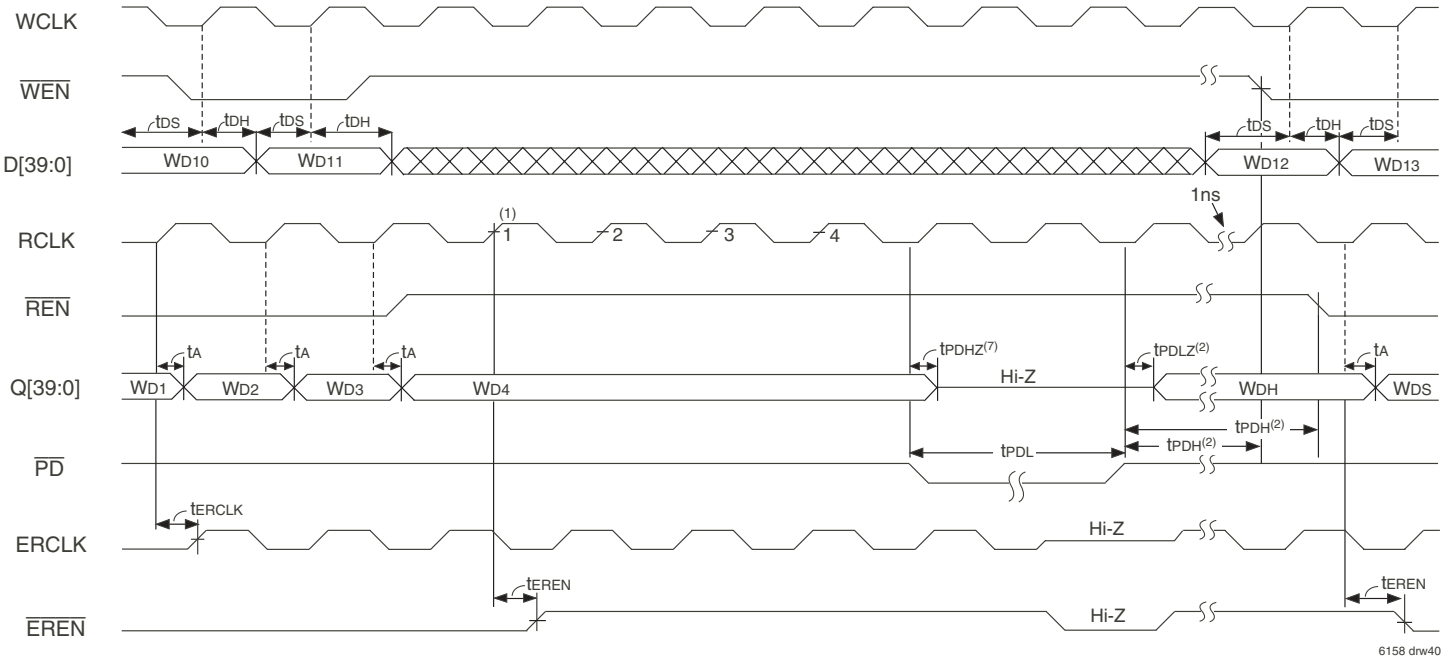
Figure 33. Asynchronous Programmable Almost-Full Flag Timing (Quad mode, IDT Standard and FWFT mode, SDR to SDR)



NOTES:
1. The timing diagram shown is for FIFO0. FIFO1-3 exhibit the same behavior.
2. n0 = $\overline{PAE}$0 offset.
3. For IDT Standard Mode.
4. For FWFT Mode.
5. $\overline{PAE}$0 is asserted LOW on RCLK0 transition and reset to HIGH on WCLK0 transition.
6. $\overline{RCS}$0 = LOW, and $\overline{WCS}$0 = LOW.
7.

MD	IW	OW	WDDR	RDDR	PFM
1	D/C	D/C	0	0	0

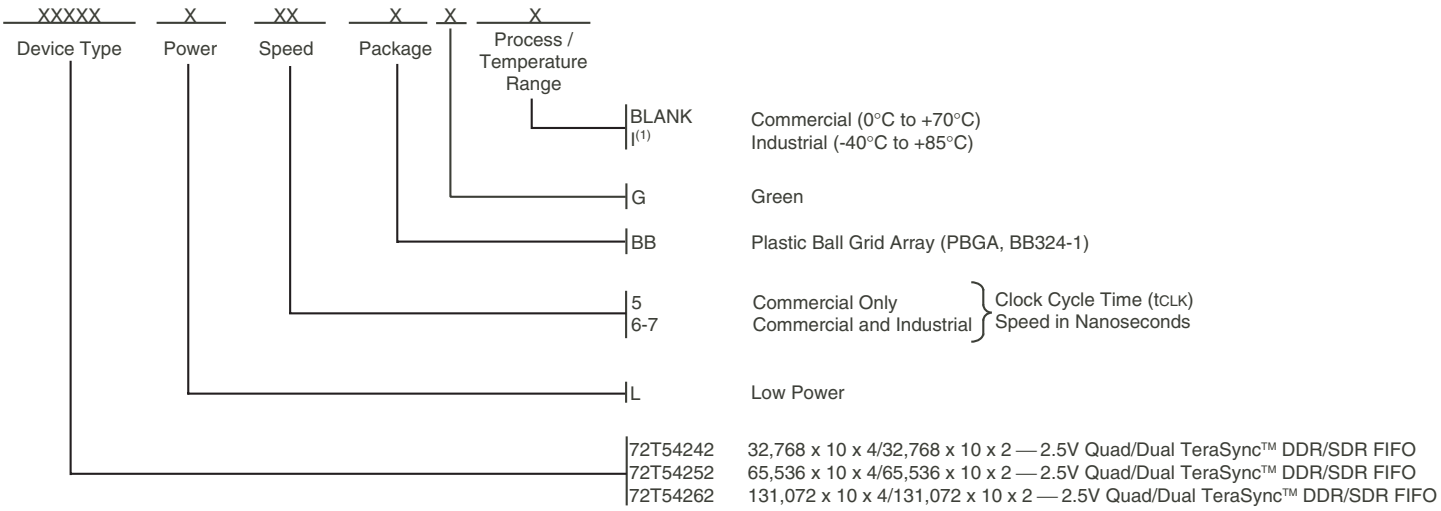
Figure 34. Asynchronous Programmable Almost-Empty Flag Timing (Quad mode, IDT Standard and FWFT mode, SDR to SDR)



NOTES:
1. All read and write operations must have ceased a minimum of 4 WCLK and 4 RCLK cycles before power down is asserted. $\overline{REN}$ and $\overline{WEN}$ must be held HIGH during this interval.
2. When the $\overline{PD}$ input becomes deasserted, there will be a 1µs waiting period before read and write operations can resume.
   All input and output signals will also resume after this time period.
3. Setup and configuration static inputs are not affected during power down.
4. Serial programming and JTAG programming port are inactive during power down.
5. $\overline{RCS}$ = 0, $\overline{WCS}$ = 0 and $\overline{OE}$ = 0. These signals can toggle during and after power down.
6. All flags remain active and maintain their current states.
7. During power down, all outputs will be in high-impedance.

Figure 35. Power Down Operation

ORDERING INFORMATION



NOTES:
1. Industrial temperature range product for the 6-7 speed grade is available as a standard device. All other speed grades available by special order.
2. Green parts available. For specific speeds contact your sales office.

DATASHEET DOCUMENT HISTORY

12/01/2003 pgs. 1, 6, 13, 27, and 30.
03/22/2005 pgs. 1, 4, 7, 12-15 and 56.
02/11/2009 pgs. 1 and 56.

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