FAIRCHILD SEMICONDUCTOR™

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74F569
4-Bit Bidirectional Counter with 3-STATE Outputs

General Description

The 74F569 is a fully synchronous, reversible counter with 3-STATE outputs. The 74F569 is a binary counter, featuring preset capability for programmable operation, carry lookahead for easy cascading, and a U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

Features

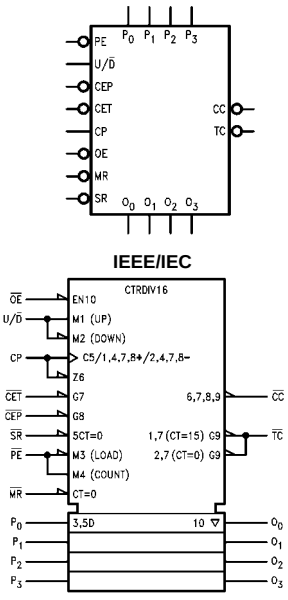
- Synchronous counting and loading
- Lookahead carry capability for easy cascading
- Preset capability for programmable operation
- 3-STATE outputs for bus organized systems

Ordering Code:

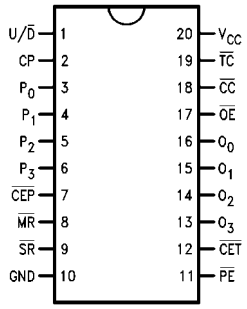
Order Number	Package Number	Package Description
74F569SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F569SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F569PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



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Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/1.0	20 µA/–1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20 µA/–1.2 mA
U/$\overline{D}$	Up/Down Count Control Input	1.0/1.0	20 µA/–0.6 mA
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{SR}$	Synchronous Reset Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
O_0–O_3	3-STATE Parallel Data Outputs	150/40(33.3)	–3 mA/24 mA (20 mA)
$\overline{TC}$	Terminal Count Output (Active LOW)	50/33.3	–1 mA/20 mA
$\overline{CC}$	Clocked Carry Output (Active LOW)	50/33.3	–1 mA/20 mA

Functional Description

The 74F569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occurs synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs—Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$) and Count Enable Trickle $\overline{CET}$)—plus the Up/Down (U/$\overline{D}$) input, determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$ and $\overline{PE}$ HIGH, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are LOW. Conversely, a HIGH signal on either $\overline{CEP}$ or $\overline{CET}$ inhibits counting.

The 74F569 uses edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or U/$\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW providing $\overline{CET}$ is LOW, when the counter reaches zero in the Down mode, or reaches maximum

(15) in the Up mode. $\overline{TC}$ will then remain LOW until a state change occurs, whether by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed. To implement synchronous multi-stage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally HIGH. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are LOW, the $\overline{CC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{CC}$ Truth Table. When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs O_0–O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces O_0–O_3 to the High Z state but does not prevent counting, loading or resetting.

Logic Equations

Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot PE$

Up: $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$

Down: $\overline{TC} = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (Down) \cdot \overline{CET}$

$\overline{CC}$ Truth Table

Inputs						Output
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$ (Note 1)	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⌐⌐	⌐⌐

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level ⌐⌐ = HIGH-to-LOW-to-HIGH Clock Transition

Note 1: $\overline{TC}$ is generated internally

Mode Select Table

Inputs						Operating Mode
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	
L	X	X	X	X	X	Asynchronous Reset
H	L	X	X	X	X	Synchronous Reset
H	H	L	X	X	X	Parallel Load
H	H	H	H	X	X	Hold
H	H	H	X	H	X	Hold
H	H	H	L	L	H	Count Up
H	H	H	L	L	L	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

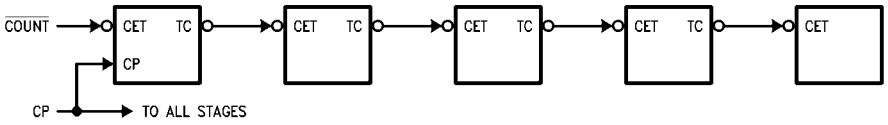


FIGURE 1. Multistage Counter with Ripple Carry

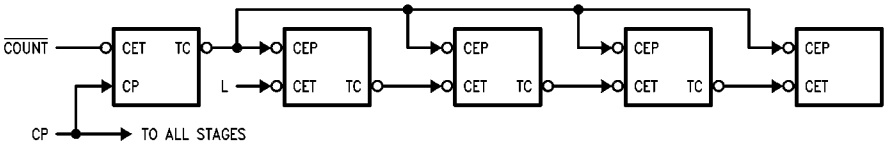
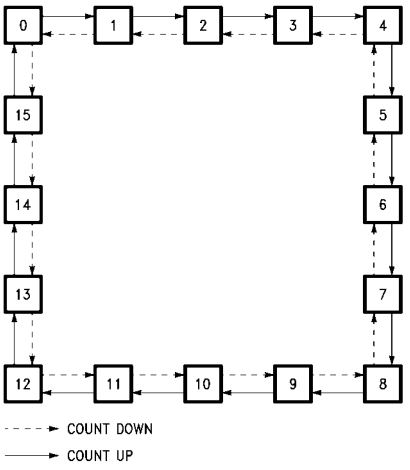
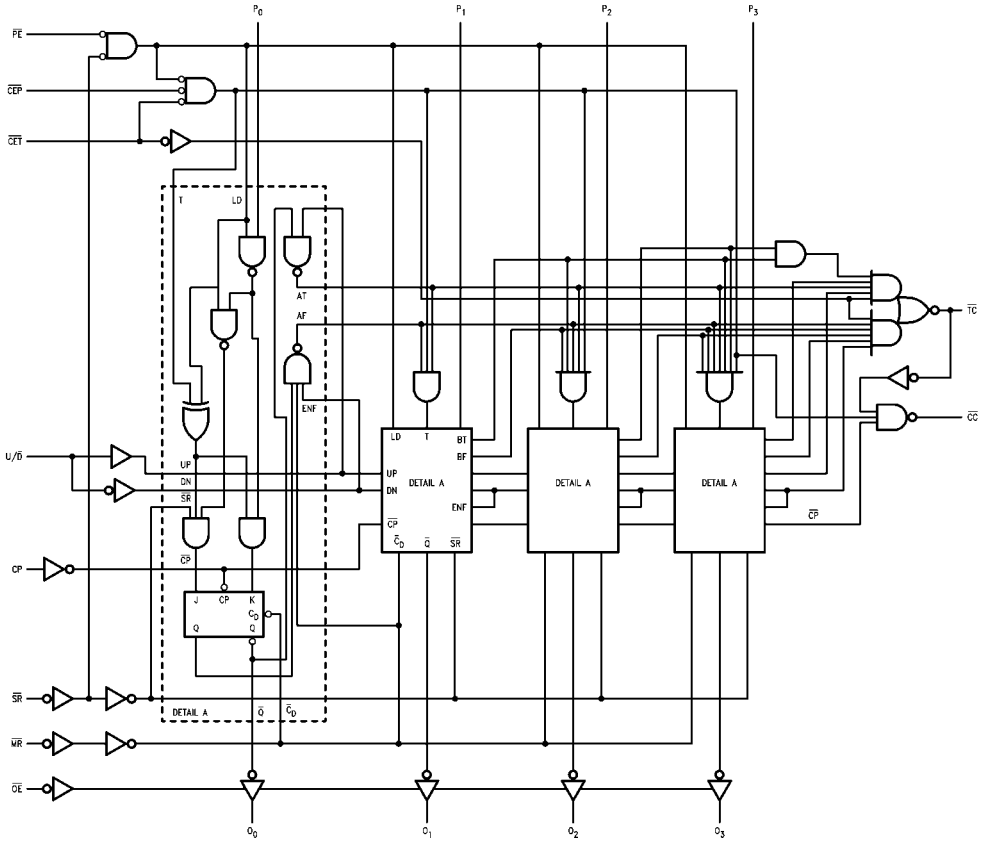


FIGURE 2. Multistage Counter with Lookahead Carry

State Diagram



Logic Diagram



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA ($\overline{TC}$, $\overline{CC}$, O_n)
	Voltage	10% V_{CC}	2.4					I_{OH} = −3 mA (O_n)
		5% V_{CC}	2.7					I_{OH} = −1 mA ($\overline{TC}$, $\overline{CC}$, O_n)
		5% V_{CC}	2.7					I_{OH} = −3 mA (O_n)
V_{OL}	Output LOW	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA ($\overline{TC}$, $\overline{CC}$)
	Voltage	10% V_{CC}			0.5			I_{OL} = 24 mA (O_n)
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC} ($\overline{TC}$, $\overline{CC}$, O_n)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (P_n, $\overline{CEP}$, CP, U/$\overline{D}$, $\overline{OE}$, $\overline{MR}$, $\overline{SR}$)
					−1.2	mA	Max	V_{IN} = 0.5V ($\overline{PE}$, $\overline{CET}$)
I_{OZH}	Output Leakage Current				50	µA	Max	V_{OUT} = 2.7V (O_n)
I_{OZL}	Output Leakage Current				−50	µA	Max	V_{OUT} = 0.5V (O_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V ($\overline{TC}$, $\overline{CC}$, O_n)
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V (O_n)
I_{CCH}	Power Supply Current			45	67	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			45	67	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			45	67	mA	Max	V_O = HIGH Z

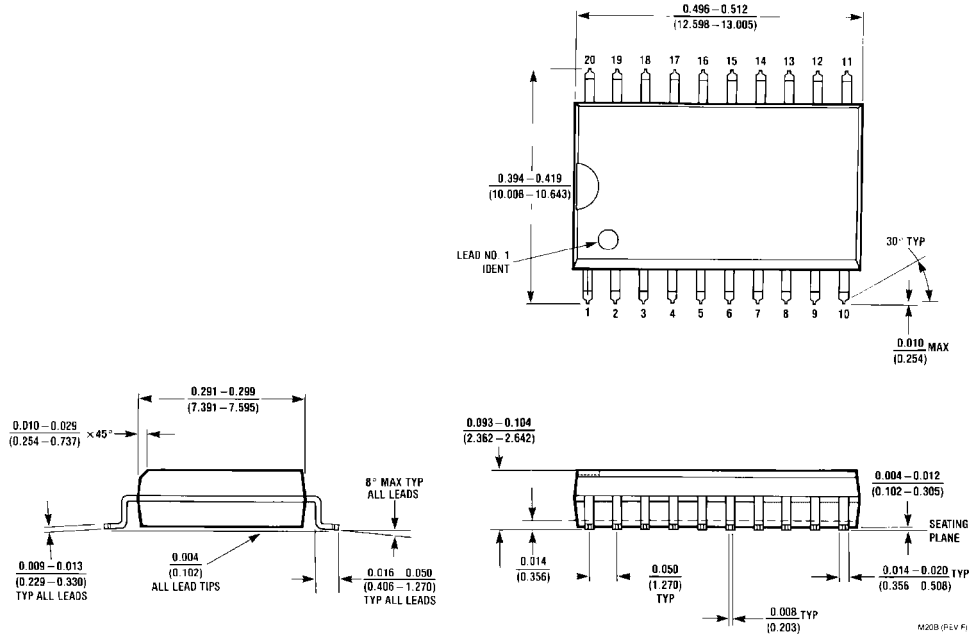
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	90			70		MHz
t_{PLH}	Propagation Delay	3.0	6.5	8.5	3.0	9.5	ns
t_{PHL}	CP to O_n ($\overline{PE}$ HIGH or LOW)	4.0	9.0	11.5	4.0	13.0	
t_{PLH}	Propagation Delay	5.5	12.0	15.5	5.5	17.5	ns
t_{PHL}	CP to $\overline{TC}$	4.0	8.5	12.5	4.0	13.0	
t_{PLH}	Propagation Delay	2.5	4.5	6.5	2.5	7.0	ns
t_{PHL}	$\overline{CET}$ to $\overline{TC}$	2.5	6.0	11.0	2.5	12.0	
t_{PLH}	Propagation Delay	3.5	8.5	11.5	3.5	12.5	ns
t_{PHL}	U/$\overline{D}$ to $\overline{TC}$	4.0	8.0	12.0	4.0	13.0	
t_{PLH}	Propagation Delay	2.5	5.5	7.0	2.0	8.0	ns
t_{PHL}	CP to $\overline{CC}$	2.0	4.5	6.0	2.0	7.0	
t_{PLH}	Propagation Delay	2.5	5.0	6.5	2.0	7.5	ns
t_{PHL}	$\overline{CEP}$, $\overline{CET}$ to $\overline{CC}$	4.0	8.5	11.0	4.0	12.5	
t_{PHL}	Propagation Delay $\overline{MR}$ to O_n	5.0	10.0	13.0	5.0	14.5	ns
t_{PZH}	Output Enable Time	2.5	5.5	8.0	2.5	8.5	ns
t_{PZL}	$\overline{OE}$ to O_n	3.0	6.0	9.0	3.0	10.0	
t_{PHZ}	Output Disable Time	1.5	5.0	7.0	1.5	8.0	
t_{PLZ}	$\overline{OE}$ to O_n	2.0	4.5	6.0	2.0	7.0	

AC Operating Requirements

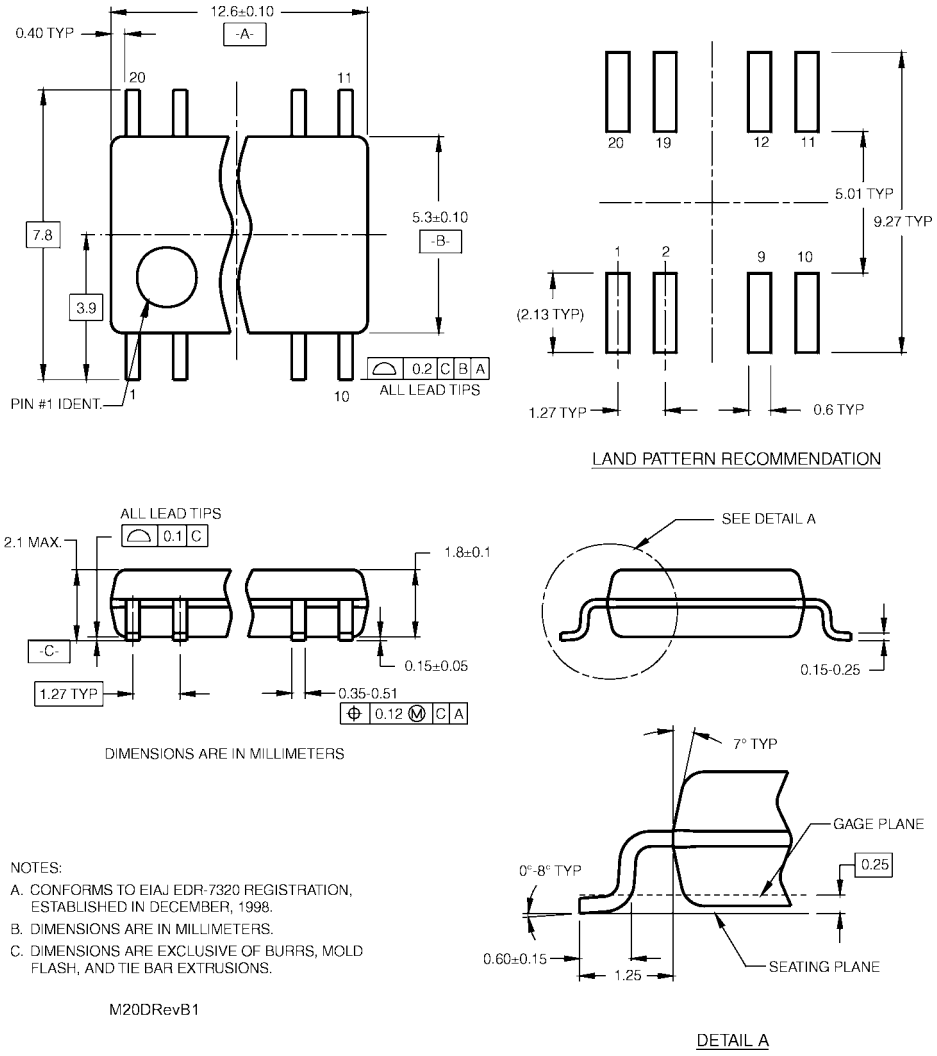
Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.0		4.5		ns
$t_S(L)$	P_n to CP	4.0		4.5		
$t_H(H)$	Hold Time, HIGH or LOW	3.0		3.5		ns
$t_H(L)$	P_n to CP	3.0		3.5		
$t_S(H)$	Setup Time, HIGH or LOW	7.0		8.0		ns
$t_S(L)$	$\overline{CEP}$ or $\overline{CET}$ to CP	5.0		6.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		ns
$t_H(L)$	$\overline{CEP}$ or $\overline{CET}$ to CP	0.5		0.5		
$t_S(H)$	Setup Time, HIGH or LOW	8.0		9.0		ns
$t_S(L)$	$\overline{PE}$ to CP	8.0		9.0		
$t_H(H)$	Hold Time, HIGH or LOW	0.0		1.0		ns
$t_H(L)$	$\overline{PE}$ to CP	0		0		
$t_S(H)$	Setup Time, HIGH or LOW	11.0		12.5		ns
$t_S(L)$	U/$\overline{D}$ to CP	7.0		8.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		ns
$t_H(L)$	U/$\overline{D}$ to CP	0		0		
$t_S(H)$	Setup Time, HIGH or LOW	10.5		11.0		ns
$t_S(L)$	$\overline{SR}$ to CP	8.5		9.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		ns
$t_H(L)$	$\overline{SR}$ to CP	0		0		
$t_W(H)$	CP Pulse Width,	4.0		4.5		ns
$t_W(L)$	HIGH or LOW	7.0		8.0		
$t_W(L)$	$\overline{MR}$ Pulse Width, LOW	4.5		6.0		ns
t_{REC}	$\overline{MR}$ Recovery Time	6.0		8.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

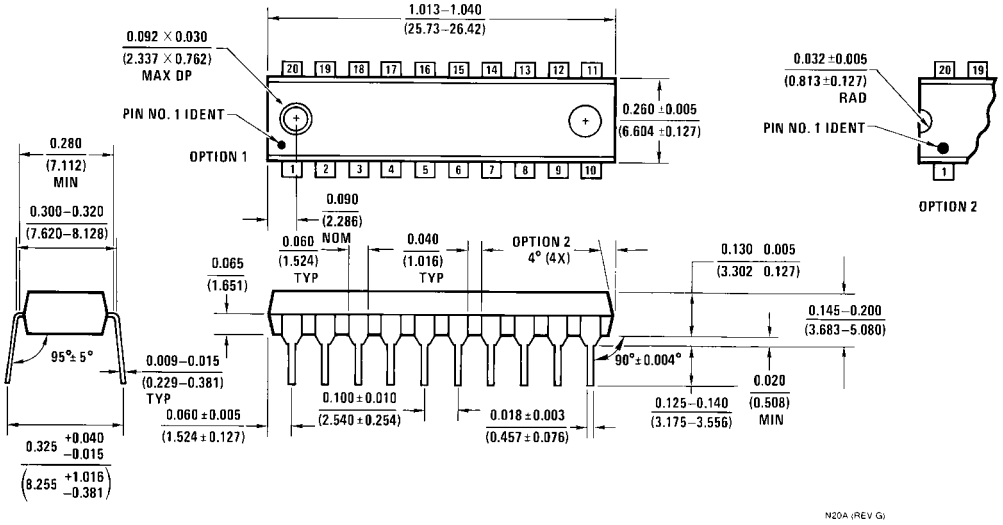
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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