

October 1987 Revised January 2004

MM74C93 4-Bit Binary Counter

General Description

The MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and $R_{02},$ and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse.

All inputs are protected against static discharge damage.

Features

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power compatibility:

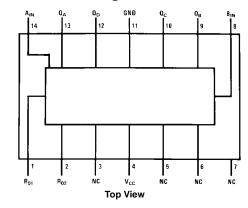
Fan out of 2 TTL driving 74L

■ The MM74C93 follows the MM74L93 Pinout

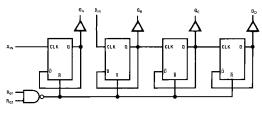
Ordering Code:

Order Number	Package Number	Package Description				
MM74C93N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide				

Connection Diagram



Logic Diagram



Truth Table

4-Bit Binary Counter Binary Count Sequence

:	Output					
Q_D	Q _C	Q_B	Q_A			
L	L	L	L			
L	L	L	Н			
L	L	Н	L			
L	L	Н	Н			
L	Н	L	L			
L	Н	L	Н			
L	Н	Н	L			
L	Н	Н	Н			
Н	L	L	L			
Н	L	L	Н			
Н	L	Н	L			
Н	L	Н	Н			
Н	Н	L	L			
Н	Н	L	Н			
Н	Н	Н	L			
Н	Н	Н	Н			
	Q _D	Q _D Q _C L	Q _D Q _C Q _B Q _C Q _B Q _C Q _C			

Output Q_A is connected to input B for binary count sequence.

- H = HIGH Level
- L = LOW Level

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Function Tables

Reset/Count Function Table

	Reset Inputs			Output				
R ₀₁	R ₀₂	R ₉₁	R ₉₂	Q_D	Q _C	Q _B	Q_A	
Н	Н	L	Х	L	L	L	L	
Н	Н	Χ	L	L	L	L	L	
X	X	Н	Н	Н	L	L	Н	
X	L	Χ	L	Count				
L	X	L	X	Count				
L	X	Χ	L	Count				
Х	L	L	Χ	Count				

Reset/Count Function Table

Reset Inputs			Out	put	
R ₀₁	R ₀₂	Q_D	Q _C	Q _B	Q_A
Н	Н	L	L	L	L
L	X	Count			
Х	L	Count			

Absolute Maximum Ratings(Note 1)

Voltage at Any Pin (Note 1) $-0.3 \text{V to V}_{CC} + 0.3 \text{V}$ Operating Temperature Range (T_A) $-55^{\circ}\text{C to} + 125^{\circ}\text{C}$

Power Dissipation (P_D)

 $\begin{array}{ccc} \text{Dual-In-Line} & 700 \text{ mW} \\ \text{Small Outline} & 500 \text{ mW} \\ \text{Operating V}_{\text{CC}} \text{ Range} & 3V \text{ to 15V} \\ \text{Absolute Maximum V}_{\text{CC}} & 18V \\ \end{array}$

Storage Temperature Range (Ts) -65° C to $+150^{\circ}$ C

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
CMOS TO	смоѕ	•				•	
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 5V	3.5			V	
		V _{CC} = 10V	8.0			V	
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 5V			1.5	V	
		V _{CC} = 10V			2.0	V	
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_{O} = -10 \mu A$	4.5			V	
		$V_{CC} = 10V$, $I_{O} = -10 \mu A$	9.0			v	
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_{O} = +10 \mu A$			0.5	V	
		$V_{CC} = 10V$, $I_{O} = +10 \mu A$			1.0	v	
I _{IN(1)}	Logical "1" Input Current	V _{CC} = 15V, V _{IN} = 15V		0.005	1.0	μΑ	
I _{IN(0)}	Logical "0" Input Current	V _{CC} = 15V, V _{IN} = 0V	-1.0	-0.005		μΑ	
I _{CC}	Supply Current	V _{CC} = 15V		0.05	300	μΑ	
CMOS/LPT	TL INTERFACE						
V _{IN(1)}	Logical "1" Input Voltage						
	MM74C90, MM74C93	V _{CC} = 4.75V	V _{CC} -1.5			V	
V _{IN(0)}	Logical "0" Input Voltage						
	MM74C90, MM74C93	$V_{CC} = 4.75V$			8.0	V	
V _{OUT(1)}	Logical "1" Output Voltage						
	MM74C90, MM74C93	$V_{CC} = 4.75V$, $I_{O} = -360 \mu A$	2.4			V	
V _{OUT(0)}	Logical "0" Output Voltage						
	MM74C90, MM74C93	$V_{CC}=4.75V,\ I_O=-360\ \mu A$			0.4	V	
OUTPUT D	RIVE (See Family Characteristics	Data Sheet) (Short Circuit Current)					
I _{SOURCE}	Output Source Current	$V_{CC} = 5V$, $V_{OUT} = 0V$	-1.75	-3.3		mA	
	(P-Channel)	T _A = 25°C	-1.75	-5.5		IIIA	
I _{SOURCE}	Output Source Current	V _{CC} = 10V, V _{OUT} = 0V	_8.0	-8.0 -15		mA	
	(P-Channel)	T _A = 25°C	-6.0				
I _{SINK}	Output Sink Current	$V_{CC} = 5V, V_{OUT} = V_{CC}$	1.75	5 3.6		mA	
	(N-Channel)	$T_A = 25^{\circ}C$	1.75	5.0		lin.	
I _{SINK}	Output Sink Current	$V_{CC} = 10V, V_{OUT} = V_{CC}$	8.0	16		mA	
	(N-Channel)	$T_A = 25^{\circ}C$	0.0	10		111/5	

AC Electrical Characteristics (Note 2)

 $T_A = 25^{\circ}C,\ C_L = 50\ \text{pF},$ unless otherwise specified

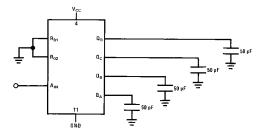
Symbol	Parameter	Conditions	Min	Тур	Max	Units	
t _{pd0} , t _{pd1}	Propagation Delay Time	V _{CC} = 5V		200	400	no	
	from A _{IN} to Q _A	V _{CC} = 10		80	150	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		450	850		
	A _{IN} to Q _B (MM74C93)	V _{CC} = 10V		160	300	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		450	800		
	A _{IN} to Q _B (MM74C90)	V _{CC} = 10V		160	300	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time	V _{CC} = 5V		500	1050	no	
	from A _{IN} to Q _C (MM74C93)	V _{CC} = 10		200	400	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		500	1000		
	A _{IN} to Q _C (MM74C93)	V _{CC} = 10V		200	400	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		600	1200		
	A _{IN} to Q _D (MM74C93)	V _{CC} = 10V		250	500	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		450	800		
	A _{IN} to Q _D (MM74C90)	V _{CC} = 10V		160	300	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		150	300		
	R_{01} or R_{02} to Q_A , Q_B , Q_C or Q_D	V _{CC} = 10V		75	150	ns	
	(MM74C93)						
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		200	400		
	R_{01} or R_{02} to Q_A , Q_B , Q_C or Q_D	V _{CC} = 10V		75	150	ns	
	(MM74C90)						
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		250	500		
	R ₉₁ or R ₉₂ to Q _A or Q _D	V _{CC} = 10V		100	200	ns	
	(MM74C90)						
t _{PW}	Min. R ₀₁ or R ₀₂ Pulse Width	V _{CC} = 5V	600	250			
	(MM74C93)	V _{CC} = 10V	30	125		ns	
t _{PW}	Min. R ₀₁ or R ₀₂ Pulse Width	V _{CC} = 5V	600	250			
	(MM74C90)	V _{CC} = 10V	300	125		ns	
t _{PW}	Min. R ₉₁ or R ₉₂ Pulse Width	V _{CC} = 5V	500	200		ns	
	(MM74C90)	V _{CC} = 10V	250	100			
t _r , t _f	Maximum Clock Rise	V _{CC} = 10V			15	μs	
	and Fall Time	V _{CC} = 10V			5		
t _W	Minimum Clock Pulse Width	V _{CC} = 5V	250	100			
		V _{CC} = 10V	100	50		ns	
f _{MAX}	Maximum Clock Frequency	V _{CC} = 5V	2			MUle	
		V _{CC} = 10V	5			MHz	
C _{IN}	Input Capacitance	Any Input (Note 3)		5		pF	
C _{PD}	Power Dissipation Capacitance	Per Package (Note 4)		45		pF	

Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

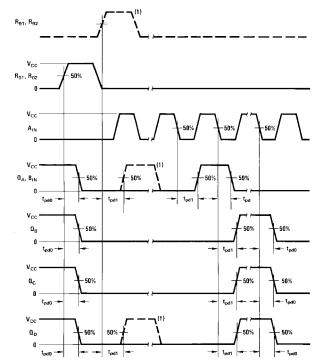
Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see Family Characteristics application note—AN-90.

AC Test Circuits



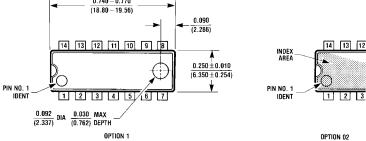
Clock rise and fall time $t_{\text{r}} = t_{\text{f}} = 20 \text{ ns}$

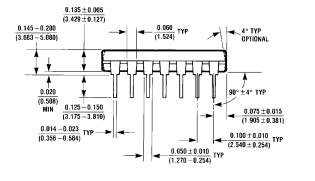
Switching Time Waveforms

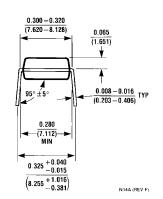


MM74C90 and MM74C93 are solid line waveforms. Dashed line waveforms are for MM74C90 only.

Physical Dimensions inches (millimeters) unless otherwise noted | - 0.740 - 0.770 / (18.80 - 19.56) | - |







14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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