

October 1987 Revised May 2002

MM74C90 • MM74C93 4-Bit Decade Counter • 4-Bit Binary Counter

General Description

The MM74C90 decade counter and the MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The 4-bit decade counter can reset to zero or preset to nine by applying appropriate logic level on the $R_{01},\,R_{02},\,R_{91}$ and R_{92} inputs. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 5 or 10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and $R_{02},$ and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse. All inputs are protected against static discharge damage.

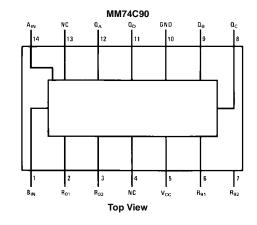
Features

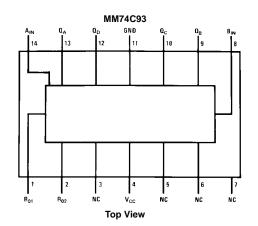
- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power compatibility: Fan out of 2 TTL driving 74L
- The MM74C93 follows the MM74L93 Pinout

Ordering Code:

Order Number	Package Number	Package Description
MM74C90N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C93N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagrams

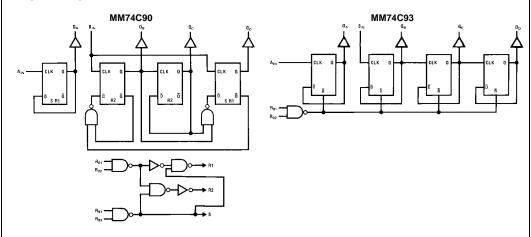




© 2002 Fairchild Semiconductor Corporation

DS005889

Logic Diagrams



Truth Tables

MM74C90 4-Bit Decade Counter BCD Count Sequence

Count	Output				
	Q_D	Q _C	Q_B	Q_A	
0	L	L	L	L	
1	L	L	L	Н	
2	L	L	Н	L	
3	L	L	Н	Н	
4	L	Н	L	L	
5	L	Н	L	Н	
6	L	Н	Н	L	
7	L	Н	Н	Н	
8	Н	L	L	L	
9	Н	L	L	Н	

Output \mathbf{Q}_{A} is connected to Input B for BCD count. H = HIGH Level L = LOW Level X = Irrelevant

MM74C93 4-Bit Binary Counter Binary Count Sequence

Count	Output				
	Q_D	Q _C	Q_B	Q_A	
0	L	L	L	L	
1	L	L	L	Н	
2	L	L	Н	L	
3	L	L	Н	Н	
4	L	Н	L	L	
5	L	Н	L	Н	
6	L	Н	Н	L	
7	L	Н	Н	Н	
8	Н	L	L	L	
9	Н	L	L	Н	
10	Н	L	Н	L	
11	Н	L	Н	Н	
12	Н	Н	L	L	
13	Н	Н	L	Н	
14	Н	Н	Н	L	
15	Н	Н	Н	Н	

Output \mathbf{Q}_A is connected to input B for binary count sequence. $\mathbf{H} = \mathbf{H} (\mathbf{G} \mathbf{H} \ \mathbf{L} \mathbf{e} \mathbf{v} \mathbf{e})$ $\mathbf{L} = \mathbf{L} \mathbf{O} \mathbf{W} \ \mathbf{L} \mathbf{e} \mathbf{v} \mathbf{e}$ $\mathbf{X} = \mathbf{I} \mathbf{r} \mathbf{r} \mathbf{e} \mathbf{e} \mathbf{v} \mathbf{a} \mathbf{t}$

Function Tables

Reset/Count Function Table

Reset Inputs					Out	put		
R ₀₁	R ₀₂	R ₉₁	R ₉₂	Q_D	Q _C	Q _B	Q_A	
Н	Н	L	Х	L	L	L	L	
Н	Н	X	L	L	L	L	L	
Х	X	Н	Н	Н	L	L	Н	
Х	L	X	L	Count				
L	X	L	Χ	Count				
L	X	X	L	Count				
Х	L	L	Χ	Count				

Reset/Count Function Table

Reset		Output			
Inputs					
R ₀₁	R ₀₂	Q _D	Q _C	Q _B	Q _A
Н	Н	L	L	L	L
L	X	Count			
Х	L	Count			

Absolute Maximum Ratings(Note 1)

Voltage at Any Pin (Note 1) -0.3V to V_{CC} +0.3V

Operating Temperature Range (T_A)

MM74C90, MM74C93 $-55^{\circ}C$ to $+125^{\circ}C$

Power Dissipation (P_D)

Dual-In-Line 700 mW Small Outline 500 mW 3V to 15V

Operating V_{CC} Range

Absolute Maximum V_{CC} 18V

Storage Temperature Range (T_S) -65°C to +150°C

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Parameter	Conditions	Min	Тур	Max	Units
CMOS	•	'			
Logical "1" Input Voltage	V _{CC} = 5V	3.5			V
	V _{CC} = 10V	8.0			v
Logical "0" Input Voltage	V _{CC} = 5V			1.5	V
	V _{CC} = 10V			2.0	v
Logical "1" Output Voltage	$V_{CC} = 5V$, $I_{O} = -10 \mu A$	4.5			V
	$V_{CC} = 10V$, $I_O = -10 \mu A$	9.0			v
Logical "0" Output Voltage	$V_{CC} = 5V$, $I_{O} = +10 \mu A$			0.5	V
	$V_{CC} = 10V$, $I_O = +10 \mu A$			1.0	v
Logical "1" Input Current	V _{CC} = 15V, V _{IN} = 15V		0.005	1.0	μА
Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μА
Supply Current	V _{CC} = 15V		0.05	300	μА
TL INTERFACE	•				
Logical "1" Input Voltage					
MM74C90, MM74C93	V _{CC} = 4.75V	V _{CC} -1.5			V
Logical "0" Input Voltage					
MM74C90, MM74C93	$V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage					
MM74C90, MM74C93	$V_{CC} = 4.75V$, $I_{O} = -360 \mu A$	2.4			V
Logical "0" Output Voltage					
MM74C90, MM74C93	$V_{CC} = 4.75V$, $I_{O} = -360 \mu A$			0.4	V
RIVE (See Family Characteristics	Data Sheet) (Short Circuit Current)				
Output Source Current	$V_{CC} = 5V$, $V_{OUT} = 0V$	1.75	2.2		mA
(P-Channel)	$T_A = 25^{\circ}C$	-1.75	-5.5		IIIA
Output Source Current	$V_{CC} = 10V, V_{OUT} = 0V$	9.0	15		mA
(P-Channel)	$T_A = 25^{\circ}C$	-0.0	-13		IIIA
Output Sink Current	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$	1 7F	3.6		mA
(N-Channel)	$T_A = 25^{\circ}C$	1.75	3.0		IIIA
Output Sink Current	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$	9.0	16		mA
(N-Channel)	$T_A = 25^{\circ}C$	0.0	10		III/A
	Logical "1" Input Voltage Logical "0" Input Voltage Logical "1" Output Voltage Logical "0" Output Voltage Logical "1" Input Current Logical "0" Input Current Supply Current TL INTERFACE Logical "1" Input Voltage MM74C90, MM74C93 Logical "0" Input Voltage MM74C90, MM74C93 Logical "0" Input Voltage MM74C90, MM74C93 Logical "0" Output Voltage MM74C90, MM74C93 Cogical "0" Output Voltage MM74C90, MM74C93 Cogical "0" Output Voltage MM74C90, MM74C93 Cogical "0" Output Voltage MM74C90, MM74C93 Coutput Source Current (P-Channel) Output Source Current (N-Channel) Output Sink Current (N-Channel) Output Sink Current	CMOS V _{CC} = 5V Logical "1" Input Voltage V _{CC} = 5V V _{CC} = 10V V _{CC} = 5V V _{CC} = 10V V _{CC} = 5V Logical "1" Output Voltage V _{CC} = 5V, I _O = −10 μA V _{CC} = 10V, I _O = −10 μA V _{CC} = 5V, I _O = +10 μA Logical "0" Output Voltage V _{CC} = 5V, I _O = +10 μA Logical "0" Input Current V _{CC} = 15V, V _{IN} = 15V Logical "0" Input Current V _{CC} = 15V, V _{IN} = 0V Supply Current V _{CC} = 15V TL INTERFACE Logical "1" Input Voltage MM74C90, MM74C93 V _{CC} = 4.75V Logical "0" Input Voltage V _{CC} = 4.75V Logical "1" Output Voltage V _{CC} = 4.75V, I _O = −360 μA Logical "0" Output Voltage V _{CC} = 4.75V, I _O = −360 μA RIVE (See Family Characteristics Data Sheet) (Short Circuit Current) Output Source Current V _{CC} = 5V, V _{OUT} = 0V (P-Channel) T _A = 25°C Output Sink Current V _{CC} = 5V, V _{OUT} = V _{CC} Output Sink Current V _{CC} = 10V, V _{OUT} = V _{CC} Output Sink Current V _{CC} = 10V, V _{OUT} = V _{CC}	CMOS Logical "1" Input Voltage $V_{CC} = 5V$ 3.5 Logical "0" Input Voltage $V_{CC} = 5V$ 8.0 Logical "1" Output Voltage $V_{CC} = 5V$ $V_{CC} = 10V$ Logical "1" Output Voltage $V_{CC} = 5V$, $I_{O} = -10 \mu A$ 9.0 Logical "0" Output Voltage $V_{CC} = 5V$, $I_{O} = +10 \mu A$ 9.0 Logical "1" Input Current $V_{CC} = 15V$, $V_{IN} = 15V$ 1.0 Logical "0" Input Current $V_{CC} = 15V$, $V_{IN} = 0V$ -1.0 Supply Current $V_{CC} = 15V$ VCC = 15V TL INTERFACE Logical "1" Input Voltage MM74C90, MM74C93 $V_{CC} = 4.75V$ $V_{CC} = 1.5$ Logical "0" Input Voltage VCC = 4.75V VCC = 1.5 MM74C90, MM74C93 $V_{CC} = 4.75V$ VCC = 1.5 Logical "0" Output Voltage VCC = 4.75V, $V_{CC} = 0.360 \mu A$ 2.4 Logical "1" Output Voltage VCC = 4.75V, $V_{CC} = 0.360 \mu A$ 2.4 Logical "0" Output Voltage VCC = 4.75V, $V_{CC} = 0.360 \mu A$ 2.4 Logical "1" Output Voltage VCC = 5.00 $V_{CC} = 0.00 \mu A$ 2.4 RIVE (See Family Characteristics Data Sheet) (Short Circuit Current) -1.75	Logical "1" Input Voltage	Logical "1" Input Voltage V _{CC} = 5V V _{CC} = 10V V _{CC} = 15V V _{CC} = 15V

AC Electrical Characteristics (Note 2)

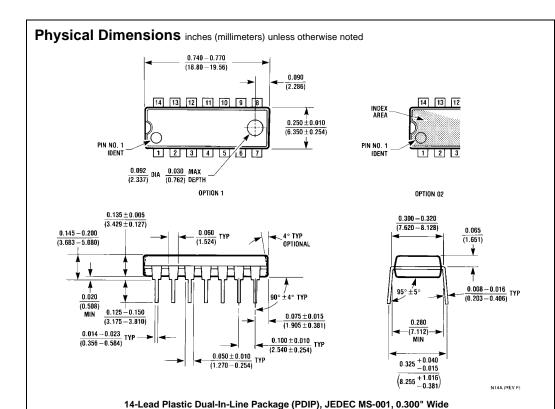
Symbol	Parameter	Conditions	Min	Тур	Max	Units	
t _{pd0} , t _{pd1}	Propagation Delay Time	V _{CC} = 5V		200	400		
	from A _{IN} to Q _A	V _{CC} = 10		80	150	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		450	850	ns	
	A _{IN} to Q _B (MM74C93)	V _{CC} = 10V		160	300		
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		450	800	ns	
	A _{IN} to Q _B (MM74C90)	V _{CC} = 10V		160	300		
t _{pd0} , t _{pd1}	Propagation Delay Time	V _{CC} = 5V		500	1050		
	from A _{IN} to Q _C (MM74C93)	V _{CC} = 10		200	400	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		500	1000		
	A _{IN} to Q _C (MM74C93)	V _{CC} = 10V		200	400	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		600	1200	no	
	A _{IN} to Q _D (MM74C93)	V _{CC} = 10V		250	500	ns	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		450	800	ns	
	A _{IN} to Q _D (MM74C90)	V _{CC} = 10V		160	300	115	
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		150	300	ne	
	R_{01} or R_{02} to Q_A , Q_B , Q_C or Q_D	V _{CC} = 10V		75	150	ns	
	(MM74C93)						
t _{pd0} , t _{pd1}	Propagation Delay Time from	V _{CC} = 5V		200	400	ns	
	R_{01} or R_{02} to Q_A , Q_B , Q_C or Q_D	V _{CC} = 10V		75	150		
	(MM74C90)						
t _{pd0} , t _{pd1}	Propagation Delay Time from	$V_{CC} = 5V$		250	500	ns	
	R_{91} or R_{92} to Q_A or Q_D	V _{CC} = 10V		100	200	113	
	(MM74C90)						
t _{PW}	Min. R ₀₁ or R ₀₂ Pulse Width	$V_{CC} = 5V$	600	250		ns	
	(MM74C93)	V _{CC} = 10V	30	125		113	
t _{PW}	Min. R ₀₁ or R ₀₂ Pulse Width	V _{CC} = 5V	600	250		ns	
	(MM74C90)	V _{CC} = 10V	300	125		113	
t _{PW}	Min. R ₉₁ or R ₉₂ Pulse Width	$V_{CC} = 5V$	500	200		ns	
	(MM74C90)	V _{CC} = 10V	250	100		110	
t _r , t _f	Maximum Clock Rise	V _{CC} = 10V			15	μs	
	and Fall Time	V _{CC} = 10V			5	μο	
t _W	Minimum Clock Pulse Width	V _{CC} = 5V	250	100		ns	
		V _{CC} = 10V	100	50		110	
f _{MAX}	Maximum Clock Frequency	V _{CC} = 5V	2			MHz	
		$V_{CC} = 10V$	5			1411 12	
C _{IN}	Input Capacitance	Any Input (Note 3)		5		pF	
C _{PD}	Power Dissipation Capacitance	Per Package (Note 4)		45		pF	

Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see Family Characteristics application note—AN-90.

MM74C90 • MM74C93 **AC Test Circuits** MM74C90 MM74C93 Clock rise and fall time $\boldsymbol{t}_{\mathrm{f}}=\boldsymbol{t}_{\mathrm{f}}=20~\mathrm{ns}$ Clock rise and fall time $t_{\rm r}=t_{\rm f}=20~{\rm ns}$ **Switching Time Waveforms** MM74C90 and MM74C93 are solid line waveforms. Dashed line waveforms are for MM74C90 only.



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and

Fairchild reserves the right at any time without notice to change said circuitry and specifications.

Package Number N14A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com