FAIRCHILD SEMICONDUCTOR™

January 1991
Revised May 2002

MM74C192 • MM74C193
Synchronous 4-Bit Up/Down Decade Counter • Synchronous 4-Bit Up/Down Binary Counter

General Description

The MM74C192 and MM74C193 up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM74C192 is a BCD counter, while the MM74C193 is a binary counter.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at a logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

Features

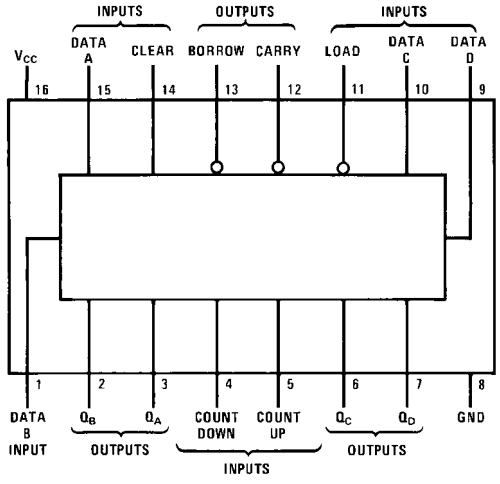
- High noise margin: 1V guaranteed
- Tenth power TTL compatible: Drive 2 LPTTL loads
- Wide supply range: 3V to 15V
- Carry and borrow outputs for N-bit cascading
- Asynchronous clear
- High noise immunity: 0.45 V_{CC} (typ.)

Ordering Code:

Order Number	Package Number	Package Description
MM74C192N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C193M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74C193N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Top View

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range (T_A)	−55°C to +125°C
Storage Temperature Range (T_S)	−65°C to +150°C
Maximum V_{CC} Voltage	18V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (T_A)	
(Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 µA V_{CC} = 10V, I_O = −10 µA	4.5 9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 µA V_{CC} = 10V, I_O = 10 µA			0.5 1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	µA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V, I_O = −100 µA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 µA			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8			mA
I_{SINK}	Output Sink Current	V_{CC} = 5V, $V_{IN(1)}$ = 5V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8			mA

AC Electrical Characteristics (Note 2)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

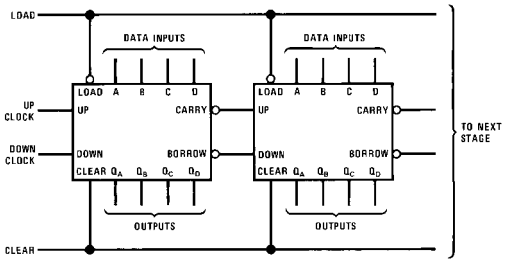
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay	$V_{CC} = 5V$		250	400	ns
	Time to Q from Count Up or Down	$V_{CC} = 10V$		100	160	
t_{pd}	Propagation Delay	$V_{CC} = 5V$		120	200	ns
	Time to Q Borrow from Count Down	$V_{CC} = 10V$		50	80	
t_{pd}	Propagation Delay	$V_{CC} = 5V$		120	200	ns
	Time to Carry from Count Up	$V_{CC} = 10V$		50	80	
t_S	Time Prior to Load	$V_{CC} = 5V$		100	160	ns
	that Data Must be Present	$V_{CC} = 10V$		30	50	
t_W	Minimum Clear Pulse Width	$V_{CC} = 5V$		300	480	ns
		$V_{CC} = 10V$		120	190	
t_W	Minimum Load Pulse Width	$V_{CC} = 5V$		100	160	ns
		$V_{CC} = 10V$		40	65	
t_{pd0}	Propagation Delay	$V_{CC} = 5V$		300	480	ns
t_{pd1}	Time to Q from Load	$V_{CC} = 10V$		120	190	
t_W	Minimum Count Pulse Width	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		35	80	
f_{MAX}	Maximum Count Frequency	$V_{CC} = 5V$	2.5	4		MHz
		$V_{CC} = 10V$	6	10		
t_r	Count Rise and Fall Time	$V_{CC} = 5V$			15	µs
t_f		$V_{CC} = 10V$			5	
C_{IN}	Input Capacitance	(Note 3)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		100		pF

Note 2: AC Parameters are guaranteed by DC correlated testing.

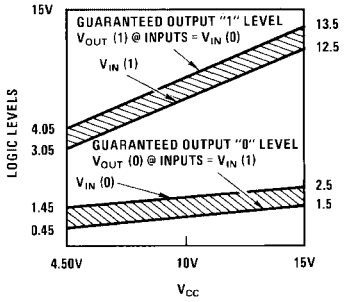
Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Application Note AN-90.

Cascading Packages

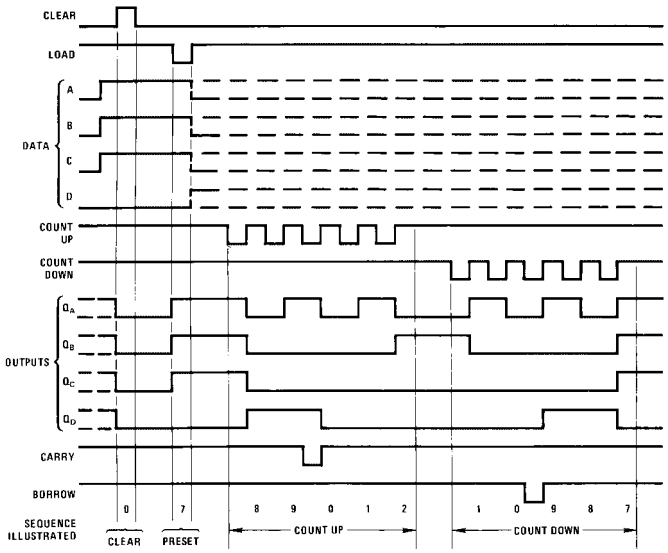


Guaranteed Noise Margin as a Function of V_{CC}



Timing Diagrams

MM74C192



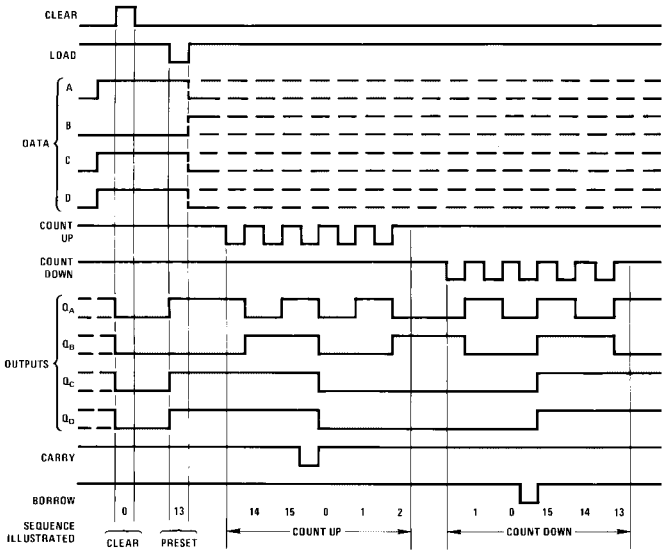
Note A: Clear outputs to zero.

Note B: Load (preset) to binary thirteen.

Note C: Count up to fourteen, fifteen, carry, zero, one and two.

Note D: Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

MM74C193



Note A: Clear outputs to zero.

Note B: Load (preset) to BCD seven.

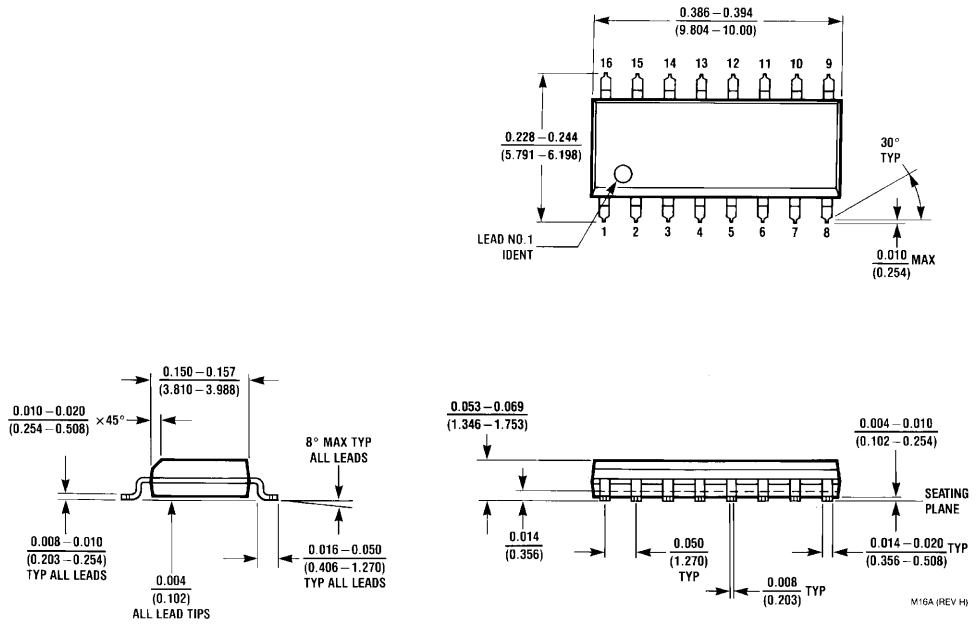
Note C: Count up to eight, nine, carry, zero, one, and two.

Note D: Count down to one, zero, borrow, nine, eight, and seven.

Note E: Clear overrides load, data, and count inputs.

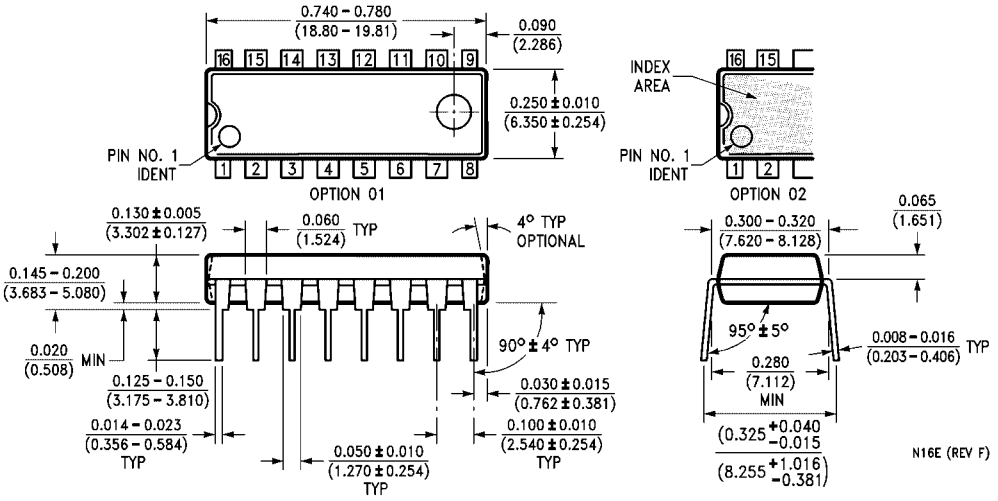
Note F: When counting up, count down input must be HIGH; when counting down, count-up input must be HIGH.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com