

16-Bit Registered Transceivers

Product Features:

Common Features:

- PI74FCT16952T, PI74FCT162952T, and PI74FCT2H952T are high-speed, low power devices with high current drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 300 mil wide plastic SSOP (V)

PI74FCT16952T Features:

- High output drive: $I_{OH} = -32 \text{ mA}$; $I_{OL} = 64 \text{ mA}$
- Power off disable outputs permit “live insertion”
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V, T_A = 25^\circ C$

PI74FCT162952T Features:

- Balanced output drivers: $\pm 24 \text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V, T_A = 25^\circ C$

PI74FCT162H952T Features:

- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull-up resistors

Product Description:

Pericom Semiconductor’s PI74FCT series of logic circuits are produced in the Company’s advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

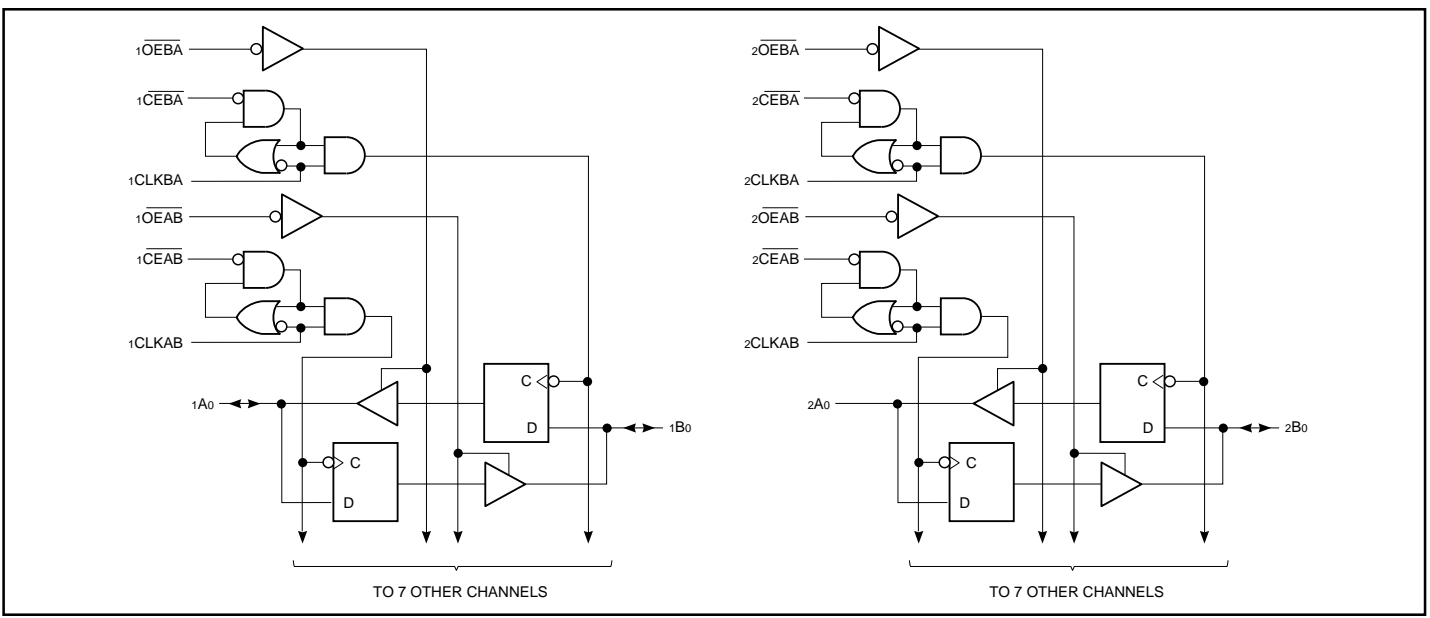
The PI74FCT16952T, PI74FCT162952T, and PI74FCT162H952T are 16-bit registered transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (\overline{xCEAB}) input must be LOW in order to enter data from xAx . The data present on the A port will be clocked on the B register when $xCLKAB$ toggles from LOW-to-HIGH. The \overline{xOEAB} control performs the output enable function on the B port. Control of data from B to A is similar, but uses the \overline{xCEBA} , $xCLKBA$, and \overline{xOEBA} inputs. By connecting the control pins of the two independent transceivers together, a full 16-bit operation can be achieved. The output buffers are designed with a Power-Off disable allowing “live insertion” of boards when used as backplane drivers.

The PI74FCT16952T output buffers are designed with a Power-Off disable function allowing “live insertion” of boards when used as backplane drivers.

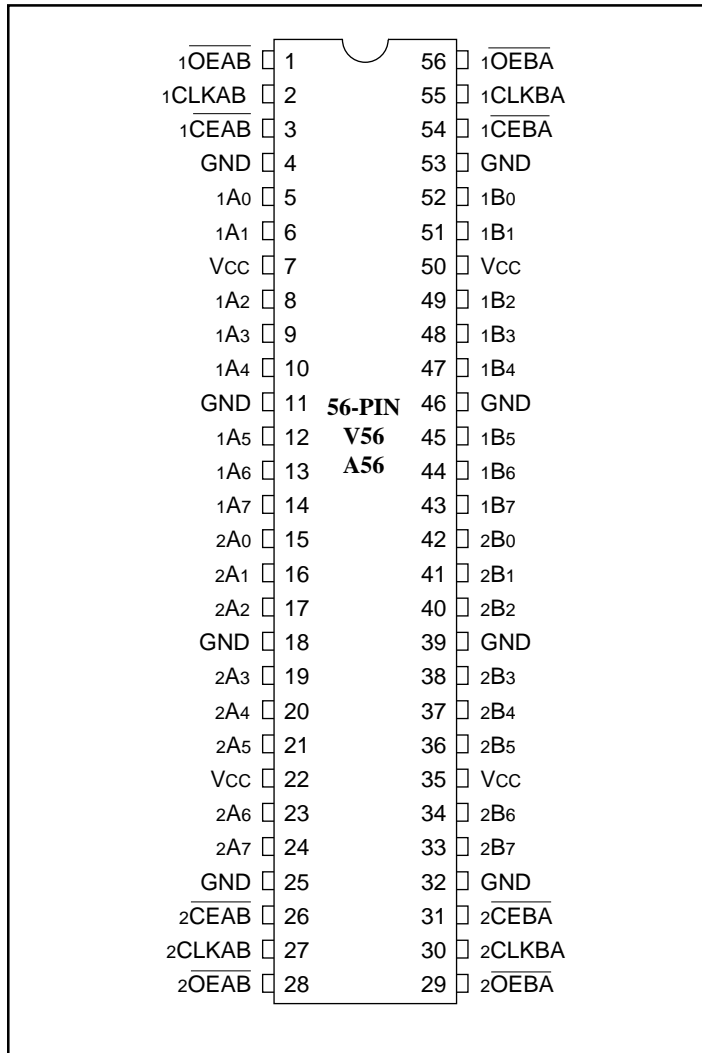
The PI74FCT162952T has $\pm 24 \text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The PI74FCT162H952T has “Bus Hold” which retains the input’s last state whenever the input goes to high-impedance preventing “floating” inputs and eliminating the need for pull-up/down resistors.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
\overline{xOEAB}	A-to-B Output Enable Input (Active LOW)
\overline{xOEBA}	B-to-A Output Enable Input (Active LOW)
\overline{xCEAB}	A-to-B Clock Enable Input (Active LOW)
\overline{xCEBA}	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
GND	Ground
Vcc	Power

Note: 1. For the PI74FCT162H952T, these pins have “Bus Hold”. All other pins are standard, outputs, or I/Os.

Truth Table^(1,2)

Inputs				Outputs
\overline{xCEAB}	xCLKAB	\overline{xOEAB}	xAx	xBx
H	X	L	X	B ⁽³⁾
X	L	L	X	B ⁽³⁾
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	High Z

- H = High Voltage Level
L = Low Voltage Level
X = Don't Care or Irrelevant
↑ = LOW-to-HIGH Transition
Z = High Impedance
- A-to-B data flow shown, B-to-A flow control is the same, except using \overline{xCEBA} , xCLKBA, and \overline{xOEBA} .
- Level of B before the indicated steady-state input conditions were established.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	Standard Input, V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IH}	Input HIGH Current	Standard I/O, V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IH}	Input HIGH Current	Bus Hold Input ⁽⁴⁾ , V _{CC} = Max.	V _{IN} = V _{CC}			±100	μA
I _{IH}	Input HIGH Current	Bus Hold I/O ⁽⁴⁾ , V _{CC} = Max.	V _{IN} = V _{CC}			±100	μA
I _{IL}	Input LOW Current	Standard Input, V _{CC} = Min.	V _{IN} = GND			-1	μA
I _{IL}	Input LOW Current	Standard I/O, V _{CC} = Min.	V _{IN} = GND			-1	μA
I _{IL}	Input LOW Current	Bus Hold Input ⁽⁴⁾ , V _{CC} = Min.	V _{IN} = GND			±100	μA
I _{IL}	Input LOW Current	Bus Hold I/O ⁽⁴⁾ , V _{CC} = Min.	V _{IN} = GND			±100	μA
I _{BHH}	Bus Hold Sustain Current	Bus Hold Input ⁽⁴⁾ , V _{CC} = Min.	V _{IN} = 2.0V	-50			μA
I _{BHL}			V _{IN} = 0.8V	+50			
I _{OZH} ⁽⁵⁾	High-Impedance	V _{CC} = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL} ⁽⁵⁾	Output Current (3-STATE OUTPUTS)	V _{CC} = Max.	V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V		-50		-180	mA
V _H	Input Hysteresis				100		mV

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. This specification does not apply to bi-directional functionalities with Bus Hold.

PI74FCT16952T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5		V
			I _{OH} = -15.0 mA	2.4	3.5		
			I _{OH} = -32.0 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64 mA		0.2	0.55	V
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V		—	—	±100	μA

PI74FCT162952T/162H952T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24 mA		0.3	0.55	V
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-150	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	500	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open x $\overline{\text{OEAB}}$ or x $\overline{\text{OEBA}}$ = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		75	120	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz (xCLKAB) 50% Duty Cycle x $\overline{\text{OEAB}}$ = x $\overline{\text{CEAB}}$ = GND x $\overline{\text{OEAB}}$ = V _{CC} One Bit Toggling f _I = 5 MHz	V _{IN} = V _{CC} V _{IN} = GND		0.8	1.7 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.3	3.2 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz (xCLKAB) 50% Duty Cycle x $\overline{\text{OEAB}}$ = x $\overline{\text{CEAB}}$ = GND x $\overline{\text{OEAB}}$ = V _{CC} 16 Bits Toggling f _I = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.8	6.5 ⁽⁵⁾	
			V _{IN} = 3.4 V _{IN} = GND		8.3	20.5 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

$$I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16952T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	16952AT		16952BT		16952CT		16952DT		16952ET		Unit	
			Com.		Com.		Com.		Com.		Com.			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	10.0	2.0	7.5	2.0	6.3	2.0	4.4	1.5	3.7	ns	
tPHL	xCLKAB, xCLKBA to xBx, xAx													
tpZH	Output Enable Time		1.5	10.5	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns	
tpZL	xOEBA, xOEAB to xAx, xBx													
tPHZ	Output Disable Time ⁽³⁾		1.5	10.0	1.5	7.5	1.5	6.5	1.5	4.0	1.5	4.0	ns	
tPLZ	xOEBA, xOEAB to xAx, xBx													
tSU	Setup Time HIGH or LOW		2.5	—	2.5	—	2.5	—	2.0	—	1.5	—	ns	
	xAx, xBx to xCLKAB, xCLKBA													
tH	Hold Time HIGH or LOW		2.0	—	2.0	—	1.5	—	1.0	—	0.0	—	ns	
	xAx, xBx to xCLKAB, xCLKBA													
tSU	Setup Time HIGH or LOW	3.0	—	3.0	—	3.0	—	2.0	—	2.0	—	ns		
	xCEAB, xCEBA to to xCLKAB, xCLKBA													
tH	Hold Time HIGH or LOW	2.0	—	2.0	—	2.0	—	1.5	—	0.0	—	ns		
	xCEAB, xCEBA to to xCLKAB, xCLKBA													
tw	Pulse Width HIGH(3) or LOW, xCLKAB or xCLKBA	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns		
Tsk(o)	OUTPUT SKEW ⁽⁴⁾	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns		

PI74FCT162952T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	16952AT		16952BT		16952CT		16952DT		16952ET		Unit	
			Com.		Com.		Com.		Com.		Com.			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	2.0	10.0	2.0	7.5	2.0	6.3	2.0	4.4	1.5	3.7	ns	
tPHL	xCLKAB, xCLKBA to xBx, xAx													
tpZH	Output Enable Time		1.5	10.5	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns	
tpZL	xOEBA, xOEAB to xAx, xBx													
tPHZ	Output Disable Time ⁽³⁾		1.5	10.0	1.5	7.5	1.5	6.5	1.5	4.0	1.5	4.0	ns	
tPLZ	xOEBA, xOEAB to xAx, xBx													
tSU	Setup Time HIGH or LOW		2.5	—	2.5	—	2.5	—	2.0	—	1.5	—	ns	
	xAx, xBx to xCLKAB, xCLKBA													
tH	Hold Time HIGH or LOW		2.0	—	2.0	—	1.5	—	1.0	—	0.0	—	ns	
	xAx, xBx to xCLKAB, xCLKBA													
tSU	Setup Time HIGH or LOW	3.0	—	3.0	—	3.0	—	2.0	—	2.0	—	ns		
	xCEAB, xCEBA to to xCLKAB, xCLKBA													
tH	Hold Time HIGH or LOW	2.0	—	2.0	—	2.0	—	1.5	—	0.0	—	ns		
	xCEAB, xCEBA to to xCLKAB, xCLKBA													
tw	Pulse Width HIGH(3) or LOW, xCLKAB or xCLKBA	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns		
Tsk(o)	OUTPUT SKEW ⁽⁴⁾	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns		

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162H952T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	16952AT		16952BT		16952CT		16952DT		16952ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay xCLKAB, xCLKBA to xBX, xAX	C _L = 50 pF R _L = 500Ω	2.0	10.0	2.0	7.5	2.0	6.3	2.0	4.4	1.5	3.7	ns
t _{PZH} t _{PZL}	Output Enable Time xOEBA, xOEAB to xAX, xBX		1.5	10.5	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
t _{PHZ} t _{PLZ}	Output Disable Time ⁽³⁾ xOEBA, xOEAB to xAX, xBX		1.5	10.0	1.5	7.5	1.5	6.5	1.5	4.0	1.5	4.0	ns
t _{SU}	Setup Time HIGH or LOW xAX, xBX to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	2.0	—	1.5	—	ns
t _H	Hold Time HIGH or LOW xAX, xBX to xCLKAB, xCLKBA		2.0	—	2.0	—	1.5	—	1.0	—	0.0	—	ns
t _{SU}	Setup Time HIGH or LOW xCEAB, xCEBA to to xCLKAB, xCLKBA		3.0	—	3.0	—	3.0	—	2.0	—	2.0	—	ns
t _H	Hold Time HIGH or LOW xCEAB, xCEBA to to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	1.5	—	0.0	—	ns
t _w	Pulse Width HIGH(3) or LOW, xCLKAB or xCLKBA		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
T _{SK(O)}	OUTPUT SKEW ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.