FAIRCHILD SEMICONDUCTOR™

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74F545
Octal Bidirectional Transceiver with 3-STATE Outputs

General Description

The 74F545 is an 8-bit, 3-STATE, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24 mA bus drive capability on the A Ports and 64 mA bus drive capability on the B Ports.

One input, Transmit/Receive ($T/\overline{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A-to-B Ports; Receive enables data from B-to-A Ports. The Output Enable input disables both A and B Ports by placing them in a 3-STATE condition.

Features

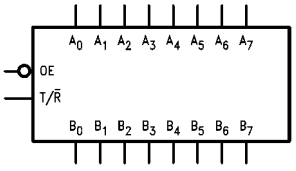
- Higher drive than 8304
- 8-bit bidirectional data flow reduces system package count
- 3-STATE inputs/outputs for interfacing with bus-oriented systems
- 24 mA and 64 mA bus drive capability on A and B Ports, respectively
- Transmit/Receive and Output Enable simplify control logic
- Guaranteed 4000V minimum ESD protection

Ordering Code:

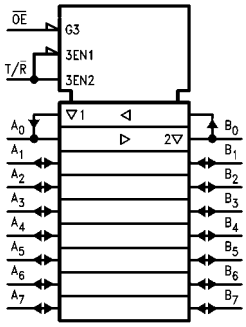
Order Number	Package Number	Package Description
74F545SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F545PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

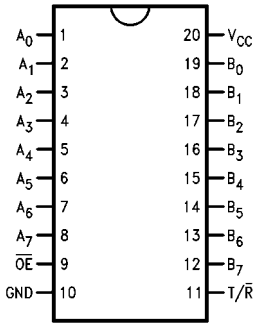
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

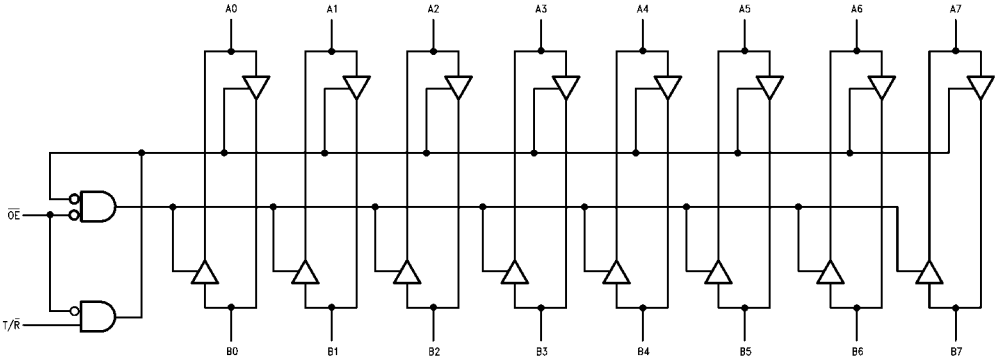
Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/2.0	20 µA/–1.2 mA
$T/\overline{R}$	Transmit/Receive Input	1.0/2.0	20 µA/–1.2 mA
A_0–A_7	Side A 3-STATE Inputs or	3.5/1.083	70 µA/–650 µA
	3-STATE Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)
B_0–B_7	Side B 3-STATE Inputs or	3.5/1.083	70 µA/–650 µA
	3-STATE Outputs	600/106.6 (80)	–12 mA/64 mA (48 mA)

Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

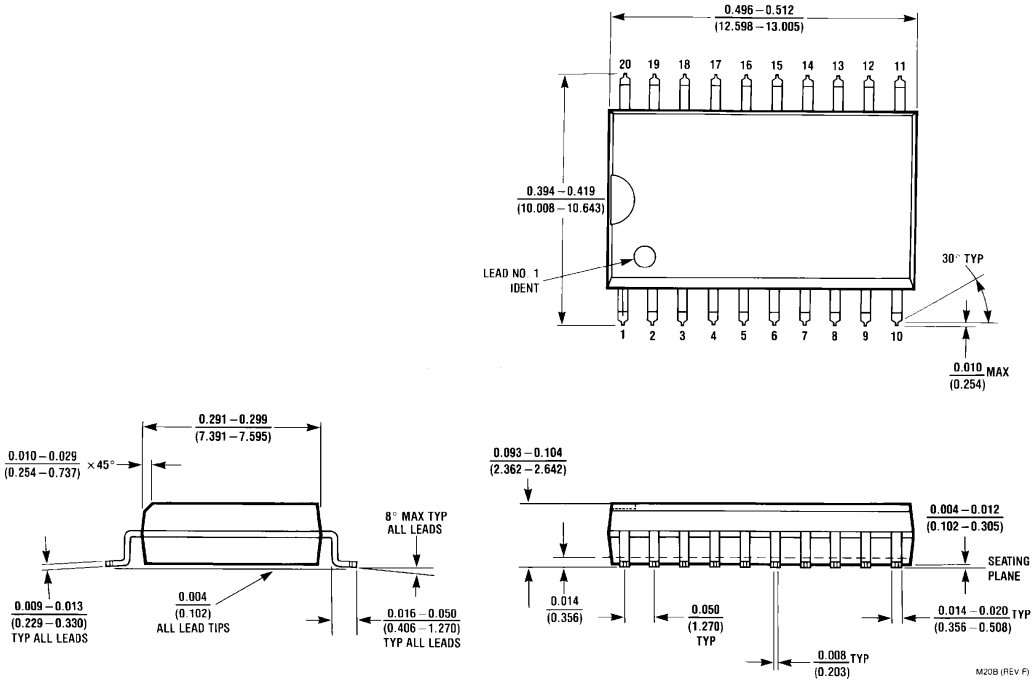
DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA ($\overline{OE}$, T/$\overline{R}$)
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (A_n)
		10% V_{CC}	2.4					I_{OH} = −3 mA (A_n)
		10% V_{CC}	2.0					I_{OH} = −15 mA (B_n)
		5% V_{CC}	2.7					I_{OH} = −1 mA (A_n)
		5% V_{CC}	2.7					I_{OH} = −3 mA (A_n)
V_{OL}	Output LOW	10% V_{CC}			0.5	V	Min	I_{OL} = 24 mA (A_n)
	Voltage	10% V_{CC}			0.55			I_{OL} = 64 mA (B_n)
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V ($\overline{OE}$, T/$\overline{R}$)
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V ($\overline{OE}$, T/$\overline{R}$)
I_{BVIT}	Input HIGH Current Breakdown (I/O)				0.5	mA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−1.2	mA	Max	V_{IN} = 0.5V ($\overline{OE}$, T/$\overline{R}$)
I_{IH} + I_{OZH}	Output Leakage Current				70	µA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	µA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V (A_n)
			−100		−225			V_{OUT} = 0V (B_n)
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			70	90	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			95	120	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			85	110	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

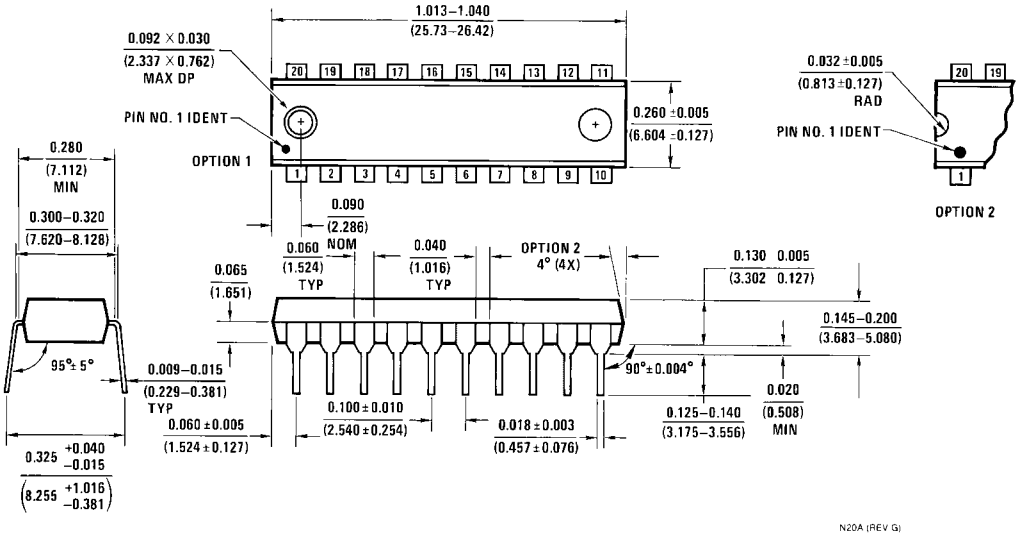
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	2.5	4.2	6.0	2.0	7.5	2.5	7.0	ns
t_{PHL}	A_n to B_n or B_n to A_n	2.5	4.6	6.0	2.0	7.5	2.5	7.0	
t_{PZH}	Output Enable Time	3.0	5.3	7.0	2.5	9.0	3.0	8.0	ns
t_{PZL}		3.5	6.0	8.0	3.0	10.0	3.5	9.0	
t_{PHZ}	Output Disable Time	3.0	5.0	6.5	2.5	9.0	3.0	7.5	
t_{PLZ}		2.0	5.0	6.5	2.0	10.0	2.0	7.5	

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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