FAIRCHILD SEMICONDUCTOR™

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GTLP16617
17-Bit TTL/GTLP Synchronous Bus Transceiver with Buffered Clock

General Description

The GTLP16617 is a 17-bit registered synchronous bus transceiver that provides TTL to GTLP signal level translation. It allows for transparent, latched and clocked modes of data flow and provides a buffered GTLP (CLKOUT) clock output from the TTL CLKAB. The device provides a high speed interface between cards operating at TTL logic levels and a backplane operating at GTLP logic levels. High speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transceiver logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is process, voltage, and temperature (PVT) compensated. Its function is similar to BTL and GTL but with different output levels and receiver threshold. GTLP output LOW level is typically less than 0.5V, the output level HIGH is 1.5V and the receiver threshold is 1.0V.

Features

- Bidirectional interface between GTLP and TTL logic levels
- Designed with edge rate control circuitry to reduce output noise on the GTLP port
- V_{REF} pin provides external supply reference voltage for receiver threshold adjustibility
- Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- TTL compatible driver and control inputs
- Designed using Fairchild advanced CMOS technology
- Bushold data inputs on the A port eliminates the need for external pull-up resistors on unused inputs.
- Power up/down and power off high impedance for live insertion
- 5 V tolerant inputs and outputs on the LVTTL port
- Open drain on GTLP to support wired-or connection
- Flow through pinout optimizes PCB layout
- D-type flip-flop, latch and transparent data paths
- A Port source/sink –32 mA/+32 mA
- GTLP Buffered CLKAB signal available (CLKOUT)

Ordering Code:

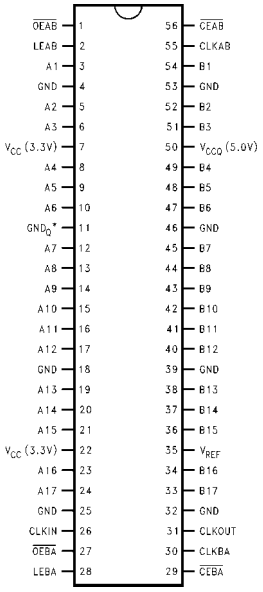
Order Number	Package Number	Package Description
GTLP16617MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
GTLP16617MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Transparent HIGH)
LEBA	B-to-A Latch Enable (Transparent HIGH)
V_{REF}	GTLP Reference Voltage
CLKAB	A-to-B Clock
CLKBA	B-to-A Clock
A1-A17	A-to-B Data Inputs or B-to-A 3-STATE Data Outputs
B1-B17	B-to-A Data Inputs or A-to-B Open Drain Outputs
CLKIN	B-to-A Buffered Clock Output
CLKOUT	GTLP Buffered Clock Output of CLKAB

Connection Diagram



Functional Description

The GTLP16617 is a 17 bit registered transceiver containing D-type flip-flop, latch and transparent modes of operation for the data path and a GTLP translation of the CLKAB signal (CLKOUT). Data flow in each direction is controlled by the clock enables ($\overline{CEAB}$ and $\overline{CEBA}$), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA) and output enables ($\overline{OEAB}$ and $\overline{OEBA}$). The clock enables ($\overline{CEAB}$ and $\overline{CEBA}$) enable all 17 data bits. The output enables ($\overline{OEAB}$ and $\overline{OEBA}$) control both the 17 bits of data and the CLKOUT/CLKIN buffered clock paths and the $\overline{OEAB}$ is synchronous with the CLKAB signal. The $\overline{OEBA}$ can not be synchronous since we are passing the clock through the device with data and we would need to generate the CLKBA signal elsewhere. It should also be noted that the $\overline{OEAB}$ register is controlled by CLKAB only, and is also not inhibited by the $\overline{CEAB}$ signal.

For A-to-B data flow, when $\overline{CEAB}$ is LOW, the device operates on the LOW-to-HIGH transition of CLKAB for the flip-flop and on the HIGH-to-LOW transition of LEAB for the latch path. That is, if $\overline{CEAB}$ is LOW and LEAB is LOW the A data is latched regardless as to the state of CLKAB (HIGH or LOW) and if LEAB is HIGH the device is in transparent mode. When $\overline{OEAB}$ is registered LOW the outputs are active. When $\overline{OEAB}$ is registered HIGH the outputs are HIGH impedance. The data flow of B-to-A is similar except that $\overline{CEBA}$, $\overline{OEBA}$, LEBA and CLKBA are used.

Truth Table

(Note 1)

Inputs					Output	Mode
$\overline{CEAB}$	$\overline{OEAB}$ (Note 2)	LEAB	CLKAB	A	B	
X	H	X	↑	X	Z (Note 3)	Latched storage
L	L	L	H	X	B_0 (Note 4)	of A data
L	L	L	L	X	(Note 5)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage
L	L	L	↑	H	H	of A data
H	L	L	X	X	B_0 (Note 5)	Clock inhibit

Note 1: A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, $\overline{CEBA}$.

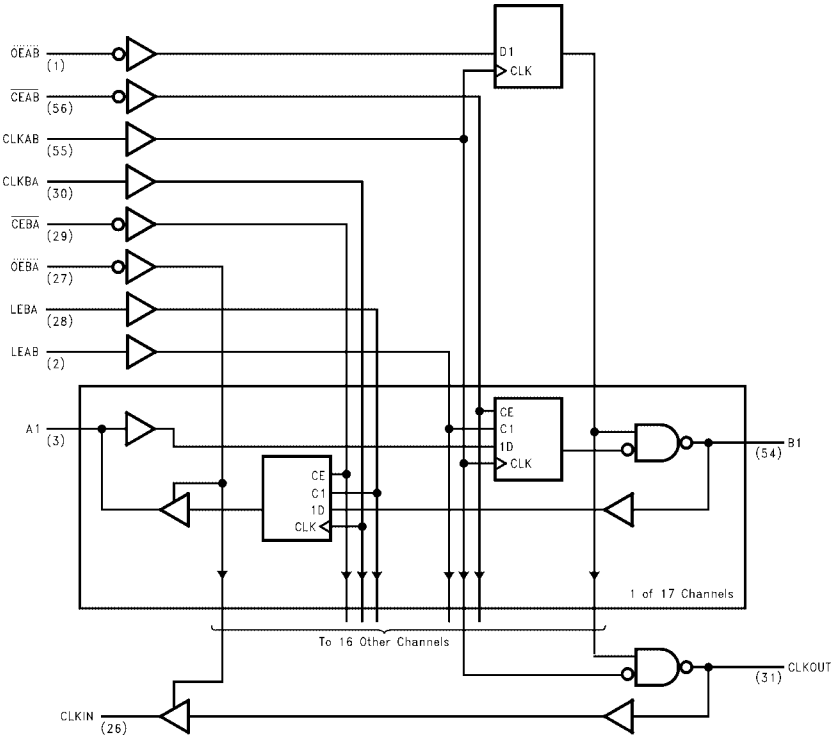
Note 2: LH edge on CLKAB is required when changing the input on $\overline{OEAB}$ pin.

Note 3: $\overline{OEAB}$ met set-up time prior to CLKAB LH transition

Note 4: Output level before the indicated steady state input conditions were established, provided CLKAB was HIGH prior to LEAB going LOW.

Note 5: Output level before the indicated steady state input conditions were established.

Logic Diagram



Absolute Maximum Ratings (Note 6)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Input Voltage (V_I)	–0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs 3-STATE	–0.5V to +7.0V
Outputs Active (Note 7)	–0.5V to V_{CC} + 0.5V
DC Output Sink Current into	
A Port I_{OL}	64 mA
DC Output Source Current from	
A Port I_{OH}	–64 mA
DC Output Sink Current	
into B Port in the LOW State, I_{OL}	80 mA
DC Input Diode Current (I_{IK})	
V_I < 0V	–50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	–50 mA
V_O > V_{CC}	+50 mA
ESD Rating	>2000V
Storage Temperature (T_{STG})	–65°C to +150°C

Recommended Operating Conditions (Note 8)

Supply Voltage V_{CC}	
V_{CC}	3.15V to 3.45V
V_{CCQ}	4.75V to 5.25V
Bus Termination Voltage (V_{TT}) GTLP	1.35V to 1.65V
Input Voltage (V_I)	
on A Port and Control Pins	0.0V to 5.5V
HIGH Level Output Current (I_{OH})	
A Port	–32 mA
LOW Level Output Current (I_{OL})	
A Port	+32 mA
B Port	+34 mA
Operating Temperature (T_A)	–40°C to +85°C

Note 6: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 7: I_O Absolute Maximum Rating must be observed.

Note 8: Unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (Unless Otherwise Noted).

Symbol		Test Conditions		Min	Typ (Note 9)	Max	Units
V_{IH}	B Port			V_{REF} +0.1		V_{TT}	V
	Others			2.0			V
V_{IL}	B Port			0.0		V_{REF} –0.2	V
	Others					0.8	V
V_{REF}	GTLP				1.0		V
	GTL				0.8		V
V_{IK}		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_I = –18 mA			–1.2	V
V_{OH}	A Port	V_{CC}, V_{CCQ} = Min to Max (Note 10)	I_{OH} = –100 µA	V_{CC} –0.2			V
		V_{CC} = 3.15V	I_{OH} = –8 mA	2.4			
		V_{CCQ} = 4.75V	I_{OH} = –32 mA	2.0			
V_{OL}	A Port	V_{CC}, V_{CCQ} = Min to Max (Note 10)	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OL} = 32 mA			0.5	
	B Port	V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OL} = 34 mA			0.65	V
I_I	Control Pins	V_{CC}, V_{CCQ} = 0 or Max	V_I = 5.5V or 0V			±10	µA
	A Port	V_{CC} = 3.45V V_{CCQ} = 5.25V	V_I = 5.5V			20	µA
			V_I = V_{CC}			1	
			V_I = 0			–30	
	B Port	V_{CC} = 3.45V V_{CCQ} = 5.25V	V_I = V_{CCQ}			5	µA
			V_I = 0			–5	
I_{OFF}	A Port and Control Pins	V_{CC} = V_{CCQ} = 0	V_I or V_O = 0 to 4.5V			100	µA
$I_{I(hold)}$	A Port	V_{CC} = 3.15V, V_{CCQ} = 4.75V	V_I = 0.8V	75			µA
			V_I = 2.0V	–20			
I_{OZH}	A Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 3.45V			1	µA
	B Port		V_O = 1.5V			5	
I_{OZL}	A Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 0			–20	µA
	B Port		V_O = 0.65V			–10	

DC Electrical Characteristics (Continued)

Symbol		Test Conditions		Min	Typ (Note 9)	Max	Units
I_{CCQ} (V_{CCQ})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, $V_I = V_{CCQ}$ or GND	Outputs HIGH		30	40	mA
			Outputs LOW		30	40	
			Outputs Disabled		30	40	
I_{CC} (V_{CC})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, $V_I = V_{CCQ}$ or GND	Outputs HIGH		0	1	mA
			Outputs LOW		0	1	
			Outputs Disabled		0	1	
ΔI_{CC} (Note 11)	A Port and Control Pins	V_{CC} = 3.45V, V_{CCQ} = 5.25V, A or Control Inputs at V_{CC} or GND	One Input at 2.7V		0	1	mA
C_{IN}	Control Pins		$V_I = V_{CCQ}$ or 0		8		pF
$C_{I/O}$	A Port		$V_I = V_{CCQ}$ or 0		9		
$C_{I/O}$	B Port		$V_I = V_{CCQ}$ or 0		6		

Note 9: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C.

Note 10: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Note 11: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted).

Symbol			Min	Max	Unit
f_{MAX}	Maximum Clock Frequency		175		MHz
t_W	Pulse Duration	LEAB or LEBA HIGH	3.0		ns
		CLKAB or CLKBA HIGH or LOW	3.2		
t_S	Setup Time	A before CLKAB↑	0.5		ns
		$\overline{OEAB}$ before CLKAB↑	1.5		
		B before CLKBA↑	3.1		
		A before LEAB↓	1.3		
		B before LEBA↓	3.7		
		$\overline{CEAB}$ before CLKAB↑	0.7		
		$\overline{CEBA}$ before CLKBA↑	1.0		
t_H	Hold Time	A after CLKAB↑	1.5		ns
		$\overline{OEAB}$ after CLKAB↑	1.0		
		B after CLKBA↑	0.0		
		A after LEAB↓	0.5		
		B after LEBA↓	0.0		
		$\overline{CEAB}$ after CLKAB↑	1.5		
		$\overline{CEBA}$ after CLKBA↑	1.7		

AC Electrical Characteristics

Over recommended range of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted).

C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 12)	Max	Unit
t_{PLH}	A	B	1.0	4.3	6.5	ns
t_{PHL}			1.0	5.0	8.2	
t_{PLH}	LEAB	B	1.8	4.5	6.7	ns
t_{PHL}			1.5	5.3	8.7	
t_{PLH}	CLKAB	B	1.8	4.6	6.7	ns
t_{PHL}			1.5	5.4	8.7	
t_{PLH}	CLKAB	CLKOUT	3.0	6.2	10.0	ns
t_{PHL}			3.0	5.7	10.0	
t_{PLH}	$\overline{OEAB}$	B	1.6	4.4	8.0	ns
t_{PHL}	(CLKAB) (Note 13)		1.3	6.1	9.8	
t_{SKEW}	B (Note 14)	CLKOUT	0		2	ns
t_{RISE}	Transition time, B outputs (20% to 80%)			2.6		ns
t_{FALL}	Transition time, B outputs (20% to 80%)			2.6		
t_{PLH}	B	A	2.0	5.6	8.2	ns
t_{PHL}			1.4	5.0	7.2	
t_{PLH}	LEBA	A	2.1	4.2	6.3	ns
t_{PHL}			1.9	3.3	5.0	
t_{PLH}	CLKBA	A	2.3	4.4	6.8	ns
t_{PHL}			2.1	3.5	5.2	
t_{PLH}	CLKOUT	CLKIN	3.0	6.0	10.0	ns
t_{PHL}			3.0	6.43	10.0	
t_{PZH}, t_{PZL}	$\overline{OEBA}$	A or CLKIN	1.5	5.0	6.4	ns
t_{PHZ}, t_{PLZ}			1.4	3.9	8.0	

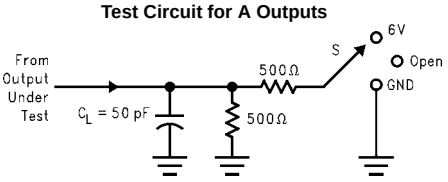
Note 12: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C.

Note 13: Three-state delays are actually synchronous with CLKAB

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delays for the CLKOUT pin and any B output transition when measured with reference to CLKAB↑. This guarantees the relationship between B output data and CLKOUT such that data is coincident or ahead of CLKOUT. This specification is guaranteed but not tested.

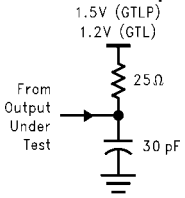
Test Circuits and Timing Waveforms

Test Circuit for A Outputs



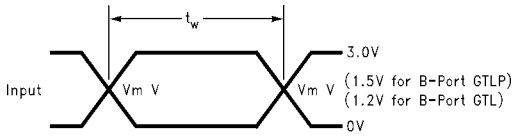
C_L includes probes and jig capacitance.

Test Circuit for B Outputs

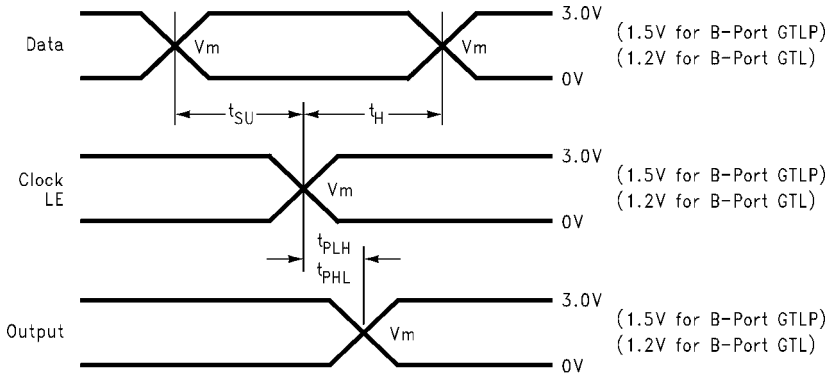


C_L includes probes and jig capacitance.
For B Port outputs, C_L = 30 pF is used for worst case edge rate.

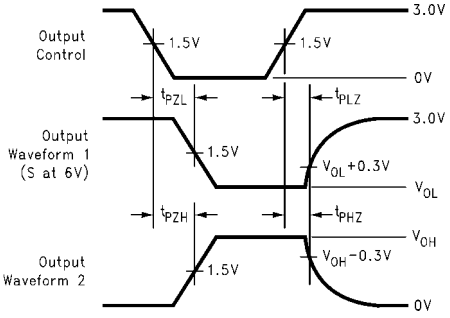
Voltage Waveforms Pulse Duration
(Vm = 1.5V for A Port and 1.0V for B Port)



Voltage Waveforms Propagation Delay and Setup and Hold Times
(Vm = 1.5V for A Port and 1.0V for B Port)

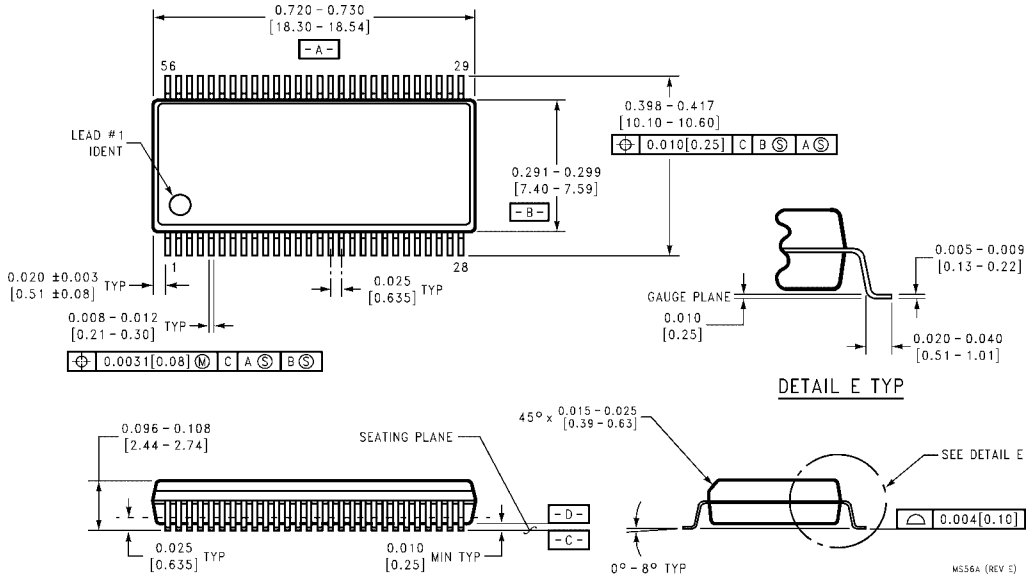


Voltage Waveforms Enable and Disable Times (A Port)



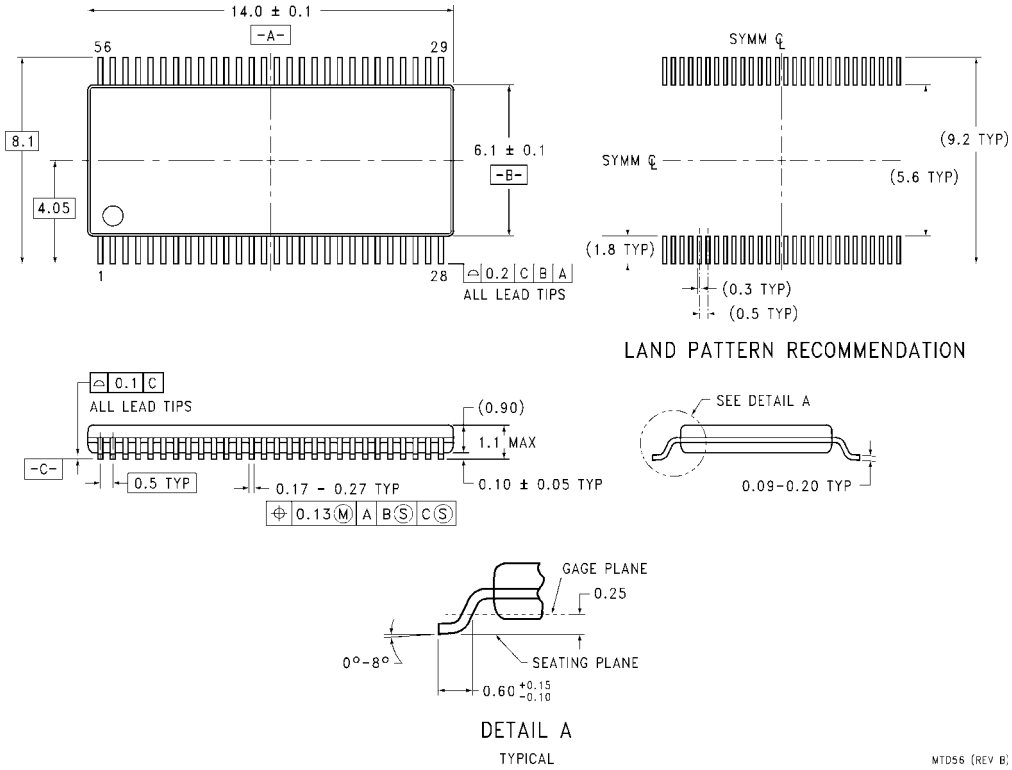
Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f = 2$ ns, $Z_O = 50\Omega$. The outputs are measured one at a time with one transition per measurement.

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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