# **Quad Bus Buffer**

# with 3-State Control Inputs

The MC74VHCT126A is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves noninverting high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT126A requires the 3-state control input (OE) to be set Low to place the output into high impedance.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT126A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when  $V_{CC}$  = 0 V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

#### **Features**

- High Speed:  $t_{PD} = 3.8 \text{ ns}$  (Typ) at  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4.0 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- TTL-Compatible Inputs:  $V_{IL} = 0.8 \text{ V}$ ;  $V_{IH} = 2.0 \text{ V}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- Pb-Free Packages are Available\*



### ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS



SOIC-14 D SUFFIX CASE 751A



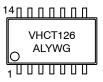


TSSOP-14 DT SUFFIX CASE 948G





SOEIAJ-14 M SUFFIX CASE 965



A = Assembly Location

WL, L = Wafer Lot Y = Year WW, W = Work Week G or ■ = Pb-Free Package

See Applications Note #AND8004/D for date code and traceability information.

#### **FUNCTION TABLE**

	VHCT126A				
	Inputs	Outputs			
А	OE	Υ			
Н	Н	Н			
L	Н	L			
X	L	Z			

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

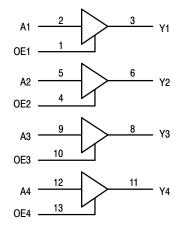


Figure 1. LOGIC DIAGRAM Active-High Output Enables

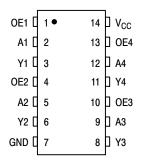


Figure 2. PIN ASSIGNMENT

#### **MAXIMUM RATINGS**

Rating		Symbol	Value	Unit
DC Supply Voltage		V <sub>CC</sub>	- 0.5 to + 7.0	٧
DC Input Voltage		V <sub>in</sub>	- 0.5 to + 7.0	٧
DC Output Voltage	Output in 3–State High or Low State	V <sub>out</sub>	-0.5  to  + 7.0 $-0.5 \text{ to } V_{CC} + 0.5$	٧
Input Diode Current		I <sub>IK</sub>	- 20	mA
Output Diode Current (V <sub>OUT</sub> <	GND; V <sub>OUT</sub> > V <sub>CC</sub> )	lok	± 20	mA
DC Output Current, per Pin		l <sub>out</sub>	± 25	mA
DC Supply Current, V <sub>CC</sub> and G	ND Pins	I <sub>CC</sub>	± 75	mA
Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	P <sub>D</sub>	500 450	mW
Storage Temperature		T <sub>stg</sub>	- 65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C TSSOP Package: – 6.1 mW/°C from 65° to 125°C

#### RECOMMENDED OPERATING CONDITIONS

Parame	eter	Symbol	Min	Max	Unit
DC Supply Voltage		V <sub>CC</sub>	4.5	5.5	V
DC Input Voltage		V <sub>in</sub>	0	5.5	V
DC Output Voltage	Output in 3–State High or Low State	V <sub>out</sub>	0 0	5.5 V <sub>CC</sub>	V
Operating Temperature		T <sub>A</sub>	- 40	+ 85	°C
Input Rise and Fall Time	V <sub>CC</sub> = 5.0 V ±0.5 V	t <sub>r</sub> , t <sub>f</sub>	0	20	ns/V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

#### DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	T,	գ = 25°	С	T <sub>A</sub> ≤	85°C	<b>T</b> <sub>A</sub> ≤ 1	125°C	
Parameter	Test Conditions	Symbol	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
Minimum High-Level Input Voltage		V <sub>IH</sub>	3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
Maximum Low-Level Input Voltage		V <sub>IL</sub>	3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
Minimum High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>II</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	V <sub>OH</sub>	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
AIV = AIH OI AIT	$\begin{aligned} V_{IN} &= V_{IH} \text{ or } V_{IL} \\ I_{OH} &= -4.0 \text{ mA} \\ I_{OH} &= -8.0 \text{ mA} \end{aligned}$		3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
Maximum Low-Level Output Voltage VIN = VIH or VII	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50 \mu A$	V <sub>OL</sub>	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
VIN = VIH OF VIL	$\begin{aligned} &V_{IN} = V_{IH} \text{ or } V_{IL} \\ &I_{OL} = 4.0 \text{ mA} \\ &I_{OL} = 8.0 \text{ mA} \end{aligned}$		3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	I <sub>IN</sub>	0 to 5.5			± 0.1		±1.0		±1.0	μА
Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	Icc	5.5			2.0		20		40	μΑ
Quiescent Supply Current	Input: V <sub>IN</sub> = 3.4 V	I <sub>CCT</sub>	5.5			1.35		1.50		1.65	mA
Maximum 3-State Leakage Current	$V_{IN} = V_{IH} \text{ or } V_{I}$ $V_{OUT} = V_{CC} \text{ or GND}$	l <sub>OZ</sub>	5.5			±0.2 5		±2.5		±2.5	μΑ
Output Leakage Current	V <sub>OUT</sub> = 5.5 V	I <sub>OPD</sub>	0.0			0.5		5.0		10	μΑ

#### AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns)

			T <sub>A</sub> = 25°C		<b>T</b> <sub>A</sub> = ≤ 85°C		<b>C T</b> <sub>A</sub> ≤ 125° <b>C</b>			
Parameter	Test Conditions	Symbol	Min	Тур	Max	Min	Max	Min	Max	Unit
Maximum Propagation Delay, A to Y	$V_{CC} = 3.3 \pm 0.3 \ V  C_L = 15 \ pF \\ C_L = 50 \ pF$	t <sub>PLH</sub> , t <sub>PHL</sub>		5.6 8.1	8.0 11.5	1.0 1.0	9.5 13.0		12.0 16.0	ns
	$V_{CC} = 5.0 \pm 0.5 \text{ V}  \begin{array}{c} C_L = 15 \text{ pF} \\ C_L = 50 \text{ pF} \end{array}$			3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5		8.5 10.5	
Maximum Output Enable TIme,OE to Y	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	t <sub>PZL</sub> , t <sub>PZH</sub>		5.4 7.9	8.0 11.5	1.0 1.0	9.5 13.0		11.5 15.0	ns
	$\begin{array}{cccccccccccccccccccccccccccccccccccc$			3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0		7.5 9.5	
Maximum Output Disable Time, OE to Y	$\begin{array}{c} V_{CC} = 3.3 \pm 0.3 \ V  C_L = 50 \ pF \\ R_L = 1.0 \ k\Omega \end{array}$	t <sub>PLZ</sub> , t <sub>PHZ</sub>		9.5	13.2	1.0	15.0		18.0	ns
	$\begin{aligned} V_{CC} &= 5.0 \pm 0.5 \text{ V}  C_L = 50 \text{ pF} \\ R_L &= 1.0 \text{ k}\Omega \end{aligned}$			6.1	8.8	1.0	10.0		12.0	
Output-to-Output Skew	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 50 pF (Note 1)	t <sub>OSLH</sub> , t <sub>OSHL</sub>			1.5		1.5		2.0	ns
	$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $C_L = 50 \text{ pF}$ (Note 1)				1.0		1.0		1.5	
Maximum Input Capacitance		C <sub>in</sub>		4	10		10		10	pF
Maximum Three–State Output Capacitance (Output in High Impedance State)		C <sub>out</sub>		6						pF
	-		Typical @ 25°C, V <sub>CC</sub> = 5.0V							
Power Dissipation Capacitance (I	Note 2)	C <sub>PD</sub>				15				pF

Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PLHn</sub>|.
 C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/4 (per buffer). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NOISE CHARACTERISTICS (Input $t_r$ = $t_f$ = 3.0ns, $C_L$ = 50pF, $V_{CC}$ = 5.0V)

		T <sub>A</sub> = 25°C		
Characteristic	Symbol	Тур	Max	Unit
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	0.3	0.8	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	- 0.3	- 0.8	V
Minimum High Level Dynamic Input Voltage	$V_{IHD}$		3.5	V
Maximum Low Level Dynamic Input Voltage	$V_{ILD}$		1.5	V

#### **SWITCHING WAVEFORMS**

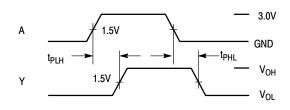


Figure 3.

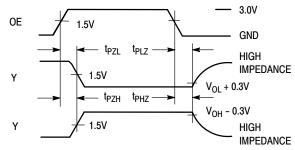
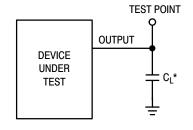


Figure 4.



\*Includes all probe and jig capacitance

Figure 5. Test Circuit

DEVICE UNDER TEST  $C_L^*$ TEST POINT

OUTPUT  $1 \text{ k}\Omega$ OUTPUT  $1 \text{ k}\Omega$   $C_L^*$ CONNECT TO  $V_{CC}$  WHEN TESTING  $t_{PLZ}$  AND  $t_{PZL}$ CONNECT TO GND WHEN TESTING  $t_{PHZ}$  AND  $t_{PZH}$ .

\*Includes all probe and jig capacitance

Figure 6. Test Circuit

#### **ORDERING INFORMATION**

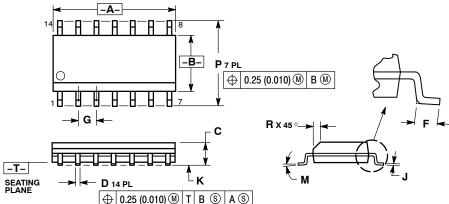
Device	Package	Shipping <sup>†</sup>
MC74VHCT126ADR2	SOIC-14	
MC74VHCT126ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74VHCT126AM	SOEIAJ-14	
MC74VHCT126AMG	SOEIAJ-14 (Pb-Free)	50 Units / Rail
MC74VHCT126AMEL	SOEIAJ-14	
MC74VHCT126AMELG	SOEIAJ-14 (Pb-Free)	2000 / Tape & Reel
MC74VHCT126ADTRG	TSSOP-14* (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>This package is inherently Pb-Free.

#### PACKAGE DIMENSIONS

SOIC-14 CASE 751A-03 ISSUE G

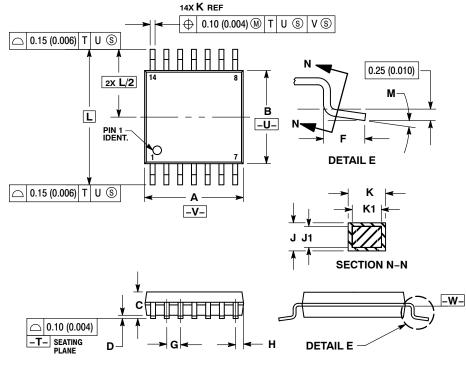


- NOTES:
  1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE
   MOLD PROTRUSION.
   MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE
- 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
М	0 °	7°	0°	7°
Р	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

#### TSSOP-14 **DT SUFFIX** CASE 948G-01 **ISSUE A**



#### NOTES:

- JTES:

  1. DIMENSIONING AND TOLERANCING PER
  ANSI Y14.5M, 1982.

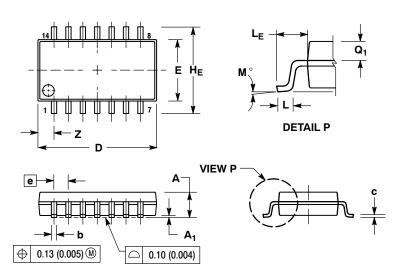
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD
  FLASH, PROTRUSIONS OR GATE BURRS.
  MOLD FLASH OR GATE BURRS SHALL NOT
- EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
  INTERLEAD FLASH OR PROTRUSION SHALL
- NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL
- CONDITION.

  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
Κ	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252	BSC
М	0 °	8 °	0 °	8 °

#### PACKAGE DIMENSIONS

#### SOEIAJ-14 CASE 965-01 ISSUE A



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- 2. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE
  MOLD FLASH OF PROTRUSIONS AND ARE
  MEASURED AT THE PARTING LINE. MOLD FLASH
  OR PROTRUSIONS SHALL NOT EXCEED 0.15
  (0.06) PER SIDE.

   TERMINAL NUMBERS ARE SHOWN FOR
- 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. 5. THE LEAD WIDTH DIMENSION (b) DOES NOT
- 5. HE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
Е	5.10	5.45	0.201	0.215
е	1.27	BSC	0.050	BSC
ΗE	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
π	1.10	1.50	0.043	0.059
M	0 °	10°	0°	10 °
Q1	0.70	0.90	0.028	0.035
Z		1.42		0.056

ON Semiconductor and limit are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5773-3850 ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

MC74VHCT126A/D