Non-Inverting 3-State Buffer, TTL Level

LSTTL-Compatible Inputs

The NLU1GT126 MiniGate[™] is an advanced CMOS high-speed non-inverting buffer in ultra-small footprint.

The NLU1GT126 requires the 3-state control input (OE) to be set Low to place the output in the high impedance state.

The device input is compatible with TTL-type input thresholds and the output has a full 5.0 V CMOS level output swing.

The NLU1GT126 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 3.8 \text{ ns (Typ)} @ V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 2 \mu A \text{ (Max)}$ at $T_A = 25^{\circ}\text{C}$
- TTL-Compatible Input: $V_{IL} = 0.8 \text{ V}$; $V_{IH} = 2.0 \text{ V}$
- CMOS-Compatible Output:
 - $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @ Load
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Ultra-Small Packages
- These are Pb-Free Devices

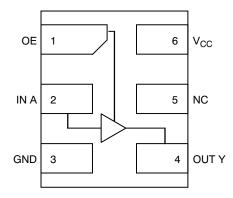


Figure 1. Pinout (Top View)



Figure 2. Logic Symbol



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MARKING DIAGRAMS



UDFN6 MU SUFFIX CASE 517AA





ULLGA6 1.0 x 1.0 CASE 613AD





ULLGA6 1.2 x 1.0 CASE 613AE





ULLGA6 1.45 x 1.0 CASE 613AF



9 = Device MarkingM = Date Code

PIN ASSIGNMENT

1	OE			
2	IN A			
3	GND			
4	OUT Y			
5	NC			
6	V _{CC}			

FUNCTION TABLE

Input		Output
Α	OE	Υ
L H	H	L H
X	L	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Parameter			
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V	
V _{IN}	DC Input Voltage		-0.5 to +7.0	V	
V _{OUT}	DC Output Voltage		-0.5 to +7.0	V	
I _{IK}	DC Input Diode Current	V _{IN} < GND	-20	mA	
I _{OK}	DC Output Diode Current	V _{OUT} < GND	±20	mA	
Io	DC Output Source/Sink Current		±12.5	mA	
I _{CC}	DC Supply Current Per Supply Pin		±25	mA	
I _{GND}	DC Ground Current per Ground Pin		±25	mA	
T _{STG}	Storage Temperature Range		-65 to +150	°C	
TL	Lead Temperature, 1 mm from Case for 10 Secon	ds	260	°C	
TJ	Junction Temperature Under Bias	150	°C		
MSL	Moisture Sensitivity	Level 1			
F _R	Flammability Rating O	xygen Index: 28 to 34	UL 94 V-0 @ 0.125 in		
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below GND	Latchup Performance Above V _{CC} and Below GND at 125°C (Note 2)			

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
 Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V	
V _{IN}	Digital Input Voltage	0	5.5	V	
V _{OUT}	Output Voltage	0	5.5	V	
T _A	Operating Free-Air Temperature			+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

				Т	A = 25 °	°C	T _A = ·	+85°C	T _A = - to +1		
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	Low-Level Input Voltage		3.0 4.5 to 5.5	1.4 2.0			1.4 2.0		1.4 2.0		V
V _{IL}	Low-Level Input Voltage		3.0 4.5 to 5.5			0.53 0.8		0.53 0.8		0.53 0.8	V
V _{OH}	High-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V _{OL}	Low-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu\text{A}$	3.0 4.5		0	0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5 V$	0 to 5.5			±0.1		±1.0		±1.0	μΑ
I _{CC}	Quiescent Supply Current	$0 \le V_{IN} \le V_{CC}$	5.5			1.0		20		40	μΑ
ГССТ	Quiescent Supply Current	V _{IN} = 3.4 V Other Input: V _{CC} or GND	5.5			1.35		1.50		1.65	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0			0.5		5.0		10	μΑ
l _{OZ}	3-State Leakage Current	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or }$ GND	0			±0.25		±2.5		±2.5	μΑ

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

		v _{cc}	Test	Т	- _A = 25 °	°C	T _A =	+85°C		-55°C 25°C	
Symbol	Parameter	(V)	Condition	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Propagation Delay, A to Y (Figures 3 and 5)	3.0 to 3.6	C _L = 15 pF C _L = 50 pF		5.6 8.1	8.0 11.5	1.0 1.0	9.5 13		12 16	ns
		4.5 to 5.5	C _L = 15 pF C _L = 50 pF		3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5		8.5 10.5	
t _{PZL} , t _{PZH}	Output Enable Time, OE to Y (Figures 4 and 6)	3.0 to 3.6	C _L = 15 pF C _L = 50 pF		5.4 7.9	8.0 11.5	1.0 1.0	9.5 13		11.5 15	ns
		4.5 to 5.5	$C_L = 15 pF$ $C_L = 50 pF$		3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0		7.5 9.5	
t _{PLZ} , t _{PHZ}	Output Disable Time, OE to Y (Figures 4 and 6)	3.0 to 3.6	$C_L = 15 pF$ $C_L = 50 pF$		6.5 8.0	9.7 13.2	1.0 1.0	11.5 15		14.5 18.5	ns
		4.5 to 5.5	C _L = 15 pF C _L = 50 pF		4.8 7.0	6.8 8.8	1.0 1.0	8.0 10		10 12	
C _{IN}	Input Capacitance				4	10		10		10	pF
C _{OUT}	3-State Output Capacitance (Output in High Impedance State)				6						pF
C _{PD}	Power Dissipation Capacitance (Note 3)	5.0			14						pF

^{3.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

SWITCHING WAVEFORMS

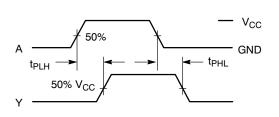
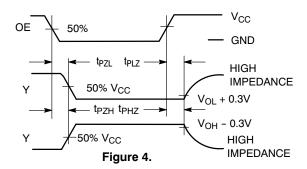
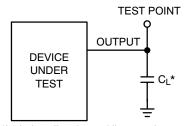
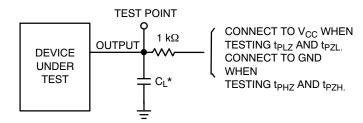


Figure 3. Switching Waveforms





*Includes all probe and jig capacitance



*Includes all probe and jig capacitance

Figure 5. Test Circuit

Figure 6. Test Circuit

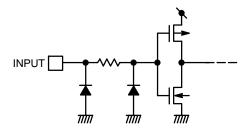


Figure 7. Input Equivalent Circuit

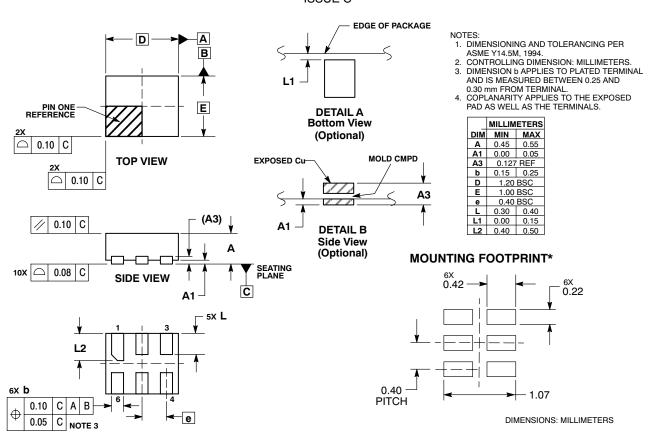
ORDERING INFORMATION

Device	Package	Shipping [†]
NLU1GT126MUTCG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NLU1GT126AMX1TCG	ULLGA6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLU1GT126BMX1TCG	ULLGA6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLU1GT126CMX1TCG	ULLGA6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

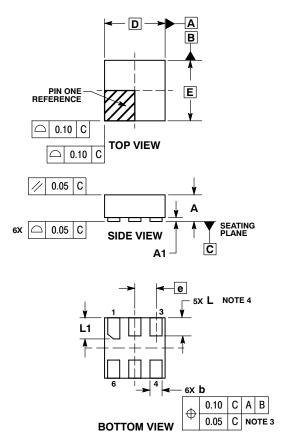
UDFN6, 1.2x1.0, 0.4P CASE 517AA-01 ISSUE C



BOTTOM VIEW

PACKAGE DIMENSIONS

ULLGA6 1.0x1.0, 0.35P CASE 613AD-01 **ISSUE A**



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

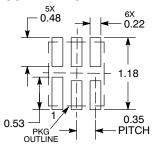
 2. CONTROLLING DIMENSION: MILLIMETERS.

 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

 4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PLACED FERMINAL FROM THE EDGE OF THE PLACED FERMINAL FROM THE EDGE OF THE PLACED FROM THE EDGE OF THE PLACED FERMINAL FROM THE EDGE OF THE PLACED FROM THE EDGE OF THE PLACED FERMINAL FROM THE EDGE OF THE PLACED FROM THE PLACED FROM THE PLACED FROM THE PLACED FROM THE PLACED FR
- PACKAGE IS ALLOWED.

	MILLIMETERS				
DIM	MIN	MAX			
Α		0.40			
A1	0.00	0.05			
b	0.12	0.22			
D	1.00	BSC			
Е	1.00	BSC			
е	0.35 BSC				
L	0.25	0.35			
11	0.30	0.40			

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

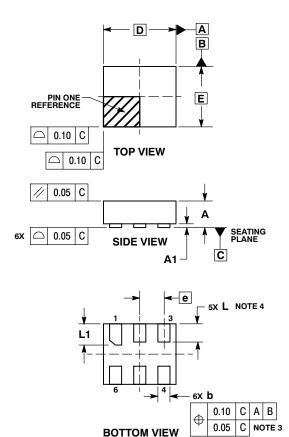


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

ULLGA6 1.2x1.0, 0.4P CASE 613AE-01 **ISSUE A**



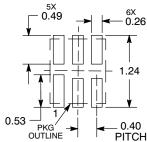
NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION 6 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
 4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS						
DIM	MIN	MAX					
Α		0.40					
A1	0.00	0.05					
b	0.15	0.25					
D	1.20 BSC						
Е	1.00	BSC					
е	0.40	BSC					
L	0.25	0.35					
L1	0.35	0.45					

MOUNTING FOOTPRINT **SOLDERMASK DEFINED***

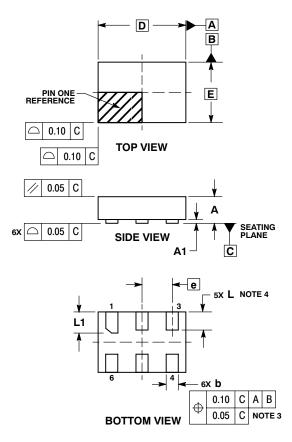


DIMENSIONS: MILLIMETERS

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

ULLGA6 1.45x1.0, 0.5P CASE 613AF-01 **ISSUE A**

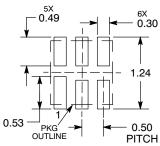


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- 1. DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE
- PACKAGE IS ALLOWED.

	MILLIMETERS					
DIM	MIN	MAX				
Α		0.40				
A1	0.00	0.05				
b	0.15	0.25				
D	1.45 BSC					
Е	1.00	BSC				
е	0.50	BSC				
L	0.25	0.35				
L1	0.30	0.40				

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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