74LVC126A

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

Rev. 06.00 — 16 May 2006 **Product data sheet**

1. General description

The 74LVC126A consists of four non-inverting buffers/line drivers with 3-state outputs, which are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a high-impedance OFF-state.

It is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs.

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard JESD8-B / JESD36
- ESD protection:
  - HBM JESD22-A114-C exceeds 2000 V
  - CDM JESD22-C101-C exceeds 1000 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC126AD	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC126ADB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC126APW	–40 °C to +125 °C	TSSOP14	plastic thin small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC126ABQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

PHILIPS

4. Functional diagram

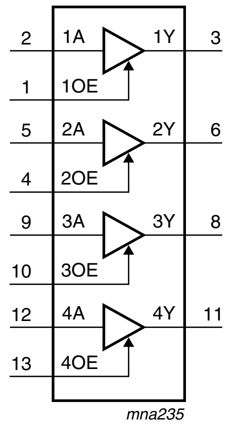


Fig 1. Logic symbol

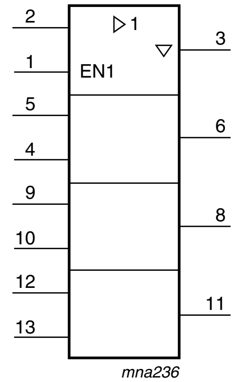


Fig 2. IEC logic symbol

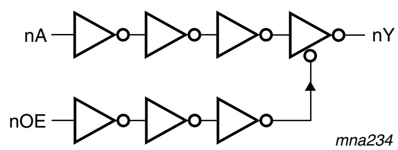


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

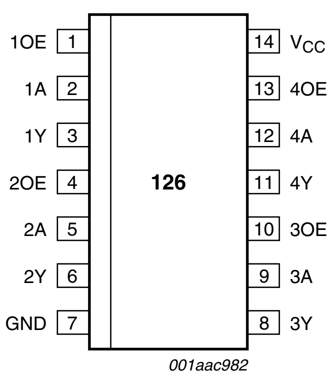
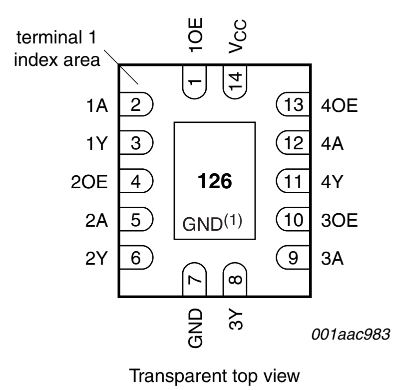


Fig 4. Pin configuration for SO14 and (T)SSOP14



(1) * The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5. Pin configuration for DHVQFN14

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
1OE	1	data enable input (active HIGH)
1A	2	data input
1Y	3	data output
2OE	4	data enable input (active HIGH)
2A	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
3OE	10	data enable input (active HIGH)
4Y	11	data output
4A	12	data input
4OE	13	data enable input (active HIGH)
V_{CC}	14	supply voltage

6. Functional description

Table 3: Functional table[1]

Inputs		Outputs
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state.

7. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW-state	[1]	–0.5	V_{CC} + 0.5	V
		output 3-state	[1]	–0.5	+6.5	V
I_O	output current	V_O = 0 to V_{CC}		-	±50	mA
I_{CC}	supply current			-	+100	mA
I_{GND}	ground current			-	–100	mA
T_{stg}	storage temperature		[2]	–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_o	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6: Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V		1.08	-	-	V
		V_{CC} = 1.65 V to 1.95 V		0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V		-	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V		-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA; V_{CC} = 1.65 V to 3.6 V		V_{CC} − 0.2	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V		V_{CC} − 0.45	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V		V_{CC} − 0.5	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V		V_{CC} − 0.5	-	-	V
		I_O = −18 mA; V_{CC} = 3.0 V		V_{CC} − 0.6	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V		V_{CC} − 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V		-	-	0.2	V
		I_O = 4 mA; V_{CC} = 1.65 V		-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V		-	-	0.6	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	-	0.55	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND		-	±0.1	±5	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 3.6 V; V_O = 5.5 V or GND;	[2]	-	±0.1	±5	μA
I_{OFF}	power-off leakage supply	V_{CC} = 0 V; V_I or V_O = 5.5 V		-	±0.1	±10	μA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0		-	0.1	10	μA
ΔI_{CC}	additional supply current per input pin	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} − 0.6 V; I_O = 0		-	5	500	μA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}		-	4.0	-	pF
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V		1.08	-	-	V
		V_{CC} = 1.65 V to 1.95 V		0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V		-	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V		-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	V

Table 6: Static characteristics *…continued*
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = -100\ \mu A$; $V_{CC} = 1.65\ V$ to $3.6\ V$		$V_{CC} - 0.3$	-	-	V
		$I_O = -4\ mA$; $V_{CC} = 1.65\ V$		$V_{CC} - 0.6$	-	-	V
		$I_O = -8\ mA$; $V_{CC} = 2.3\ V$		$V_{CC} - 0.65$	-	-	V
		$I_O = -12\ mA$; $V_{CC} = 2.7\ V$		$V_{CC} - 0.65$	-	-	V
		$I_O = -18\ mA$; $V_{CC} = 3.0\ V$		$V_{CC} - 0.75$	-	-	V
		$I_O = -24\ mA$; $V_{CC} = 3.0\ V$		$V_{CC} - 1$	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 100\ \mu A$; $V_{CC} = 1.65\ V$ to $3.6\ V$		-	-	0.3	V
		$I_O = 4\ mA$; $V_{CC} = 1.65\ V$		-	-	0.65	V
		$I_O = 8\ mA$; $V_{CC} = 2.3\ V$		-	-	0.8	V
		$I_O = 12\ mA$; $V_{CC} = 2.7\ V$		-	-	0.6	V
		$I_O = 24\ mA$; $V_{CC} = 3.0\ V$		-	-	0.8	V
I_I	input leakage current	$V_{CC} = 3.6\ V$; $V_I = 5.5\ V$ or GND		-	-	±20	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 3.6\ V$; $V_O = 5.5\ V$ or GND;	[2]	-	-	±20	μA
I_{OFF}	power-off leakage supply	$V_{CC} = 0.0\ V$; V_I or $V_O = 5.5\ V$		-	-	±20	μA
I_{CC}	supply current	$V_{CC} = 3.6\ V$; $V_I = V_{CC}$ or GND; $I_O = 0$		-	-	40	μA
ΔI_{CC}	additional supply current per input pin	$V_{CC} = 2.7\ V$ to $3.6\ V$; $V_I = V_{CC} - 0.6\ V$; $I_O = 0$		-	-	5000	μA

[1] All typical values are measured at $V_{CC} = 3.3\ V$ (unless stated otherwise) and $T_{amb} = 25\ °C$.

[2] For I/O ports, the parameter I_{OZ} includes the input leakage current.

10. Dynamic characteristics

Table 7: Dynamic characteristics
Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$T_{amb} = -40\ °C$ to $+85\ °C$						
t_{PHL}, t_{PLH}	HIGH to LOW, LOW to HIGH propagation delay nA to nY	see Figure 6				
		$V_{CC} = 1.2\ V$	-	11.0	-	ns
		$V_{CC} = 1.65\ V$ to $1.95\ V$	1.2	5.2	10.2	ns
		$V_{CC} = 2.3\ V$ to $2.7\ V$	0.8	2.8	5.3	ns
		$V_{CC} = 2.7\ V$	1.5	2.7	4.8	ns
		$V_{CC} = 3.0\ V$ to $3.6\ V$	1.1	2.4	4.5	ns
t_{PZH}, t_{PZL}	OFF-state to HIGH, OFF-state to LOW propagation delay nOE to nY	see Figure 7				
		$V_{CC} = 1.2\ V$	-	15.0	-	ns
		$V_{CC} = 1.65\ V$ to $1.95\ V$	2.2	6.7	11.9	ns
		$V_{CC} = 2.3\ V$ to $2.7\ V$	1.8	3.8	6.6	ns
		$V_{CC} = 2.7\ V$	1.6	3.1	5.7	ns
		$V_{CC} = 3.0\ V$ to $3.6\ V$	1.5	3.1	5.3	ns

Table 7: Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{PHZ}, t_{PLZ}	HIGH to OFF-state, LOW to OFF-state propagation delay nOE to nY	see Figure 7					
		V_{CC} = 1.2 V		-	8.0	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.1	3.3	7.6	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	1.8	4.3	ns
		V_{CC} = 2.7 V		2.3	3.4	5.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.4	2.5	4.6	ns
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[2]	-	-	1.0	ns
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	HIGH to LOW, LOW to HIGH propagation delay nA to nY	see Figure 6					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.2	-	13.0	ns
		V_{CC} = 2.3 V to 2.7 V		0.8	-	7.0	ns
		V_{CC} = 2.7 V		1.5	-	6.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.1	-	6.0	ns
t_{PZH}, t_{PZL}	OFF-state to HIGH, OFF-state to LOW propagation delay nOE to nY	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		2.2	-	15.0	ns
		V_{CC} = 2.3 V to 2.7 V		1.8	-	8.5	ns
		V_{CC} = 2.7 V		1.6	-	7.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	7.0	ns
t_{PHZ}, t_{PLZ}	HIGH to OFF-state, LOW to OFF-state propagation delay nOE to nY	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.1	-	9.5	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	-	5.5	ns
		V_{CC} = 2.7 V		2.3	-	6.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.4	-	6.0	ns
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[2]	-	-	1.5	ns
T_{amb} = 25 °C							
C_{PD}	power dissipation capacitance per gate.	V_I = GND to V_{CC}	[3]				
		V_{CC} = 1.65 V to 1.95 V		-	6.0	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	9.0	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	12	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz,

f_o = output frequency in MHz,

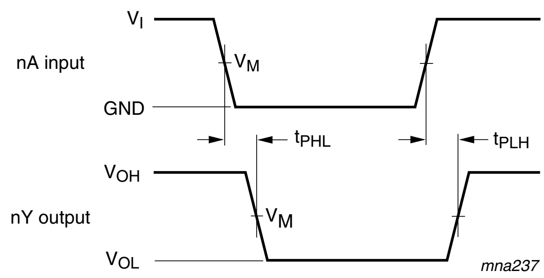
C_L = output load capacitance in pF,

V_{CC} = supply voltage in Volts,

N = number of inputs switching,

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. AC waveforms

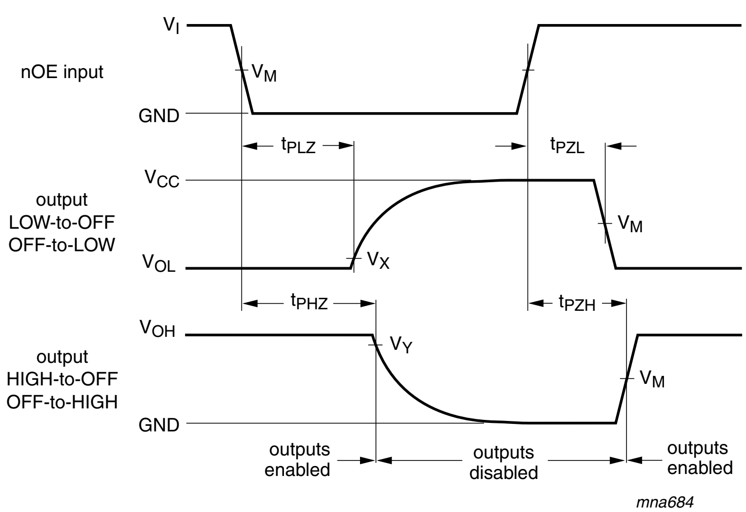


V_M = 1.5 V at $V_{CC} \geq 2.7$ V;

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V;

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 6. The input nA to output nY propagation delays



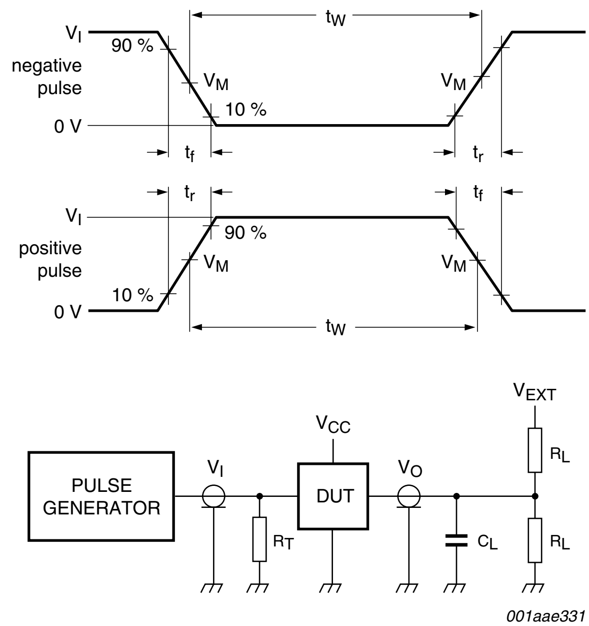
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 7. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
$V_{CC} < 2.7$ V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
$V_{CC} \geq 2.7$ V	1.5 V	1.5 V	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

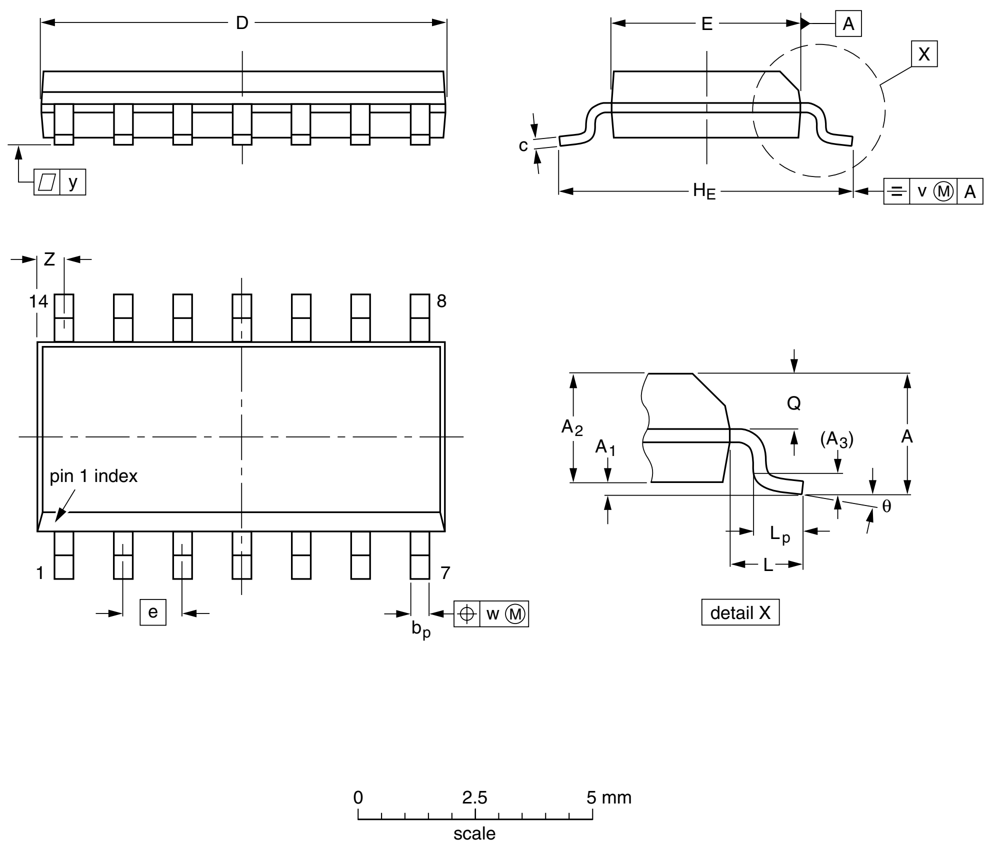
Fig 8. Load circuitry for switching times

Table 9: Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

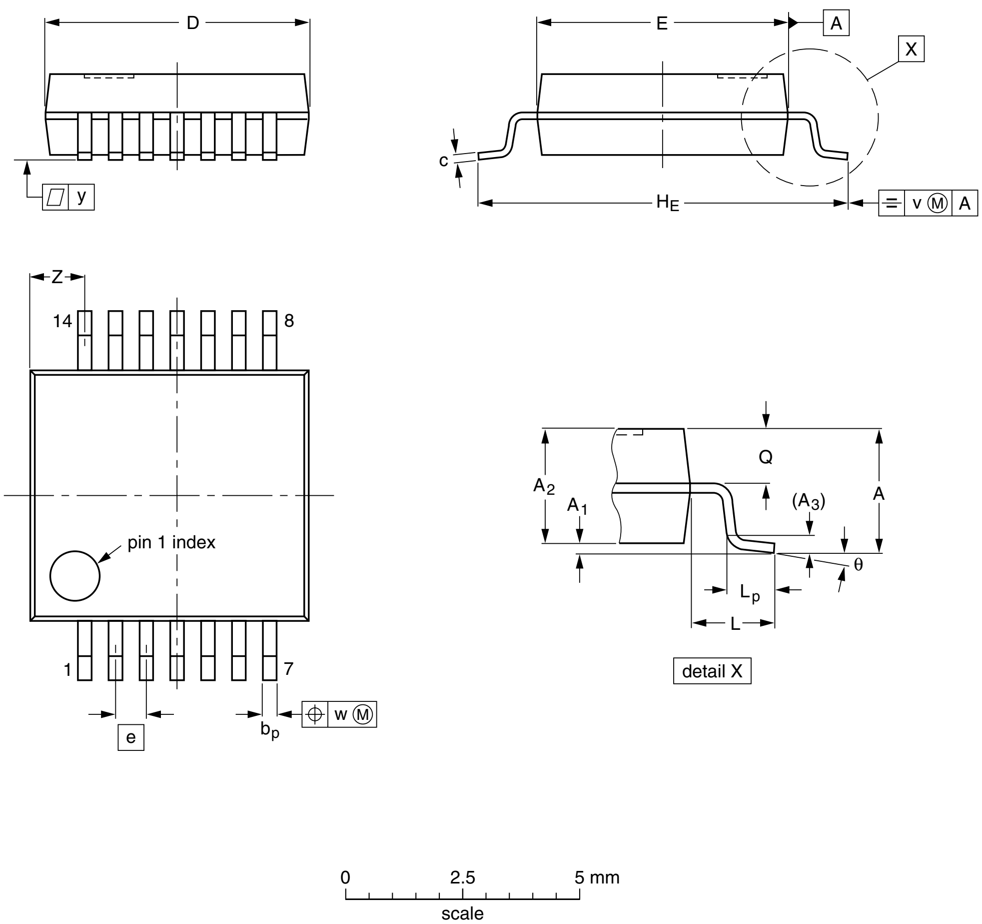
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

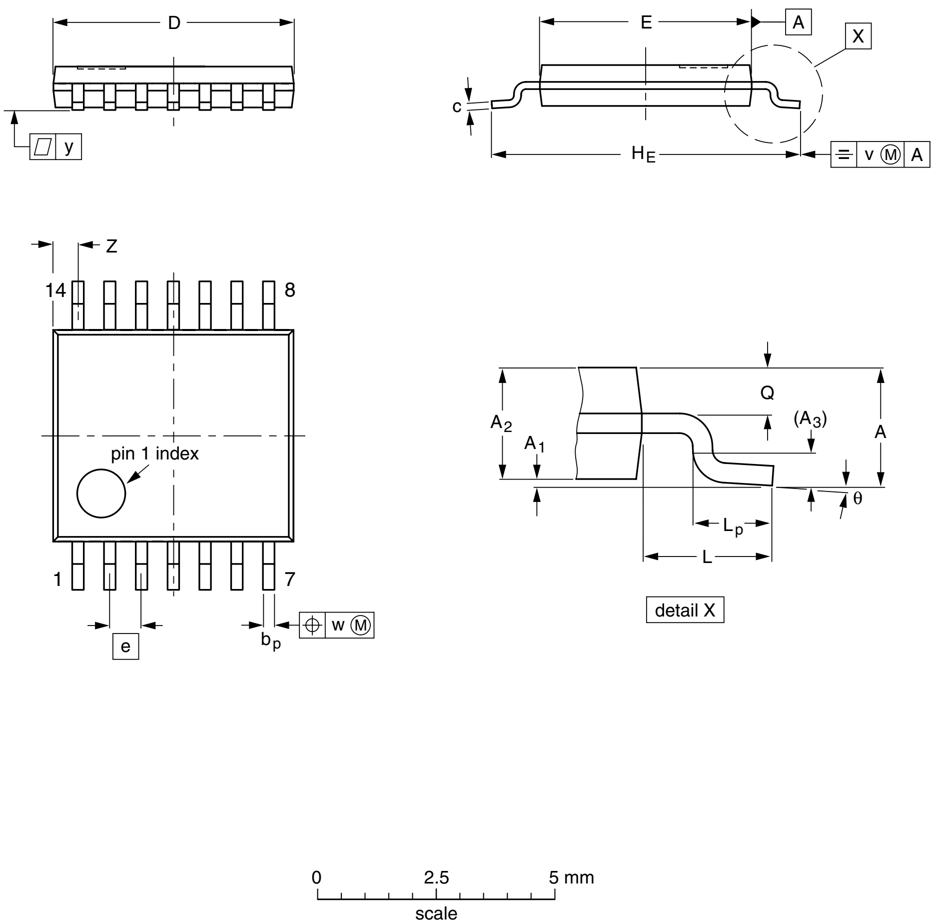
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

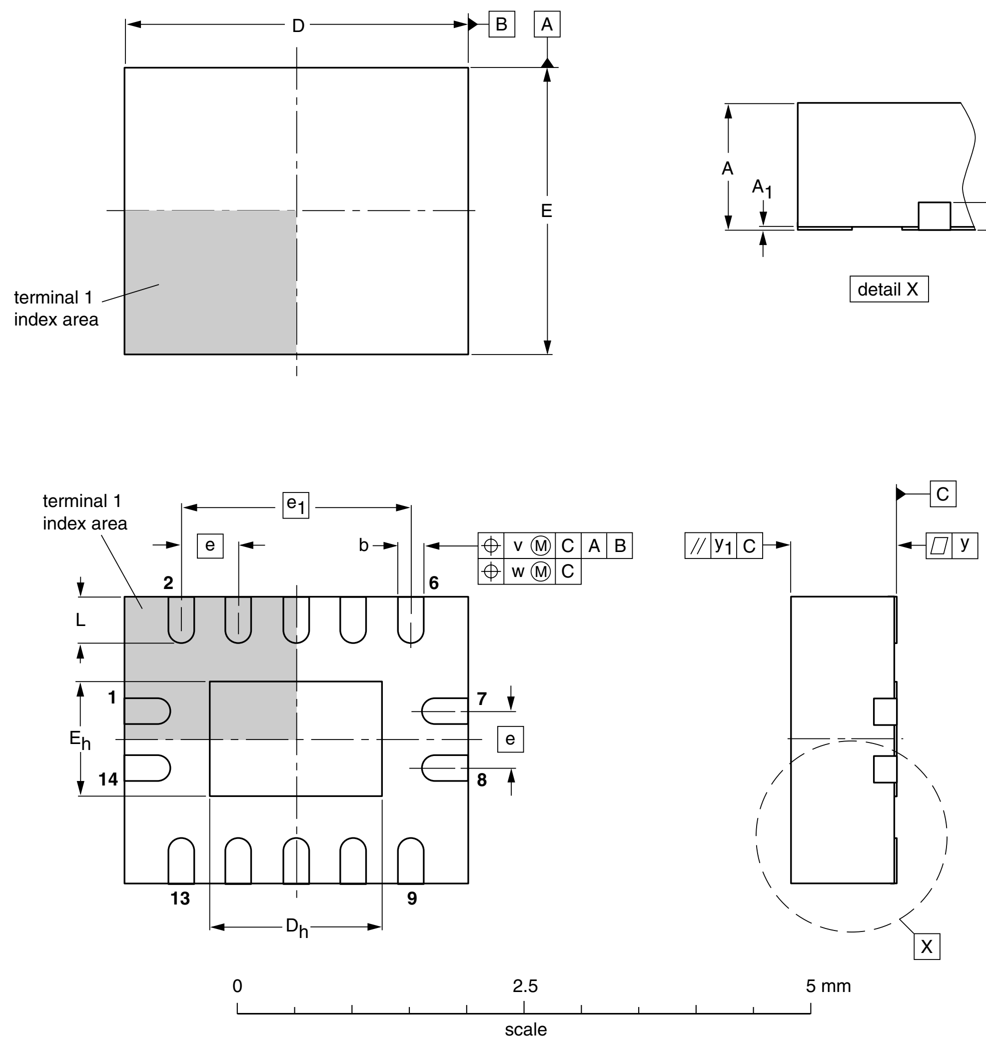
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 12. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC126A_6	<tbd>	Product data sheet	-	74LVC126A_5
Modifications:	• The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Table 4, Table 5, Table 6, Table 7 and Table 9: values added for lower voltage ranges.			
74LVC126A_5 (9397 750 10533)	030228	Product specification	-	74LVC126A_4
74LVC126A_4 (9397 750 09447)	020308	Product specification	-	74LVC126A_3
74LVC126A_3 (9397 750 04492)	980428	Product specification	-	74LVC126A_2
74LVC126A_2	970801	Product specification	-	74LVC126A_1
74LVC126A_1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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17. Contents

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Date of release: 16 May 2006

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