

74AUP2G125

Low-power dual buffer/line driver; 3-state

Rev. 7 — 21 September 2010

Product data sheet

1. General description

The 74AUP2G125 provides the dual non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (\overline{nOE}). A HIGH level at pin \overline{nOE} causes the output to assume a high-impedance OFF-state. This device has the input-disable feature, which allows floating input signals. The inputs are disabled when the output enable input (\overline{nOE}) is HIGH.

Schmitt-trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V. This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
 - ◆ JESD8-12 (0.8 V to 1.3 V)
 - ◆ JESD8-11 (0.9 V to 1.65 V)
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - ◆ JESD8-5 (1.8 V to 2.7 V)
 - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F Class 3A exceeds 5000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; $I_{CC} = 0.9 \mu\text{A}$ (maximum)
- Latch-up performance exceeds 100 mA per JESD78B Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- Input-disable feature allows floating input conditions
- I_{OFF} circuitry provides partial power-down mode operation
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$



3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AUP2G125DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AUP2G125GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74AUP2G125GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
74AUP2G125GD	-40 °C to +125 °C	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm	SOT996-2
74AUP2G125GM	-40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm	SOT902-1
74AUP2G125GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74AUP2G125GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code ^[1]
74AUP2G125DC	p25
74AUP2G125GT	p25
74AUP2G125GF	aM
74AUP2G125GD	p25
74AUP2G125GM	p25
74AUP2G125GN	aM
74AUP2G125GS	aM

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

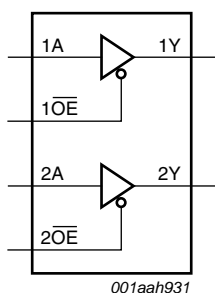


Fig 1. Logic symbol

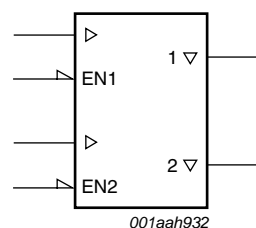


Fig 2. IEC logic symbol

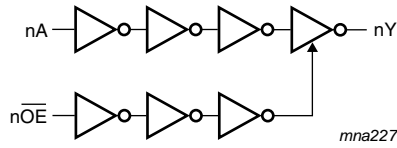


Fig 3. Logic diagram (one gate)

6. Pinning information

6.1 Pinning

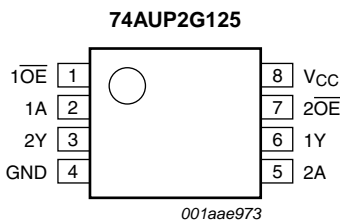


Fig 4. Pin configuration SOT765-1

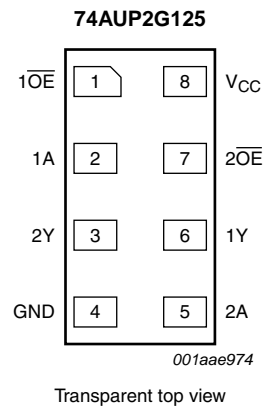


Fig 5. Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203

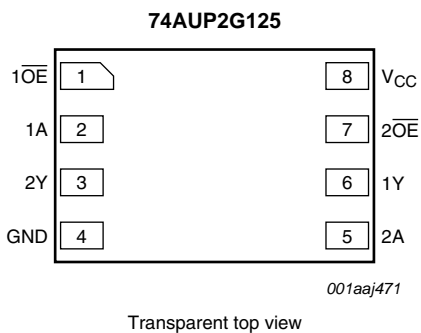


Fig 6. Pin configuration SOT996-2

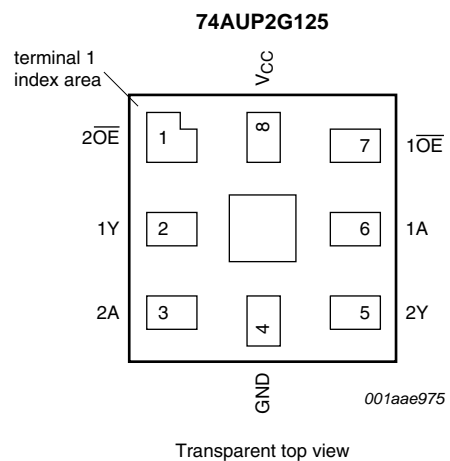


Fig 7. Pin configuration SOT902-1

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT765-1, SOT833-1, SOT1089, SOT996-2, SOT1116 and SOT1203	SOT902-1	
$\overline{1OE}, \overline{2OE}$	1, 7	7, 1	output enable input (active LOW)
1A, 2A	2, 5	6, 3	data input
GND	4	4	ground (0 V)
1Y, 2Y	6, 3	2, 5	data output
V _{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Output	
nOE	nA	nY	
L	L	L	
L	H	H	
H	X	Z	

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		[1] -0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
V _O	output voltage	Active mode and Power-down mode	[1] -0.5	+4.6	V
I _O	output current	V _O = 0 V to V _{CC}	-	±20	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2] -	250	mW

- [1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
 For XSON8, XSON8U and XQFN8U packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8$ V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 0.8$ V	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.6	-	-	V
		$V_{CC} = 3.0$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 0.8$ V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 3.0$ V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ μ A; $V_{CC} = 0.8$ V to 3.6 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1$ mA; $V_{CC} = 1.1$ V	$0.75 \times V_{CC}$	-	-	V
		$I_O = -1.7$ mA; $V_{CC} = 1.4$ V	1.11	-	-	V
		$I_O = -1.9$ mA; $V_{CC} = 1.65$ V	1.32	-	-	V
		$I_O = -2.3$ mA; $V_{CC} = 2.3$ V	2.05	-	-	V
		$I_O = -3.1$ mA; $V_{CC} = 2.3$ V	1.9	-	-	V
		$I_O = -2.7$ mA; $V_{CC} = 3.0$ V	2.72	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 3.0$ V	2.6	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ μ A; $V_{CC} = 0.8$ V to 3.6 V	-	-	0.1	V
		$I_O = 1.1$ mA; $V_{CC} = 1.1$ V	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7$ mA; $V_{CC} = 1.4$ V	-	-	0.31	V
		$I_O = 1.9$ mA; $V_{CC} = 1.65$ V	-	-	0.31	V
		$I_O = 2.3$ mA; $V_{CC} = 2.3$ V	-	-	0.31	V
		$I_O = 3.1$ mA; $V_{CC} = 2.3$ V	-	-	0.44	V
		$I_O = 2.7$ mA; $V_{CC} = 3.0$ V	-	-	0.31	V
		$I_O = 4.0$ mA; $V_{CC} = 3.0$ V	-	-	0.44	V

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input leakage current	$V_I = \text{GND to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	± 0.1	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH} \text{ or } V_{IL}; V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	± 0.1	μA
I_{OFF}	power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	± 0.2	μA
ΔI_{OFF}	additional power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	± 0.2	μA
I_{CC}	supply current	$V_I = \text{GND or } V_{CC}; I_O = 0 \text{ A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.5	μA
ΔI_{CC}	additional supply current	data input; $V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	[1]	-	40	μA
		nOE input; $V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	[1]	-	110	μA
		all inputs; $V_I = \text{GND to } 3.6 \text{ V}; \text{nOE} = \text{GND}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	[2]	-	1	μA
C_I	input capacitance	$V_I = \text{GND or } V_{CC}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	0.8	-	pF
C_O	output capacitance	output enabled; $V_O = \text{GND}; V_{CC} = 0 \text{ V}$	-	1.4	-	pF
		output disabled; $V_O = \text{GND or } V_{CC}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	1.3	-	pF
$T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 0.8 \text{ V}$	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	-	-	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 0.8 \text{ V}$	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = -20 \mu\text{A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.7 \times V_{CC}$	-	-	V
		$I_O = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	1.03	-	-	V
		$I_O = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.30	-	-	V
		$I_O = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.97	-	-	V
		$I_O = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.85	-	-	V
		$I_O = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.67	-	-	V
$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.55	-	-	V		

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V		
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = 0 V to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.5	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.6	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.9	μA
ΔI _{CC}	additional supply current	data input; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V	[1]	-	50	μA
		n $\overline{\text{OE}}$ input; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V	[1]	-	120	μA
		all inputs; V _I = GND to 3.6 V; n $\overline{\text{OE}}$ = GND; V _{CC} = 0.8 V to 3.6 V	[2]	-	1	μA
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.75 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.6 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	0.93	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.17	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
I _O = -4.0 mA; V _{CC} = 3.0 V	2.30	-	-	V		

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.11	V	
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33 × V _{CC}	V	
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V	
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V	
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V	
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V	
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V	
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V	
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	μA	
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = 0 V to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	μA	
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	μA	
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	μA	
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	1.4	μA	
ΔI _{CC}	additional supply current	data input; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V	[1]	-	-	75	μA
		n $\overline{\text{OE}}$ input; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V	[1]	-	-	180	μA
		all inputs; V _I = GND to 3.6 V; n $\overline{\text{OE}}$ = GND; V _{CC} = 0.8 V to 3.6 V	[2]	-	-	1	μA

[1] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

[2] To show I_{CC} remains very low when the input-disable feature is enabled.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C			Unit
			Min	Typ ^[1]	Max	Min	Max (85 °C)	Max (125 °C)	

C_L = 5 pF

t _{pd}	propagation delay	nA to nY; see Figure 8	[2]						
		V _{CC} = 0.8 V	-	20.6	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.8	5.5	10.5	2.5	11.7	12.9	ns
		V _{CC} = 1.4 V to 1.6 V	2.2	3.9	6.1	2.0	7.3	8.1	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	3.2	4.8	1.7	6.1	6.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.6	2.6	3.6	1.4	4.3	4.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.4	2.4	3.1	1.2	3.9	4.4	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C			Unit
			Min	Typ ^[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t _{en}	enable time	n $\overline{\text{OE}}$ to nY; see Figure 9 ^[3]							
		V _{CC} = 0.8 V	-	69.9	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.1	6.1	11.8	2.9	13.9	15.4	ns
		V _{CC} = 1.4 V to 1.6 V	2.5	4.2	6.6	2.3	7.7	8.3	ns
		V _{CC} = 1.65 V to 1.95 V	2.1	3.4	5.1	2.0	6.2	6.8	ns
		V _{CC} = 2.3 V to 2.7 V	1.8	2.6	3.7	1.7	4.5	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.7	2.4	3.1	1.7	3.5	3.9	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nY; see Figure 9 ^[4]							
		V _{CC} = 0.8 V	-	14.3	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.7	4.3	6.5	2.7	7.3	8.2	ns
		V _{CC} = 1.4 V to 1.6 V	2.1	3.2	4.4	2.1	5.1	5.7	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	3.0	4.3	2.0	5.0	5.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	2.2	2.9	1.4	3.3	4.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.7	2.5	3.2	1.7	3.4	3.9	ns
C_L = 10 pF									
t _{pd}	propagation delay	nA to nY; see Figure 8 ^[2]							
		V _{CC} = 0.8 V	-	24.0	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.2	6.4	12.3	3.0	13.8	15.2	ns
		V _{CC} = 1.4 V to 1.6 V	2.1	4.5	7.3	1.9	8.5	9.4	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	3.8	5.5	1.7	6.8	7.6	ns
		V _{CC} = 2.3 V to 2.7 V	2.1	3.2	4.2	1.6	5.3	5.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	3.0	3.8	1.6	4.6	5.2	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nY; see Figure 9 ^[3]							
		V _{CC} = 0.8 V	-	73.7	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.6	6.9	13.5	3.4	15.8	17.5	ns
		V _{CC} = 1.4 V to 1.6 V	2.3	4.8	7.7	2.2	8.6	9.4	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	3.9	5.8	1.9	6.8	7.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.8	3.2	4.3	1.7	5.3	5.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.7	3.0	3.9	1.7	4.3	4.8	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nY; see Figure 9 ^[4]							
		V _{CC} = 0.8 V	-	32.7	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.4	5.4	7.9	3.4	8.8	9.9	ns
		V _{CC} = 1.4 V to 1.6 V	2.2	4.1	5.5	2.2	6.2	7.1	ns
		V _{CC} = 1.65 V to 1.95 V	2.2	4.2	5.6	1.9	6.3	7.1	ns
		V _{CC} = 2.3 V to 2.7 V	1.7	3.0	3.8	1.7	4.5	5.1	ns
		V _{CC} = 3.0 V to 3.6 V	2.1	3.8	4.8	1.7	5.0	5.6	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C			Unit
			Min	Typ ^[1]	Max	Min	Max (85 °C)	Max (125 °C)	
C_L = 15 pF									
t _{pd}	propagation delay	nA to nY; see Figure 8 ^[2]							
		V _{CC} = 0.8 V	-	27.4	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.6	7.2	14.1	3.3	15.8	17.5	ns
		V _{CC} = 1.4 V to 1.6 V	3.0	5.1	8.1	2.5	9.8	10.9	ns
		V _{CC} = 1.65 V to 1.95 V	2.2	4.3	6.3	2.0	7.9	8.8	ns
		V _{CC} = 2.3 V to 2.7 V	2.0	3.7	4.9	1.8	6.0	6.7	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	3.5	4.4	1.8	5.4	6.1	ns
t _{en}	enable time	nOE to nY; see Figure 9 ^[3]							
		V _{CC} = 0.8 V	-	77.5	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.0	7.7	15.2	3.7	17.6	19.6	ns
		V _{CC} = 1.4 V to 1.6 V	3.0	5.3	8.4	2.5	9.8	10.7	ns
		V _{CC} = 1.65 V to 1.95 V	2.3	4.4	6.5	2.1	7.7	8.5	ns
		V _{CC} = 2.3 V to 2.7 V	2.1	3.6	5.0	2.0	6.1	6.8	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	3.5	4.4	1.9	4.9	5.5	ns
t _{dis}	disable time	nOE to nY; see Figure 9 ^[4]							
		V _{CC} = 0.8 V	-	60.8	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.3	6.5	9.2	3.7	10.3	11.6	ns
		V _{CC} = 1.4 V to 1.6 V	3.0	5.0	6.5	2.5	7.4	8.4	ns
		V _{CC} = 1.65 V to 1.95 V	3.0	5.3	7.0	2.1	7.4	8.9	ns
		V _{CC} = 2.3 V to 2.7 V	2.1	3.8	4.9	2.0	5.1	6.4	ns
		V _{CC} = 3.0 V to 3.6 V	2.9	5.0	6.2	1.9	6.6	7.4	ns
C_L = 30 pF									
t _{pd}	propagation delay	nA to nY; see Figure 8 ^[2]							
		V _{CC} = 0.8 V	-	37.4	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.8	9.5	19.0	4.4	21.6	24.0	ns
		V _{CC} = 1.4 V to 1.6 V	4.0	6.7	10.8	3.0	13.0	14.5	ns
		V _{CC} = 1.65 V to 1.95 V	2.9	5.6	8.4	2.6	10.3	11.5	ns
		V _{CC} = 2.3 V to 2.7 V	2.7	4.8	6.3	2.5	7.8	8.7	ns
		V _{CC} = 3.0 V to 3.6 V	2.7	4.6	5.8	2.5	7.5	8.3	ns
t _{en}	enable time	nOE to nY; see Figure 9 ^[3]							
		V _{CC} = 0.8 V	-	88.9	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	5.2	9.9	19.8	4.8	22.8	25.3	ns
		V _{CC} = 1.4 V to 1.6 V	4.0	6.8	10.8	3.1	12.6	14.1	ns
		V _{CC} = 1.65 V to 1.95 V	3.0	5.6	8.5	2.8	10.2	11.3	ns
		V _{CC} = 2.3 V to 2.7 V	2.7	4.8	6.5	2.6	7.8	8.8	ns
		V _{CC} = 3.0 V to 3.6 V	2.7	4.6	6.0	2.6	6.9	7.7	ns

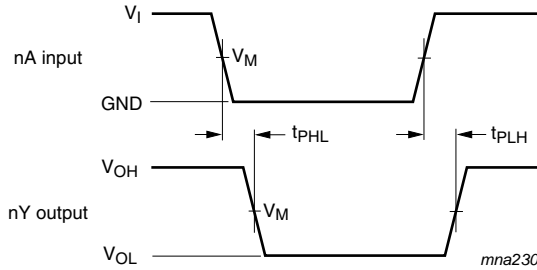
Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C			Unit
			Min	Typ ^[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t _{dis}	disable time	n $\overline{\text{OE}}$ to nY; see Figure 9 ^[4]							
		V _{CC} = 0.8 V	-	49.9	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	6.0	9.9	13.3	4.8	14.8	16.5	ns
		V _{CC} = 1.4 V to 1.6 V	4.4	7.7	9.6	3.1	10.8	12.1	ns
		V _{CC} = 1.65 V to 1.95 V	5.1	8.7	11.1	2.8	12.4	13.8	ns
		V _{CC} = 2.3 V to 2.7 V	3.6	6.2	7.6	2.6	8.6	9.6	ns
		V _{CC} = 3.0 V to 3.6 V	5.2	8.7	10.5	2.6	10.8	13.1	ns
C_L = 5 pF, 10 pF, 15 pF and 30 pF									
C _{PD}	power dissipation capacitance	output enabled; f _i = 1 MHz; ^[5] V _I = GND to V _{CC}							
		V _{CC} = 0.8 V	-	2.7	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	2.8	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	2.9	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	3.0	-	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	3.6	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	4.2	-	-	-	-	pF

- [1] All typical values are measured at nominal V_{CC}.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] t_{en} is the same as t_{PZH} and t_{PZL}.
- [4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms

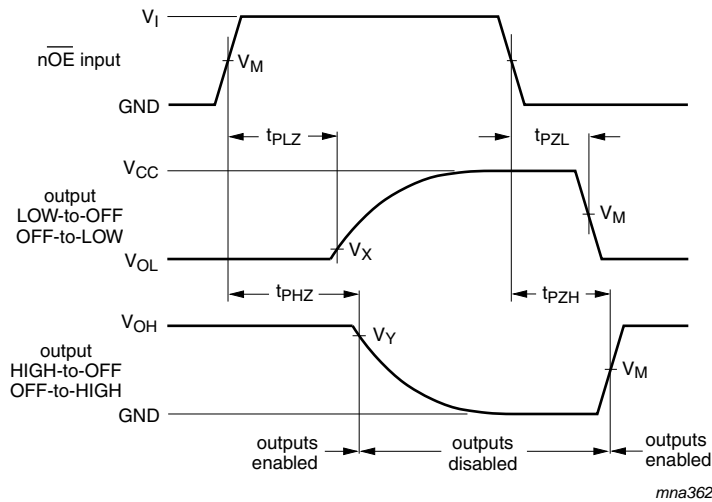


Measurement points are given in [Table 9](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The data input (nA) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns

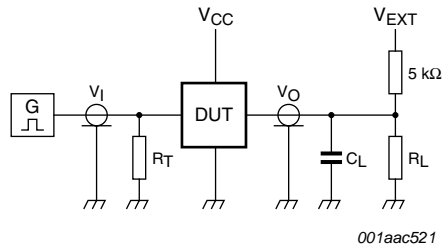


Measurement points are given in [Table 10](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1$ V	$V_{OH} - 0.1$ V
1.65 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
3.0 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V



Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Load		V_{EXT}			
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}	
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$	

[1] For measuring enable and disable times $R_L = 5 \text{ k}\Omega$.

For measuring propagation delays, set-up and hold times, and pulse width, $R_L = 1 \text{ M}\Omega$.

13. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

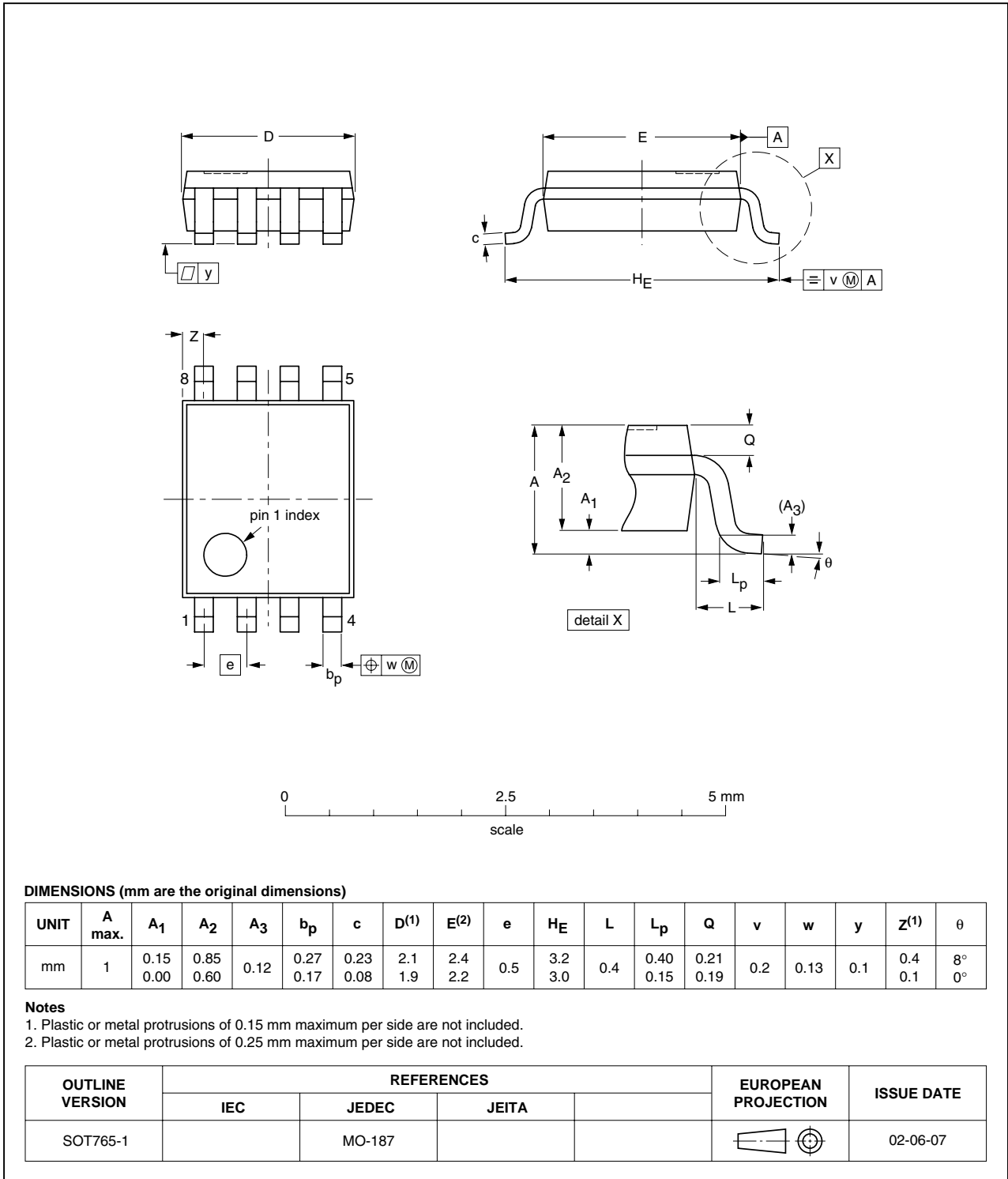


Fig 11. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

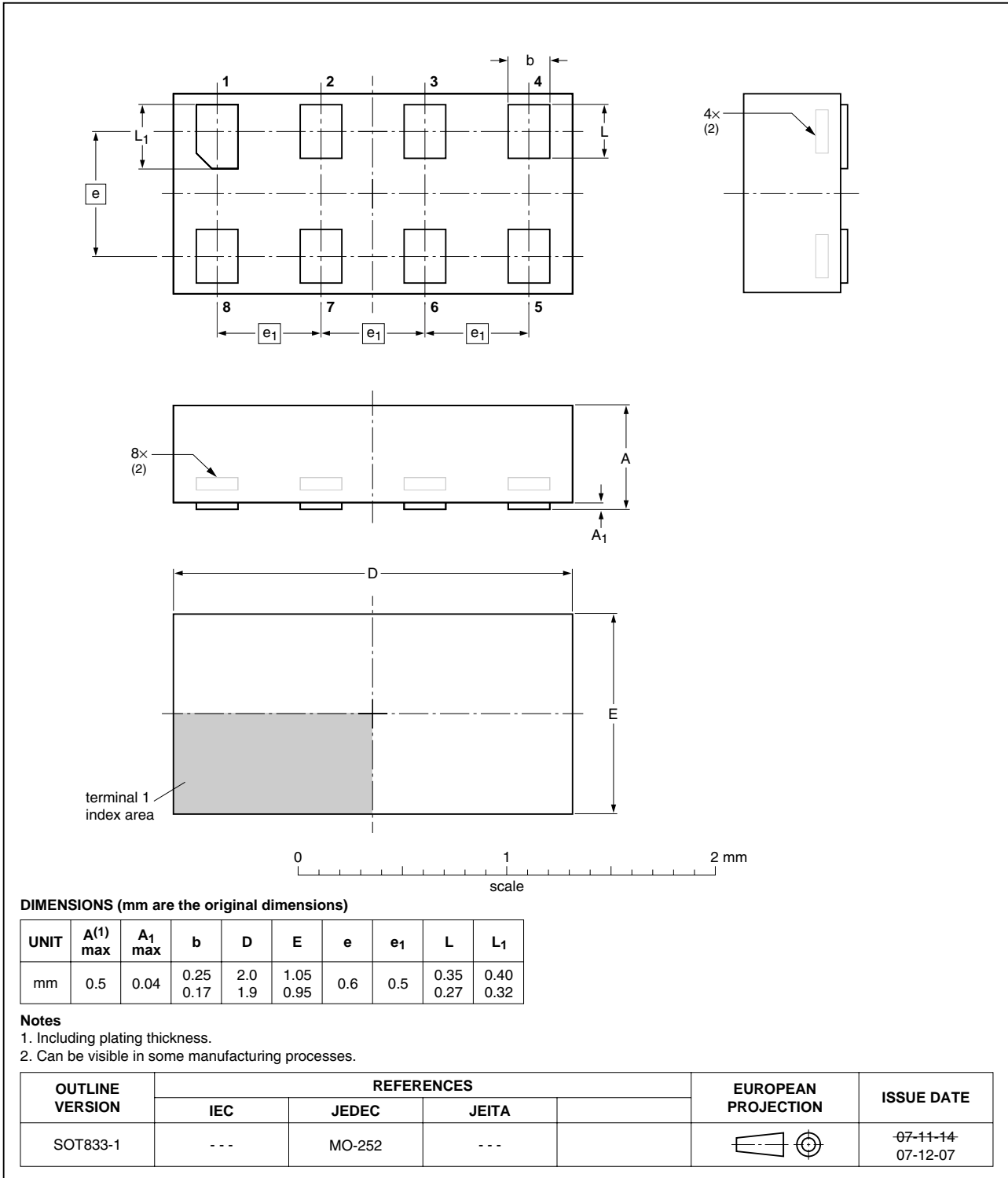


Fig 12. Package outline SOT833-1 (XSON8)

**XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm**

SOT1089

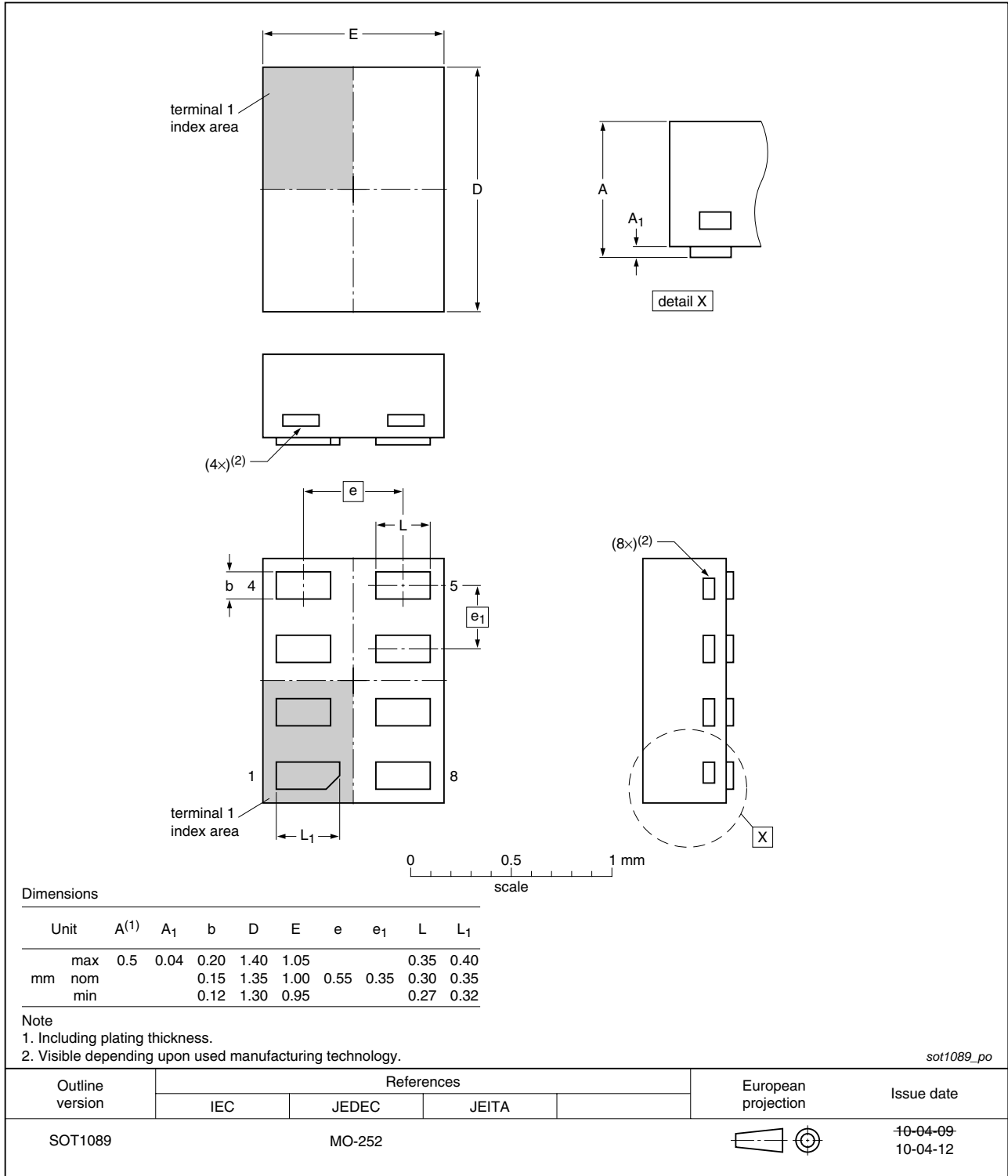


Fig 13. Package outline SOT1089 (XSON8)

XSON8U: plastic extremely thin small outline package; no leads;
8 terminals; UTLP based; body 3 x 2 x 0.5 mm

SOT996-2

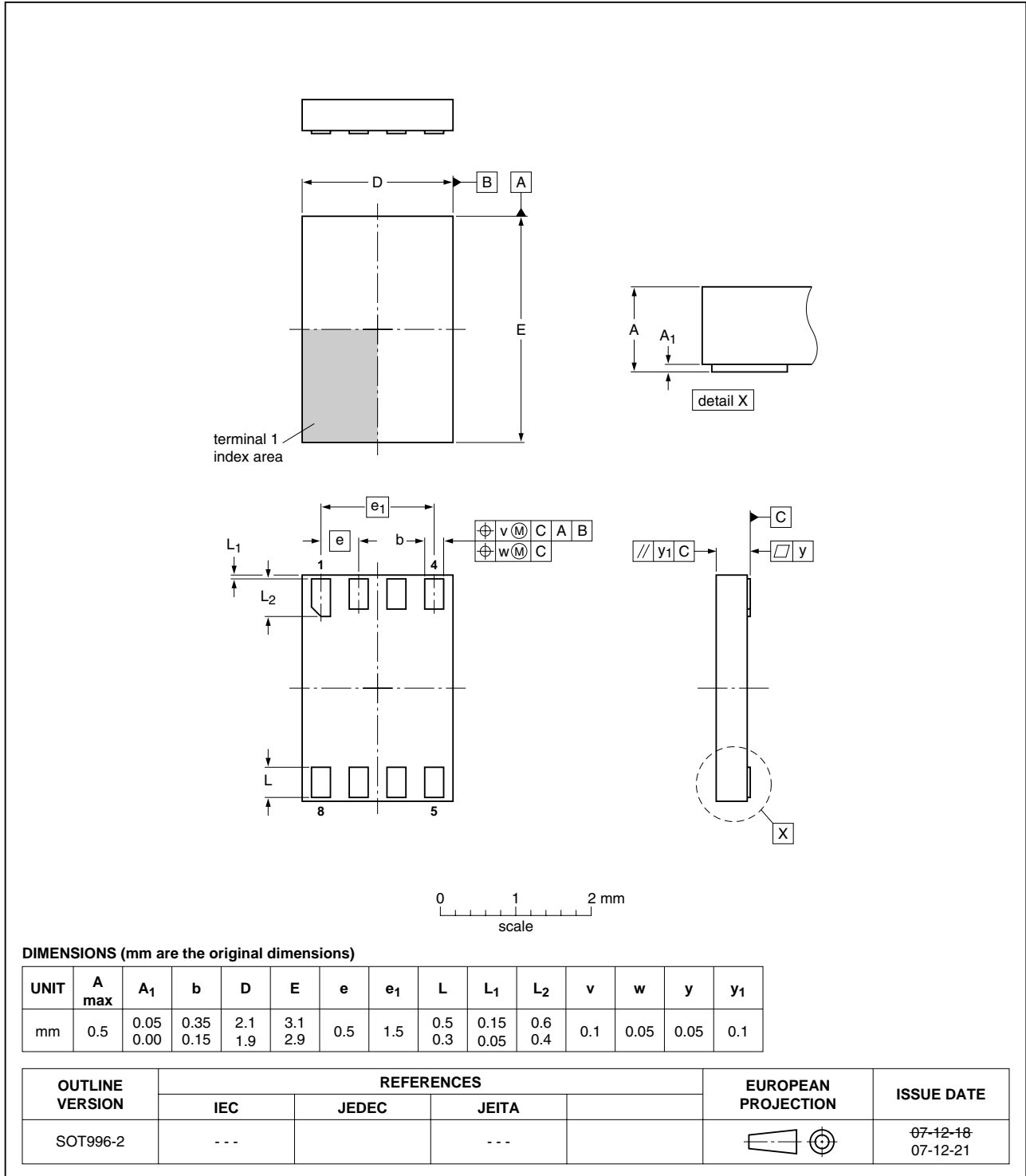


Fig 14. Package outline SOT996-2 (XSON8U)

XQFN8U: plastic extremely thin quad flat package; no leads;
8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

SOT902-1

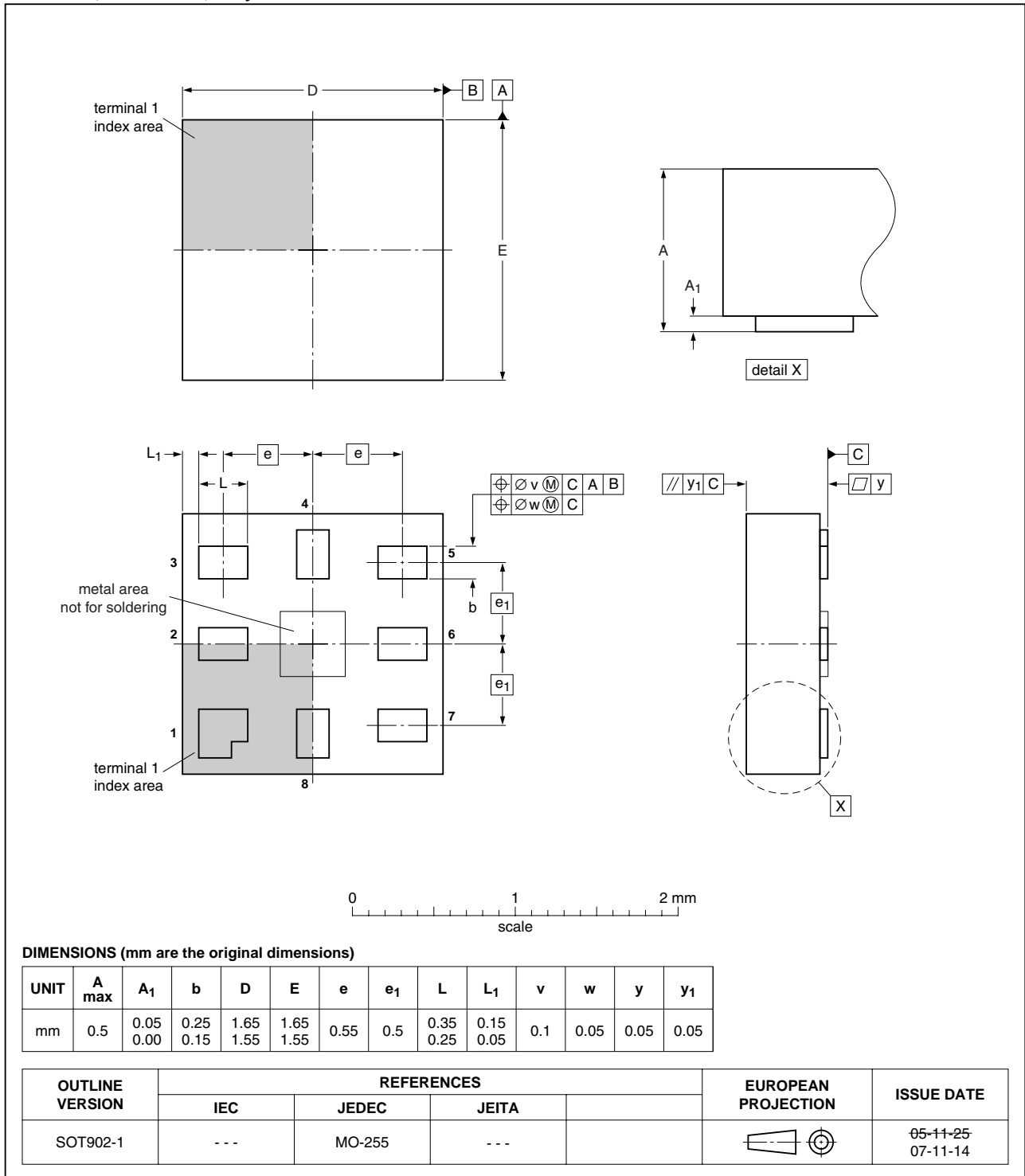


Fig 15. Package outline SOT902-1 (XQFN8U)

**XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm**

SOT1116

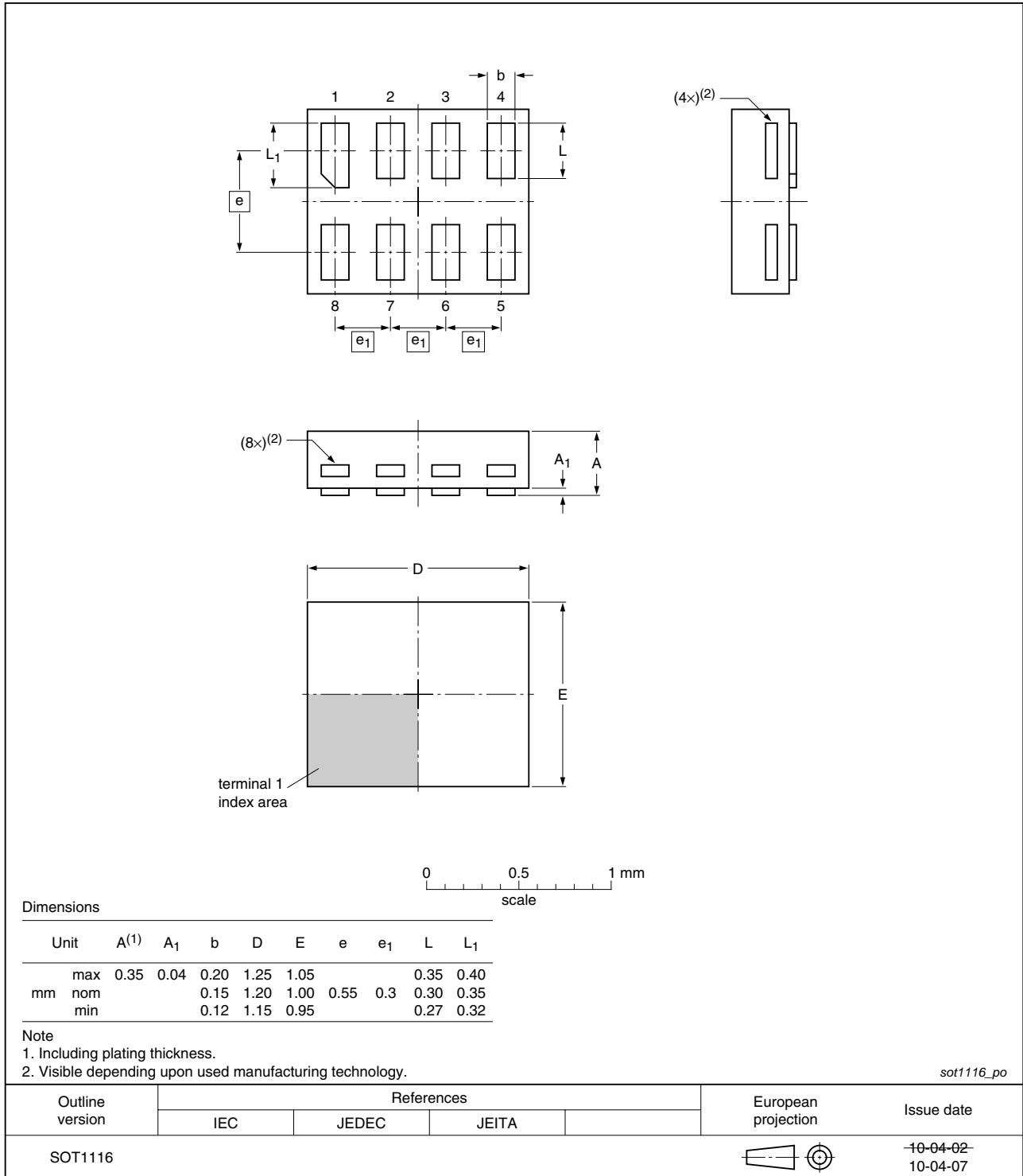


Fig 16. Package outline SOT1116 (XSON8)

**XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm**

SOT1203

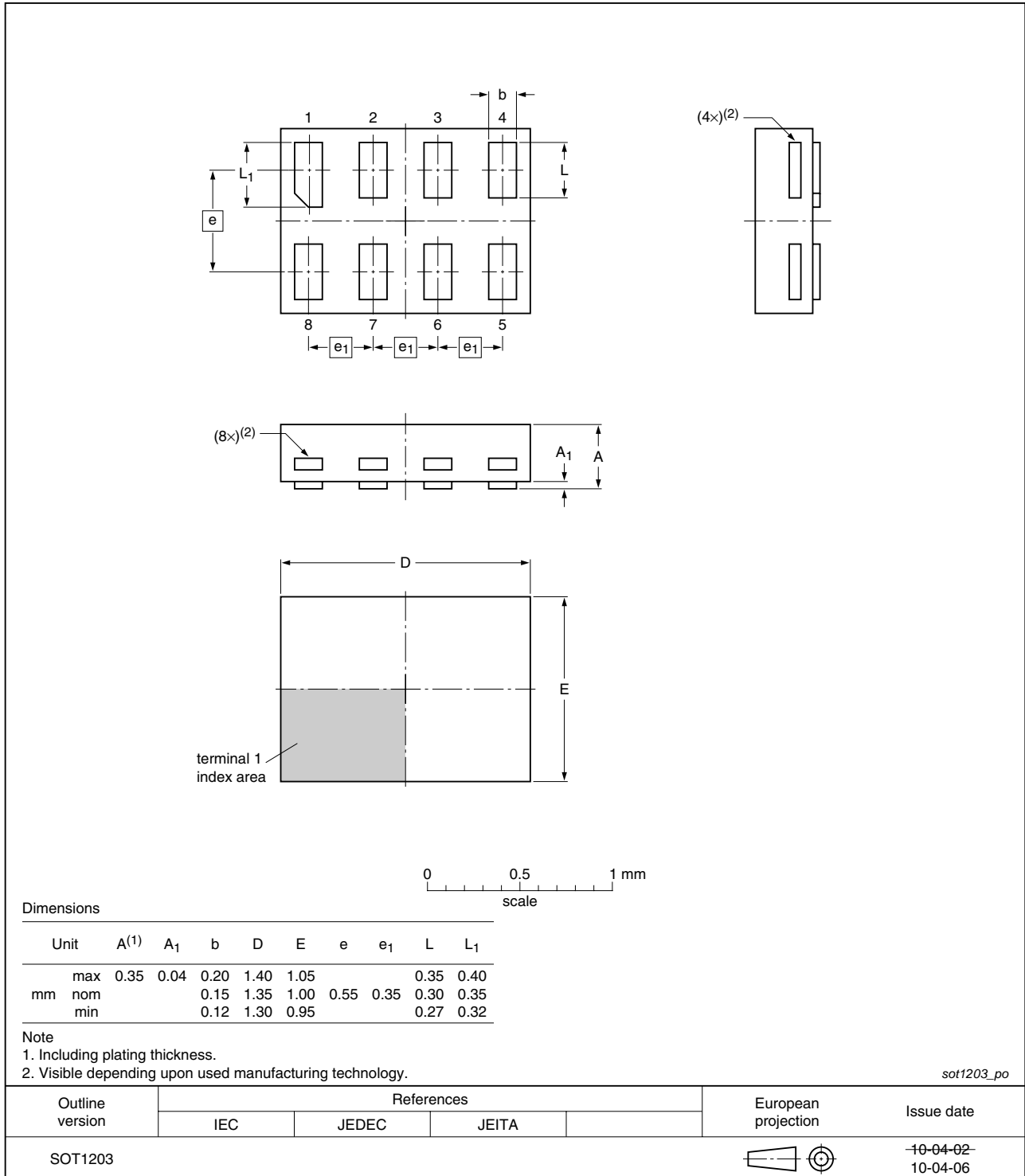


Fig 17. Package outline SOT1203 (XSON8)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G125 v.7	20100921	Product data sheet	-	74AUP2G125 v.6
Modifications:	<ul style="list-style-type: none"> • Added type number 74AUP2G125GN (SOT1116/XSON8 package). • Added type number 74AUP2G125GS (SOT1203/XSON8 package). 			
74AUP2G125 v.6	20091127	Product data sheet	-	74AUP2G125 v.5
74AUP2G125 v.5	20090202	Product data sheet	-	74AUP2G125 v.4
74AUP2G125 v.4	20090122	Product data sheet	-	74AUP2G125 v.3
74AUP2G125 v.3	20080409	Product data sheet	-	74AUP2G125 v.2
74AUP2G125 v.2	20070419	Product data sheet	-	74AUP2G125 v.1
74AUP2G125 v.1	20061017	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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