FAIRCHILD SEMICONDUCTOR®

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# 74ALVC16244
# Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs

## General Description

The ALVC16244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The 74ALVC16244 is designed for low voltage (1.65V to 3.6V) $V_{CC}$ applications with I/O capability up to 3.6V.

The 74ALVC16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

## Features

- 1.65V–3.6V $V_{CC}$ supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$
  - 3.0 ns max for 3.0V to 3.6V $V_{CC}$
  - 3.5 ns max for 2.3V to 2.7V $V_{CC}$
  - 6.0 ns max for 1.65V to 1.95V $V_{CC}$
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latch-up conforms to JEDEC JED98
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

**Note 1:** To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

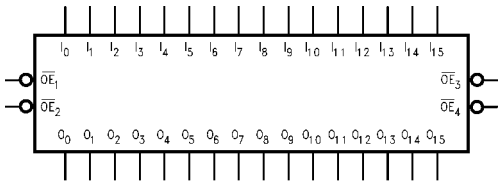
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74ALVC16244GX (Note 2) | BGA54A | 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel] |
| 74ALVC16244MTD (Note 3) | MTD48 | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

**Note 2:** BGA package available in Tape and Reel only.

**Note 3:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

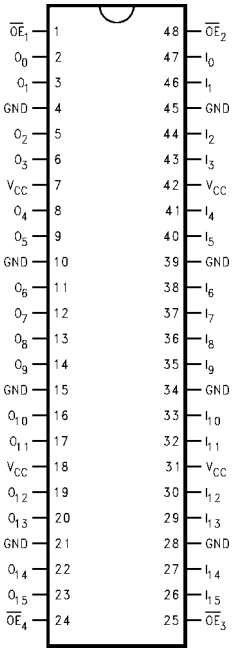
## Logic Symbol



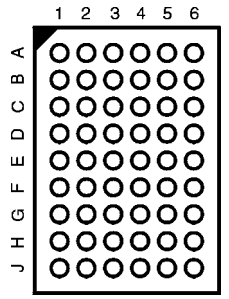

 

## Connection Diagrams

**Pin Assignment for TSSOP**




**Pin Assignment for FBGA**




**(Top Thru View)**

## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Output Enable Input (Active LOW) |
| $I_0$–$I_{15}$ | Inputs |
| $O_0$–$O_{15}$ | Outputs |
| NC | No Connect |

## FBGA Pin Assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | $O_0$ | NC | $\overline{OE}_1$ | $\overline{OE}_2$ | NC | $I_0$ |
| **B** | $O_2$ | $O_1$ | NC | NC | $I_1$ | $I_2$ |
| **C** | $O_4$ | $O_3$ | $V_{CC}$ | $V_{CC}$ | $I_3$ | $I_4$ |
| **D** | $O_6$ | $O_5$ | GND | GND | $I_5$ | $I_6$ |
| **E** | $O_8$ | $O_7$ | GND | GND | $I_7$ | $I_8$ |
| **F** | $O_{10}$ | $O_9$ | GND | GND | $I_9$ | $I_{10}$ |
| **G** | $O_{12}$ | $O_{11}$ | $V_{CC}$ | $V_{CC}$ | $I_{11}$ | $I_{12}$ |
| **H** | $O_{14}$ | $O_{13}$ | NC | NC | $I_{13}$ | $I_{14}$ |
| **J** | $O_{15}$ | NC | $\overline{OE}_4$ | $\overline{OE}_3$ | NC | $I_{15}$ |

## Truth Tables

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_1$ | $I_0$–$I_3$ | $O_0$–$O_3$ |
| L | L | L |
| L | H | H |
| H | X | Z |

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_3$ | $I_8$-$I_{11}$ | $O_8$–$O_{11}$ |
| L | L | L |
| L | H | H |
| H | X | Z |

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_2$ | $I_4$-$I_7$ | $O_4$-$O_7$ |
| L | L | L |
| L | H | H |
| H | X | Z |

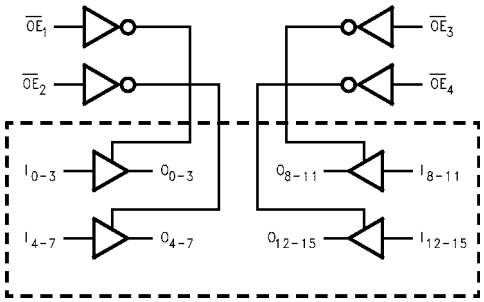
| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_4$ | $I_{12}$-$I_{15}$ | $O_{12}$-$O_{15}$ |
| L | L | L |
| L | H | H |
| H | X | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

## Functional Description

The 74ALVC16244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation.The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

## Logic Diagram



## Absolute Maximum Ratings (Note 4)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +4.6V |
| DC Input Voltage ($V_I$) | −0.5V to 4.6V |
| Output Voltage ($V_O$) (Note 5) | −0.5V to $V_{CC}$ +0.5V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ < 0V | −50 mA |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ < 0V | −50 mA |
| DC Output Source/Sink Current | |
| ($I_{OH}$/$I_{OL}$) | ±50 mA |
| DC $V_{CC}$ or GND Current per | |
| Supply Pin ($I_{CC}$ or GND) | ±100 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |

## Recommended Operating Conditions (Note 6)

| | |
|---|---|
| Power Supply | |
| Operating | 1.65V to 3.6V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Free Air Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate ($\Delta t/\Delta V$) | |
| $V_{IN}$ = 0.8V to 2.0V, $V_{CC}$ = 3.0V | 10 ns/V |

**Note 4:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 5:** $I_O$ Absolute Maximum Rating must be observed, limited to 4.6V.

**Note 6:** Floating or unused control inputs must be held HIGH or LOW.

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | Min | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH Level Input Voltage | | 1.65 - 1.95 | 0.65 x $V_{CC}$ | | V |
| | | | 2.3 - 2.7 | 1.7 | | |
| | | | 2.7 - 3.6 | 2.0 | | |
| $V_{IL}$ | LOW Level Input Voltage | | 1.65 - 1.95 | | 0.35 x $V_{CC}$ | V |
| | | | 2.3 - 2.7 | | 0.7 | |
| | | | 2.7 - 3.6 | | 0.8 | |
| $V_{OH}$ | HIGH Level Output Voltage | $I_{OH}$ = −100 μA | 1.65 - 3.6 | $V_{CC}$ - 0.2 | | V |
| | | $I_{OH}$ = −4 mA | 1.65 | 1.2 | | |
| | | $I_{OH}$ = −6 mA | 2.3 | 2.0 | | |
| | | $I_{OH}$ = −12 mA | 2.3 | 1.7 | | |
| | | | 2.7 | 2.2 | | |
| | | | 3.0 | 2.4 | | |
| | | $I_{OH}$ = −24 mA | 3.0 | 2 | | |
| $V_{OL}$ | LOW Level Output Voltage | $I_{OL}$ = 100 μA | 1.65 - 3.6 | | 0.2 | V |
| | | $I_{OL}$ = 4 mA | 1.65 | | 0.45 | |
| | | $I_{OL}$ = 6 mA | 2.3 | | 0.4 | |
| | | $I_{OL}$ = 12 mA | 2.3 | | 0.7 | |
| | | | 2.7 | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3.0 | | 0.55 | |
| $I_I$ | Input Leakage Current | 0 ≤ $V_I$ ≤ 3.6V | 3.6 | | ±5.0 | μA |
| $I_{OZ}$ | 3-STATE Output Leakage | 0 ≤ $V_O$ ≤ 3.6V | 3.6 | | ±10 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6 | | 40 | μA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH}$ = $V_{CC}$ − 0.6V | 3 - 3.6 | | 750 | μA |

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$ | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $C_L = 50$ pF | | | | $C_L = 30$ pF | | | | |
| | | $V_{CC} = 3.3V \pm 0.3V$ | | $V_{CC} = 2.7V$ | | $V_{CC} = 2.5V \pm 0.2V$ | | $V_{CC} = 1.8V \pm 0.15V$ | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay | 1.3 | 3 | 1.5 | 3.5 | 1.0 | 3.0 | 1.5 | 6.0 | ns |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time | 1.3 | 4.0 | 1.5 | 4.6 | 1.0 | 4.1 | 1.5 | 8.2 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | 1.3 | 4.0 | 1.5 | 4.3 | 1.0 | 3.8 | 1.5 | 6.8 | ns |

## Capacitance

| Symbol | Parameter | | Conditions | $T_A = +25°C$ | | Units |
|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ | Typical | |
| $C_{IN}$ | Input Capacitance | | $V_I = 0V$ or $V_{CC}$ | 3.3 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | | $V_I = 0V$ or $V_{CC}$ | 3.3 | 7 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | Outputs Enabled | f = 10 MHz, $C_L = 0$ pF | 3.3 | 20 | pF |
| | | | | 2.5 | 20 | |

## AC Loading and Waveforms

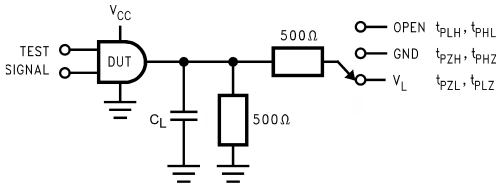



**FIGURE 1. AC Test Circuit**

**Table 1: Values for Figure 1**

| TEST | SWITCH |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | $V_L$ |
| $t_{PZH}$, $t_{PHZ}$ | GND |

**Table 2: Variable Matrix**
**(Input Characteristics: f = 1MHz; $t_r = t_f$ = 2ns; $Z_0$ = 50Ω)**

| Symbol | $V_{CC}$ | | | |
|---|---|---|---|---|
| | **3.3V ± 0.3V** | **2.7V** | **2.5V ± 0.2V** | **1.8V ± 0.15V** |
| $V_{mi}$ | 1.5V | 1.5V | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_{mo}$ | 1.5V | 1.5V | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_X$ | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.15V | $V_{OL}$ + 0.15V |
| $V_Y$ | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.15V | $V_{OH}$ − 0.15V |
| $V_L$ | 6V | 6V | $V_{CC}$*2 | $V_{CC}$*2 |

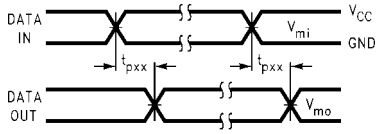



**FIGURE 2. Waveform for Inverting and Non-Inverting Functions**

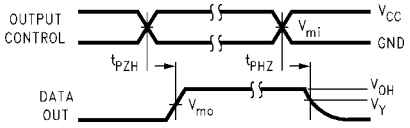



**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**

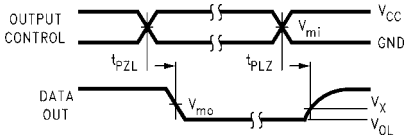
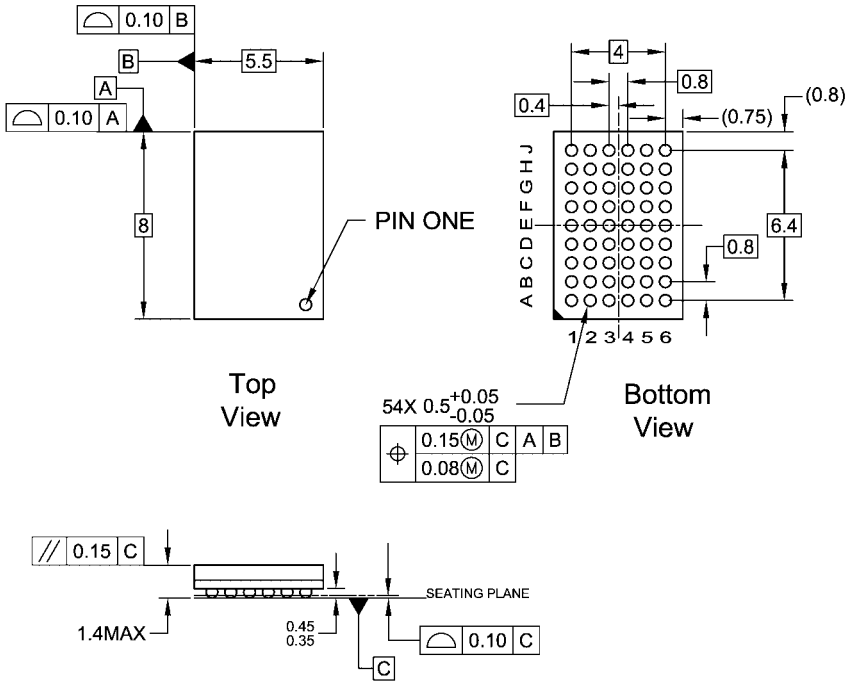



**FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic**

## Physical Dimensions inches (millimeters) unless otherwise noted



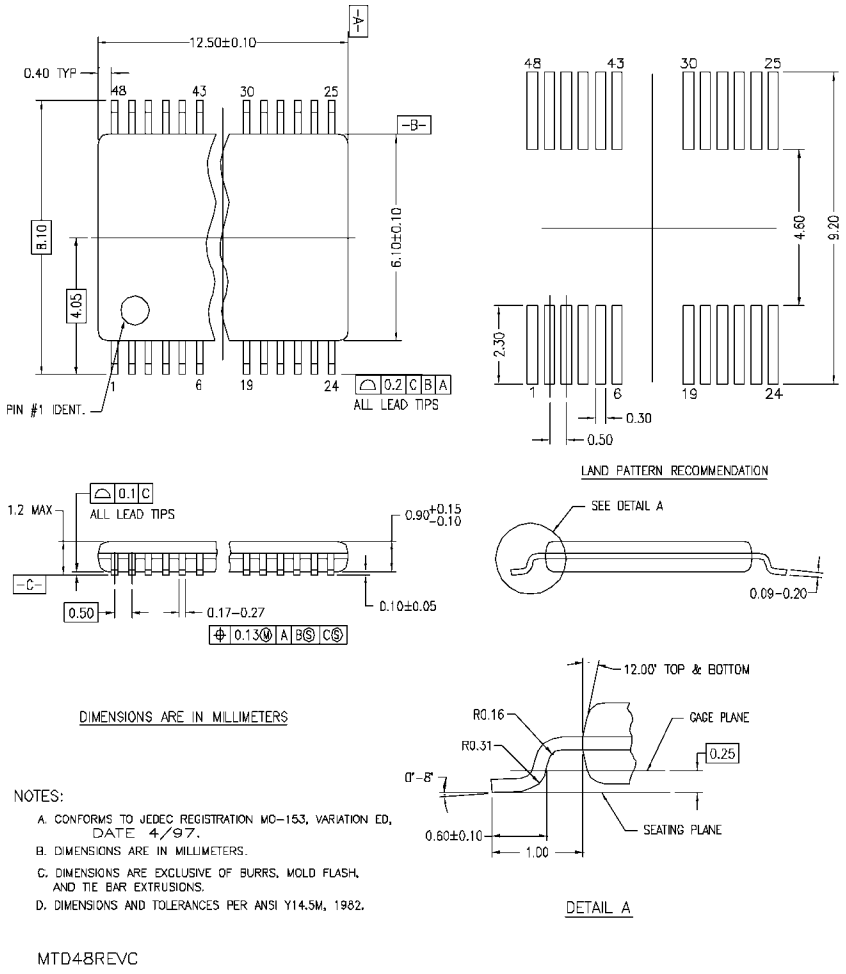

NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide**
**Package Number BGA54A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD48**



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