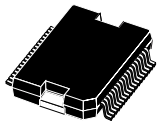
STA500

30V 3.5A QUAD POWER HALF BRIDGE

- MINIMUM INPUT OUTPUT PULSE WIDTH DISTORTION
- 200mΩ R_{dsON} COMPLEMENTARY DMOS OUTPUT STAGE
- CMOS COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- THERMAL WARNING OUTPUT
- OVERVOLTAGE, UNDERVOLTAGE PROTECTION

MULTIPOWER BCD TECHNOLOGY



PowerSO36

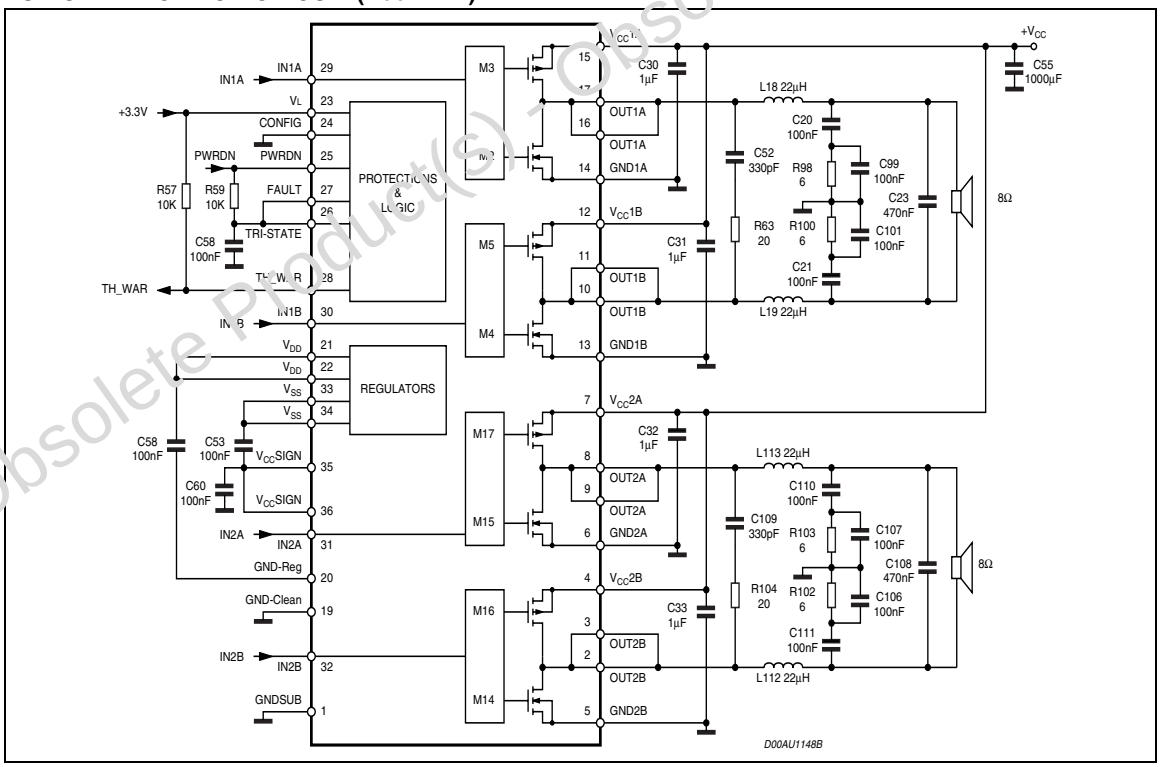
ORDERING NUMBER: STA500

DESCRIPTION

STA500 is a monolithic quad half bridge stage in Multipower BCD Technology. The device can be used as dual bridge or reconfigured, by connecting CONFIG pin to Vdd pin, as single bridge with double current capability, and as half bridge (Binary mode) with half current capability.

The device is particulary designed to make the output stage of a stereo All-Digital High Efficiency (DDX™) amplifier capable to deliver 20 + 30W output power on 8Ω load and 60W on 8Ω load in bridge BTL configuration or more 60W on 4Ω load. The input pins have threshold proportional to Ibias pin voltage.

AUDIO APPLICATION CIRCUIT (Dual BTL)



Rev. 7

PIN FUNCTION

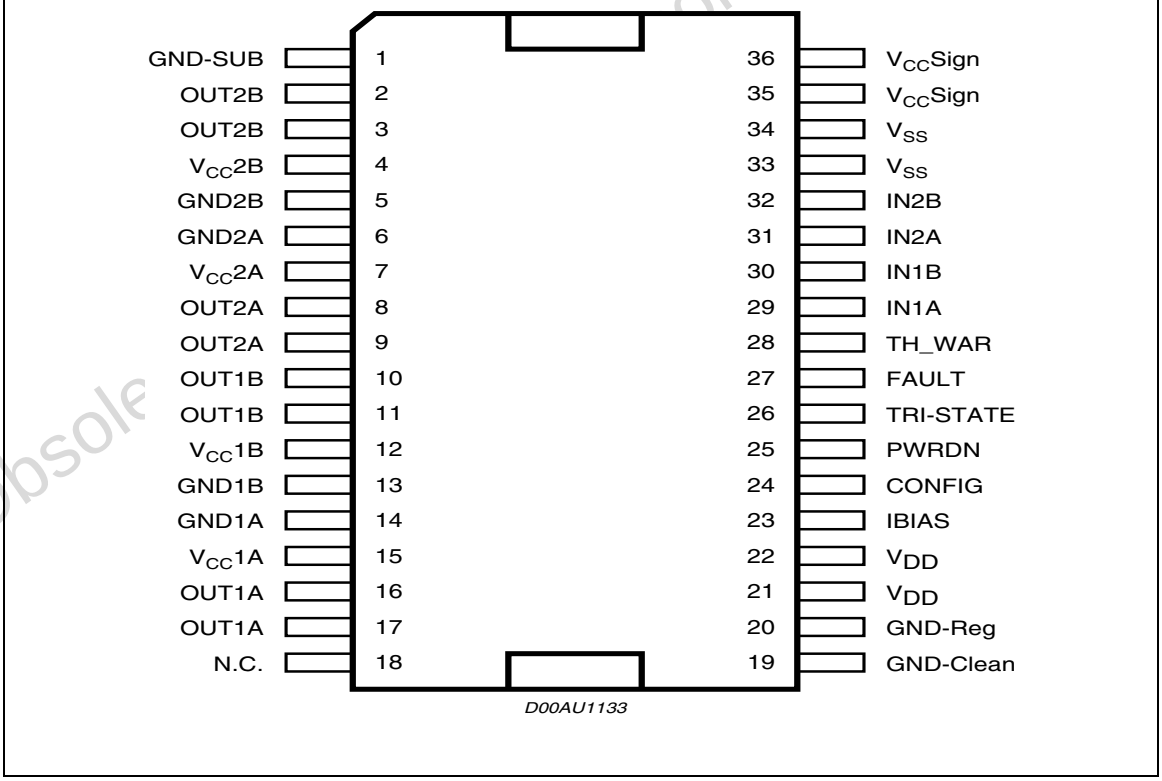
N°	Pin	Description
1	GND-SUB	Substrate ground
35 ; 36	Vcc Sign	Signal Positive supply
15	Vcc1A	Positive Supply
12	Vcc1B	Positive Supply
7	Vcc2A	Positive Supply
4	Vcc2B	Positive Supply
14	GND1A	Negative Supply
13	GND1B	Negative Supply
6	GND2A	Negative Supply
5	GND2B	Negative Supply
16 ; 17	OUT1A	Output half bridge 1A
10 ; 11	OUT1B	Output half bridge 1B
8 ; 9	OUT2A	Output half bridge 2A
2 ; 3	OUT2B	Output half bridge 2B
29	IN1A	Input of half bridge 1A
30	IN1B	Input of half bridge 1B
31	IN2A	Input of half bridge 2A
32	IN2B	Input of half bridge 2B
21 ; 22	Vdd	5V Regulator referred to ground
33 ; 34	Vss	5V Regulator referred to +Vcc
25	PWRDN	Stand-by pin (Control input)
26	TRI-STATE	Hi-Z pin (Control input)
27	FAULT	Fault pin advisor (Open Collector Output)
24	CONFIG	Configuration setting pin
28	TH-WAR	Thermal warning advisor (Open Collector Output)
19	GND-clean	Logical ground
23	IBIAS	High logical state setting voltage
18	NC	Not connected
20	GND-Reg	Ground for Vdd regulator

FUNCTIONAL PIN STATUS

PIN NAME	Logical value	IC -STATUS
FAULT	0	Fault detected (Short circuit, or Thermal ..)
FAULT (*)	1	Normal Operation
TRI-STATE	0	All powers in Hi-Z state
TRI-STATE	1	Normal operation
PWRDN	0	Low absorpion
PWRDN	1	Normal operation
THWAR	0	Temperature of the IC =130°C
THWAR(*)	1	Normal operation
CONFIG	0	Normal Operation
CONFIG(**)	1	OUT1A=OUT1B ; OUT2A=OUT2B (IF IN1A = IN1B; IN2A = IN2B)

(*) : The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.
(**:) To put CONFIG = 1 means connect Pin 24 (CONFIG) to Pins 21, 22 (Vdd)

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CE}	DC Supply Voltage (Pin 4,7,12,15)	40	V
V_{max}	Maximum Voltage on pins (23 to 32)	5.5	V
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{j\text{-}case}$	Thermal Resistance Junction to Case (thermal pad)			2.5	°C/W
T_{jSD}	Thermal shut-down junction temperature		150		°C
T_{warn}	Thermal warning temperature		130		°C
t_{hSD}	Thermal shut-down hysteresis		25		°C

ELECTRICAL CHARACTERISTCS

(Ibias = 3.3V; Vcc = 28V; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{dsON}	Power Pchannel/Nchannel MOSFET R_{dsON}	Id=1A;		200	270	mΩ
I_{dss}	Power Pchannel/Nchannel leakage I_{dss}	Vcc=35V			50	µA
g_N	Power Pchannel RdsON Matching (*)	Id=1A	95			%
g_P	Power Nchannel RdsON Matching (*)	Id=1A	95			%
Dt_s	Low current Dead Time (static)	see test circuit no.1; see fig. 1		10	20	ns
Dt_d	High current Dead Time (dinamic)	L=22µH; C = 470nF; Rl = 8Ω Id = 3.5A; see fig. 3			50	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load			100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load			100	ns
t_r	Rise time	Resistive load; as fig. 1			25	ns
t_f	Fall time	Resistive load; as fig. 1			25	ns
V_{CC}	Supply voltage operating voltage		9		V_{OV}	V
$V_{IN\text{-}H}$	High level input voltage		Ibias/2 +300mV			V
$V_{IN\text{-}L}$	Low level input voltage				Ibias/2 -300mV	V
$I_{IN\text{-}H}$	Hi level Input current	Pin voltage=Ibias		1		µA
$I_{IN\text{-}L}$	Low level input current	Pin voltage = 0.3V		1		µA
$I_{PWRDN\text{-}H}$	Hi level PWRDN pin input current	Ibias = 3.3V		35		µA
V_L	Low logical state voltage VL (pin PWRDN, TRISTATE) (note 1)	Ibias = 3.3V			0.8	V
V_H	High logical state voltage VH (pin PWRDN, TRISTATE) (note 1)	Ibias = 3.3V	1.7			V

ELECTRICAL CHARACTERISTCS (continued)
(Ibias = 3.3V; Vcc = 28V; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{VCC-PWRDN}$	Supply current from Vcc in Power Down	PWRDN = 0			3	mA
I_{FAULT}	Output Current pins FAULT -TH-WARN when FAULT CONDITIONS	Vpin = 3.3V		1		mA
$I_{VCC-hiz}$	Supply current from Vcc in Tri-state	Tri-state=0		22		mA
I_{VCC}	Supply current from Vcc in operation (both channel switching)	Input pulse width = 50% Duty; Switching Frequency = 384Khz; No LC filters;		80		mA
I_{OUT-SH}	Overcurrent Protection Threshold (short circuit current limit) (note 2)		3.5	6	8	A
V_{OV}	Overvoltage protection threshold		30	35	40	V
V_{UV}	Undervoltage protection threshold			7		V
t_{pw_min}	Output minimum pulse width	No Load	70		150	ns

Notes: 1. The following table explains the VL, VH variation with Ibias

Ibias	VLmax	VHmin	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Note 2: If used in single BTL configuration, the device may be not short circuit protected

LOGIC TRUTH TABLE (see fig. 2)

TRI-STATE	INxA	INxB	Q1	Q2	Q3	Q4	OUTPUT MODE
0	X	X	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 1. Test Circuit.

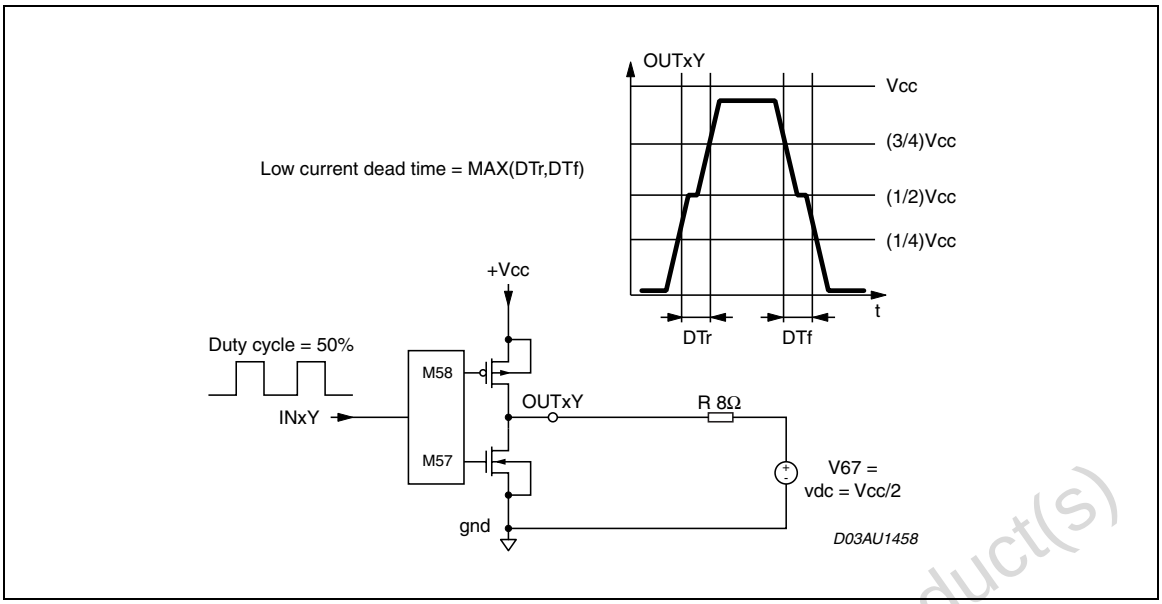


Figure 2.

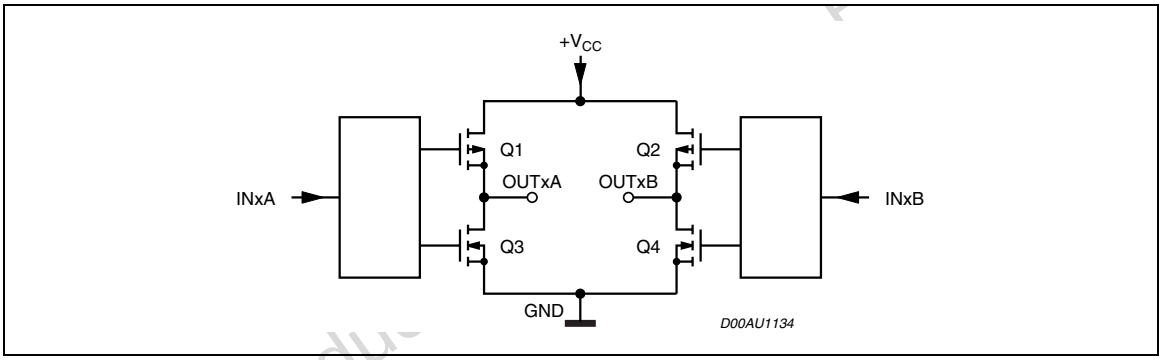


Figure 3.

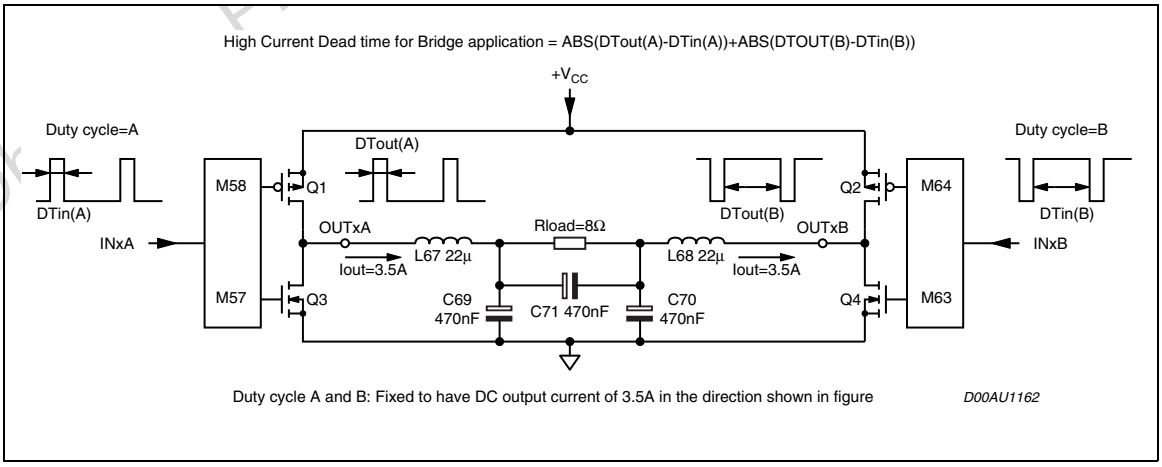
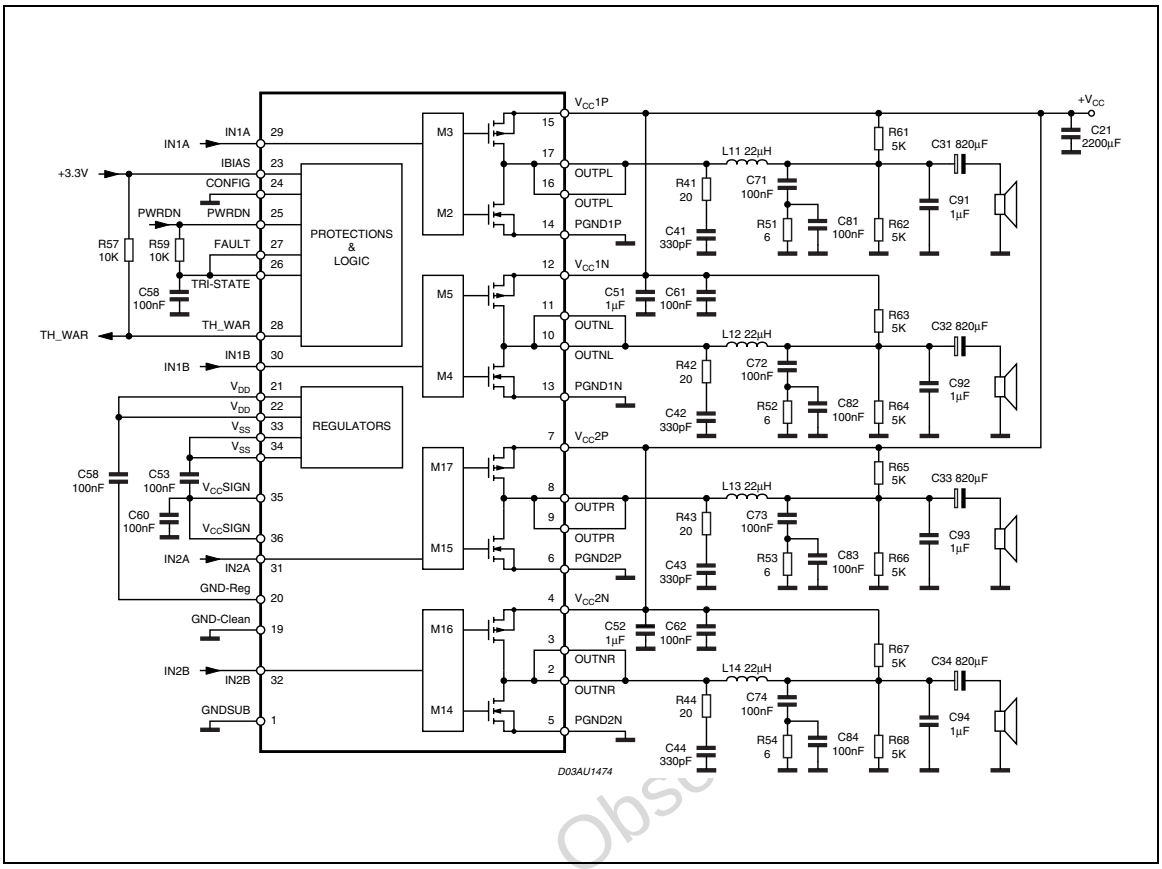


Figure 4. Typical Quad Half Bridge Configuration



Note:

The diagran showed below, have been obtained using the demonstration board described in the application Note AN1456 (STA304 + STA500 Digital Audioprocessor evolution board evaluating manual - Jan 2002), refer to the schematic shown in fig. 1).

For the Quad Half Bridge Configuration (fig. 4), refers to the application note AN1661 (STA308 Half Bridge Board - March 2003)

Figure 5. Distortion vs Output Power (STA304A+STA500)

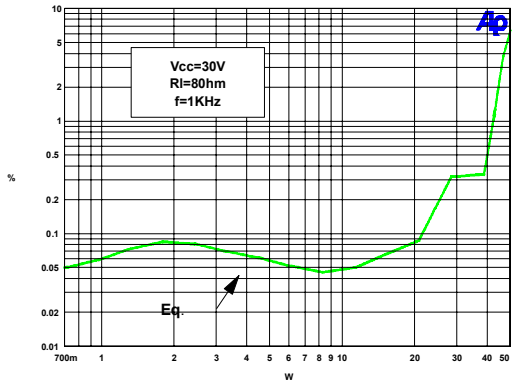


Figure 6. Tolal Power Dissipation & Efficiency vs Output Power

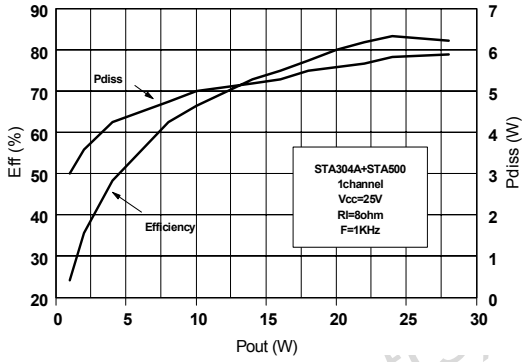


Figure 7. Output Power vs Supply Voltage (STA304A+STA500)

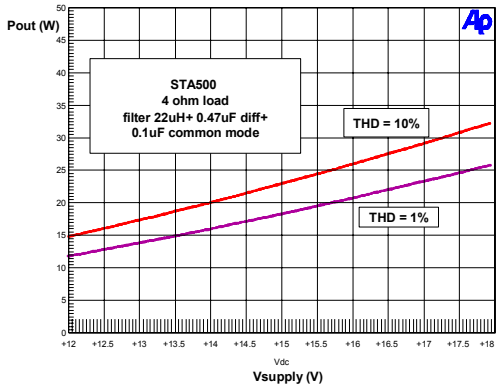
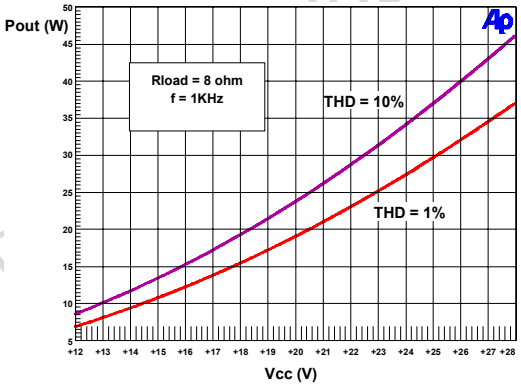


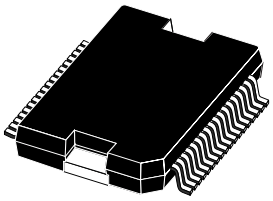
Figure 8. Output Power vs Supply Voltage (STA304A+STA500)



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10			0.0039
b	0.22		0.38	0.0087		0.0150
c	0.23		0.32	0.0091		0.0126
D	15.80		16.00	0.6220		0.6299
D1	9.40		9.80	0.3701		0.3858
E	13.90		14.5	0.5472		0.5709
E1	10.90		11.10	0.4291		0.4370
E2			2.90			0.1142
E3	5.80		6.20	0.2283		0.2441
e		0.65			0.0256	
e3		11.05			0.4350	
G	0		0.10			0.0039
H	15.50		15.90	0.6102		0.6260
h			1.10			0.0433
L	0.8		1.10	0.0315		0.0433
N	10° (max)					
s	8° (max)					

Note: “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



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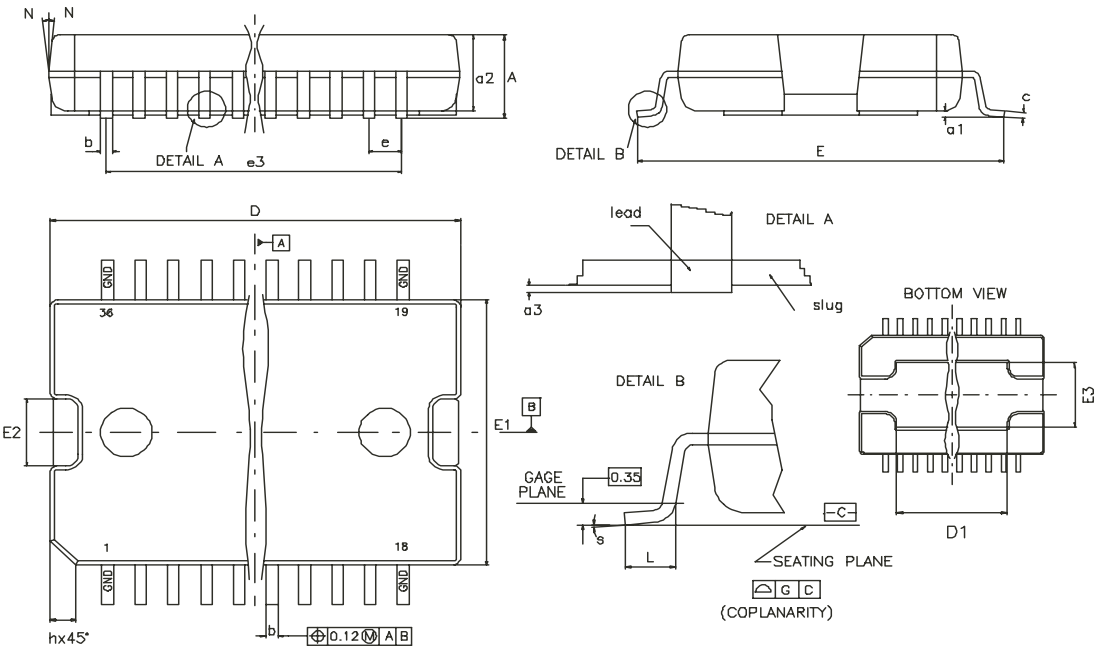

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Table 1. Revision History

Date	Revision	Description of Changes
July 2003	6	First Issue
January 2006	7	Modified in the Electrical Characteristics table (page 4) the values of V_{IN-H}, V_{IN-L}, V_L & V_H parameters. Modified the notes 1(page 5).