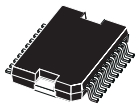
TDA7266D

5W+5W DUAL BRIDGE AMPLIFIER

PRELIMINARY DATA

- WIDE SUPPLY VOLTAGE RANGE (3.5 - 12V)
- OUTPUT POWER
  5+5W @THD = 10%, R_L = 8Ω, V_{CC} = 9.5V
- SINGLE SUPPLY
- MINIMUM EXTERNAL COMPONENTS
  - NO SVR CAPACITOR
  - NO BOOTSTRAP
  - NO BOUCHEROT CELLS
  - INTERNALLY FIXED GAIN
- STAND-BY & MUTE FUNCTIONS
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION

TECHNOLOGY BI20II

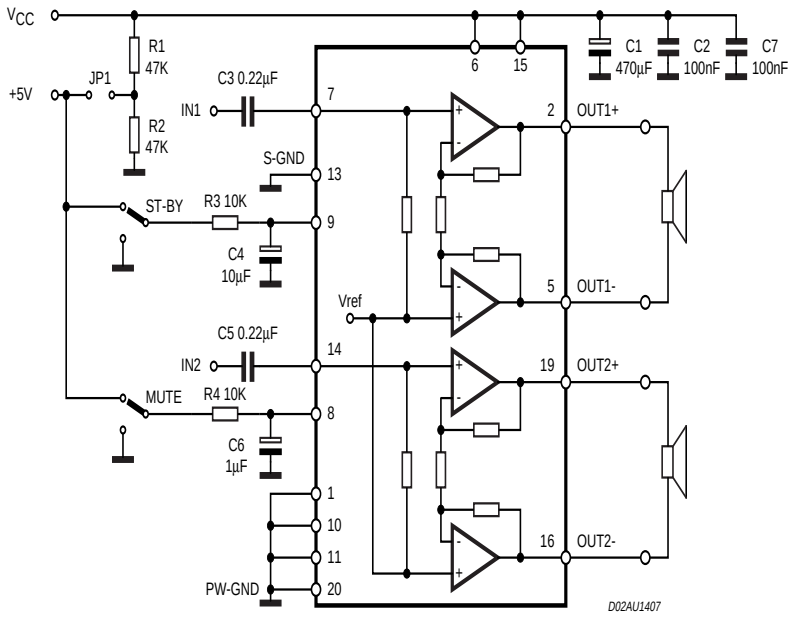


PowerSO20 Slug Down
ORDERING NUMBER: TDA7266D

DESCRIPTION

The TDA7266D is a dual bridge amplifier specially designed for LCD TV/Monitor, PC Motherboard, TV and Portable Audio applications.

TEST AND APPLICATION CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

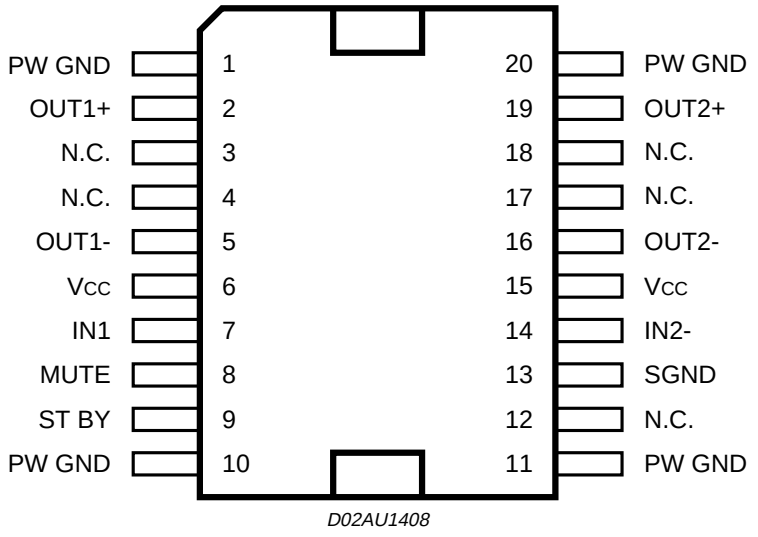
Symbol	Parameter	Value	Unit
V_S	Supply Voltage	20	V
I_O	Output Peak Current (internally limited)	1.5	A
P_{tot}	Total Power Dissipation (T_{amb} = 70°C	25	W
T_{op}	Operating Temperature	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	2.1	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (on recomended PCB) note1	15	°C/W

Notes: 1. See Application note AN668, available on WEB FR4 with 15 via holes and ground layer.

PIN CONNECTION



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ELECTRICAL CHARACTERISTCS (Refer to test circuit) V_{CC} = 9.5V, R_L = 8Ω, f = 1KHz, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Range		3.5	9.5	12	V
I_q	Total Quiescent Current			50	60	mA
V_{OS}	Output Offset Voltage				120	mV
P_O	Output Power	THD 10%	4.3	5		W
THD	Total Harmonic Distortion	P_O = 1W		0.05	0.2	%
		P_O = 0.1W to 2W f = 100Hz to 15KHz			1	%
SVR	Supply Voltage Rejection	f = 100Hz, VR =0.5V	40	56		dB
CT	Crosstalk		46	60		dB
A_{MUTE}	Mute Attenuation		60	80		dB
T_w	Thermal Threshold			150		°C
G_V	Closed Loop Voltage Gain		25	26	27	dB
ΔG_V	Voltage Gain Matching				0.5	dB
R_i	Input Resistance		25	30		KΩ
VT_{MUTE}	Mute Threshold	for V_{CC} > 6.4V; Vo = -30dB	2.3	2.9	4.1	V
		for V_{CC} < 6.4V; Vo = -30dB	$V_{CC}/2$ -1	$V_{CC}/2$ -0.75	$V_{CC}/2$ -0.5	V
VT_{ST-BY}	St-by Threshold		0.8	1.3	1.8	V
I_{ST-BY}	St-by Current V6 = GND				100	µA
e_N	Total Output Voltage	A Curve		150		µV

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APPLICATIVE SUGGESTIONS

STAND-BY AND MUTE FUNCTIONS

(A) Microprocessor Application

In order to avoid annoying "Pop-Noise" during Turn-On/Off transients, it is necessary to guarantee the right St-by and mute signals sequence.It is quite simple to obtain this function using a microprocessor (Fig. 1 and 2).

At first St-by signal (from µP) goes high and the voltage across the St-by terminal (Pin 9) starts to increase exponentially. The external RC network is intended to turn-on slowly the biasing circuits of the amplifier, this to avoid "POP" and "CLICK" on the outputs.

When this voltage reaches the St-by threshold level, the amplifier is switched-on and the external capacitors in series to the input terminals (C1, C3) start to charge.

It's necessary to mantain the mute signal low until the capacitors are fully charged, this to avoid that the device goes in play mode causing a loud "Pop Noise" on the speakers.

A delay of 100-200ms between St-by and mute signals is suitable for a proper operation.

Figure 1. Microprocessor Application

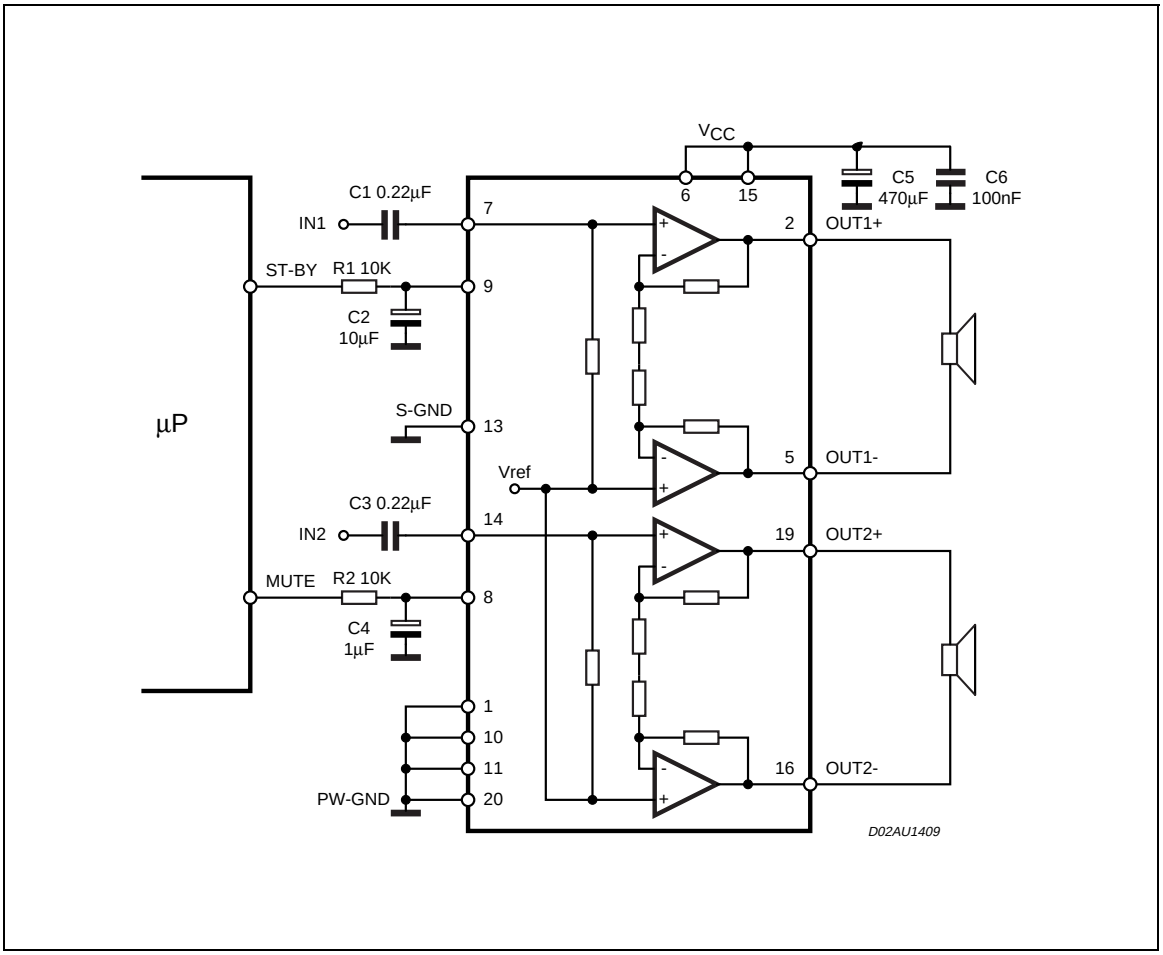

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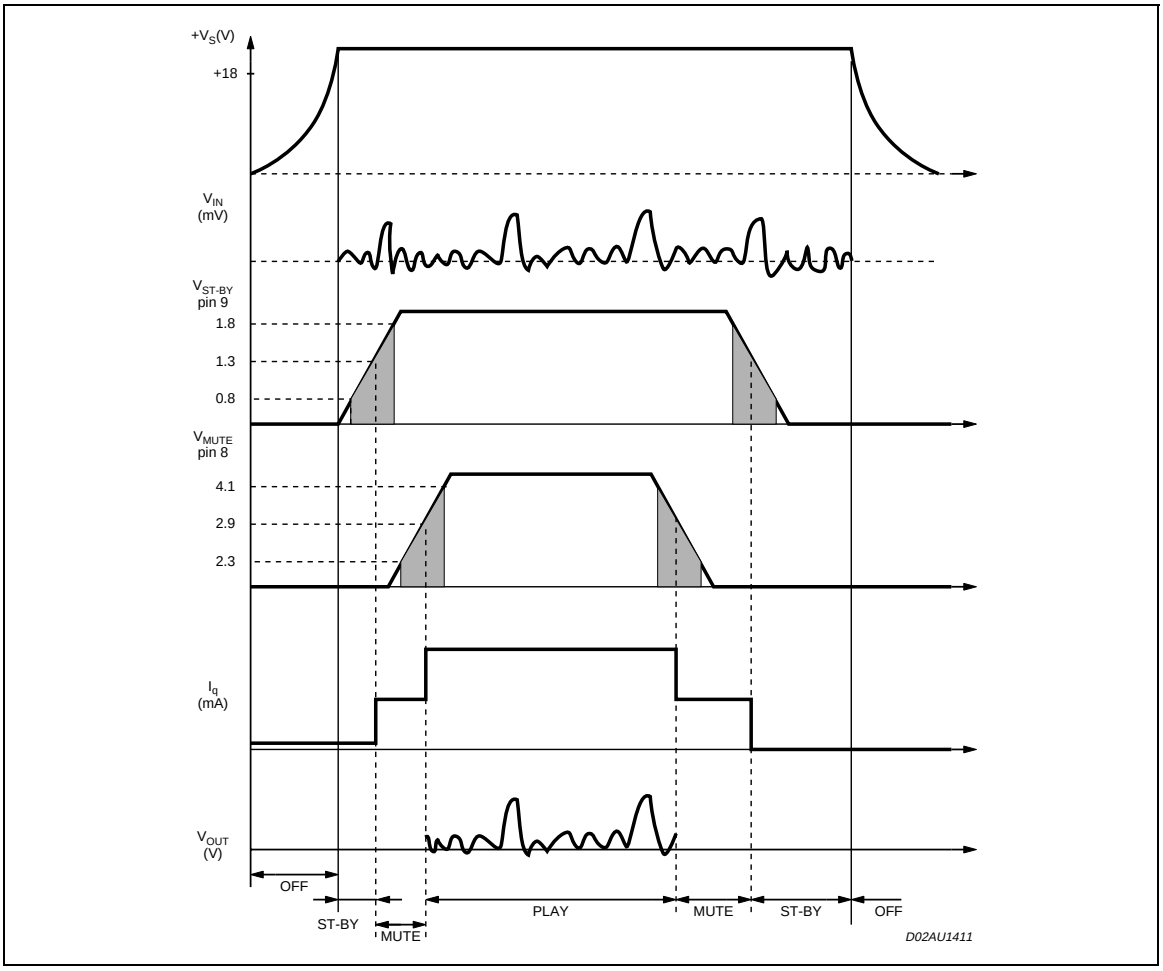
Figure 2. Microprocessor Driving Signals



B) Low Cost Application

In low cost applications where the mP is not present, the suggested circuit is shown in fig.3.

The St-by and mute terminals are tied together and they are connected to the supply line via an external voltage divider.

The device is switched-on/off from the supply line and the external capacitor C4 is intended to delay the St-by and mute threshold exceeding, avoiding "Popping" problems.
So to avoid any popping or clicking sond, it is important to clock:

a **Correct Sequence:** At turn-ON, the Stand-by must be removed at first, then the Mute must be released after a delay of about 100-200ms. On the contrary at turn-OFF the Mute must be activated as first and then the Stand-by.
With the values suggested in the Application circuit the right operation is guaranteed.

b **Correct Threshold Voltages:** In order to avoid that due to the spread in the internal thresholds (see the above limits) a wrong external voltage causes uncertain commutations for the two functions we suggest to use the following values:

Mute for Vcc>6.4V	:	VT = 2.3V
Mute for Vcc<6.4V	:	VT = Vcc/2 - 1
Stand-by	:	VT = 0.8V

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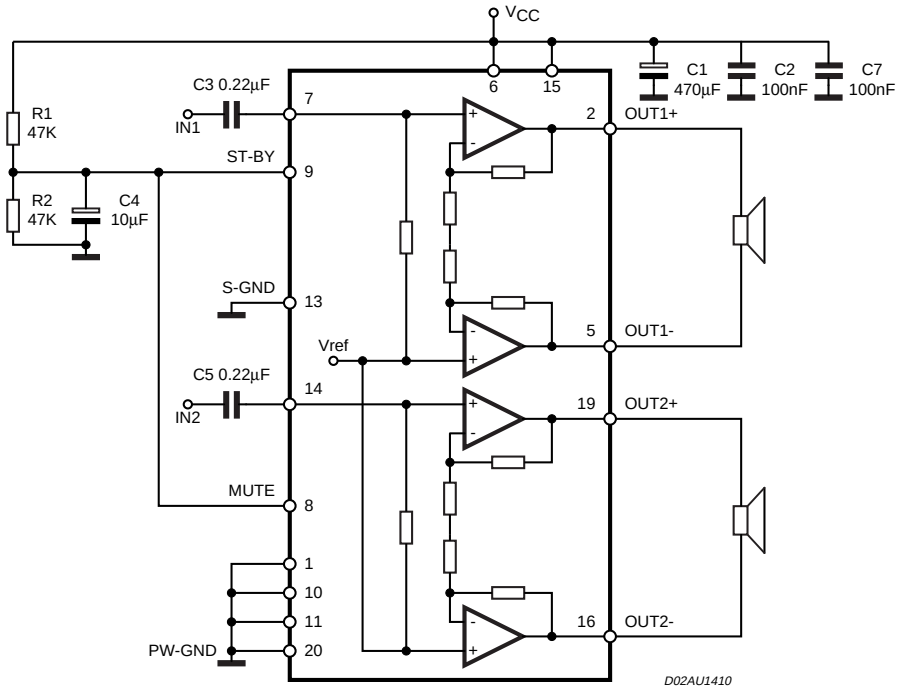
Figure 3. Stand-alone low-cost Application



PCB Layout and External Components:

Regarding the PCB layout care must be taken for three main subjects:

c) Signal and Power Gnd separation

d) Dissipating Copper Area

e) Filter Capacitors positioning

)Signal and Power Gnd separation:

c To the Signal GND must be referred the Audio Input Signals, the Mute and Stand-by Voltages and the device PIN.13. This Gnd path must be as clean as possible in order to improve the device THD+Noise and to avoid spurious oscillations across the speakers.
The Power GND is directly connected to the Output power Stage transistors (Emitters) and is crossed by large amount of current, this path is also used in this device to dissipate the heating generated (no needs of external heatsinker).
Referring to the typical application circuit, the separation between the two GND paths must be obtained connecting them separately (star routing) to the bulk
Electrolithic capacitor C1 (470µF).
Regarding the Power Gnd dimensioning we have to consider the Dissipated Power the Thermal Protection Threshold and the Package thermal Characteristics.

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d Dissipating Copper Area:

Dissipated Power:
The max dissipated power happens for a THD near 1% and is given by the formula:

$$P_{dmax(W)} = 2 \cdot \frac{V_{CC}^2}{\pi^2 \frac{Rl}{2}} + I_q V_{CC}$$

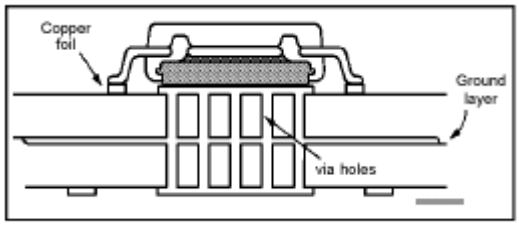
This gives for: Vcc = 9.5V, Rl = 8Ω ,Iq = 50mA a dissipated power of Pd = 5W.

Thermal Protection:

The thermal protection threshold is placed at a junction temperature of 150°C.

Package Thermal Characteristics:

The thermal resistance Junction to Ambient obtainable with a GND copper Area of 3x3 cm and with 16 via holes (see picture) is about 15°C/W. This means that with the above mentioned max dissipated Power (Pd=5W) we can expect a 75°C, this gives a safety margin before the thermal protection intervention in the consumer environments where a 50°C ambient is specified as maximum



The Thermal constraints determine the max supply voltage that can be used for the different Load Impedances, this in order to avoid the thermal Protection Intervention.

The max. dissipated power must be not in excess of 5W , this at turns gives the following operating supply voltages:

Load (Ohm)	Supply Voltage (V)
4	6.5
6	8.5
8	9.5
16	14

e Filter Capacitors Positioning:
The two Ceramic capacitors C2/C7 (100nF) must be placed as close as possible respectively to the two Vcc pins (6 - 15) in order to avoid the possibiltiy of oscillations arising on the output Audio signals.

Package Informations:

You can find a complete description for the PowerSO package into the APPLICATION NOTE AN668 available on web.

Here we want to focalize the attention only on the the Dissipating elements and ground layer.

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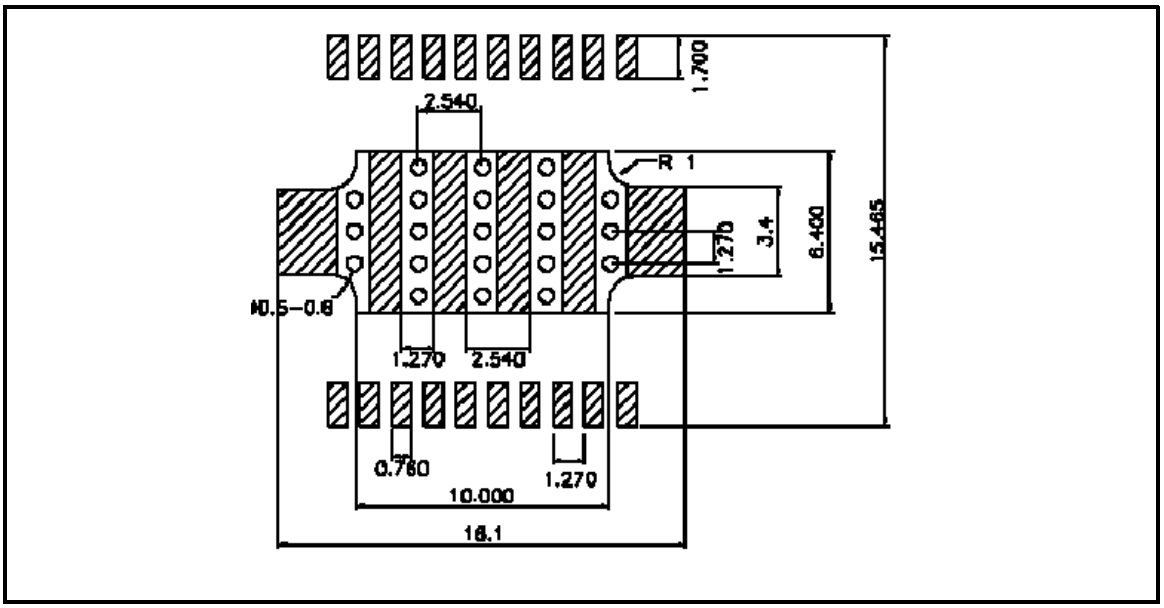
Considering the dissipated power involved in the TDA7266D application that is in the range of 5W, as explained in a previous section, we suggest via holes (see fig. 4).

Using via holes a more direct thermal path is obtained from the slug to the ground layer.The number of vias is chosen accordingly to the desired performance (in our demonstration board we use 15 vias).

In fig.4 is shown as an example the footprint to be used to create the vias.

Figure 4.



The above metioned mounting solution is enough to dissipate the power involved

In the most part of the application using the TDA7266D.

If necessary a further improvement in the Rth J-Ambient can be obtained as shown in fig.5 where the PowerSO20 is soldered onto a via hole structure with a metal plate glued on the opposite side of the board.

Figure 5. Mounting on epoxy FR4 using via Holes for heat transfer and external metal plate

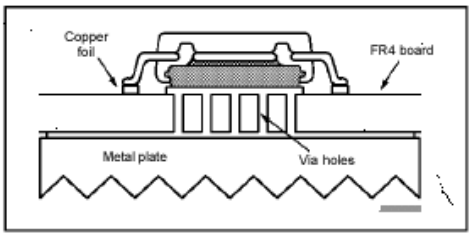


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Figure 6. Distortion vs Frequency

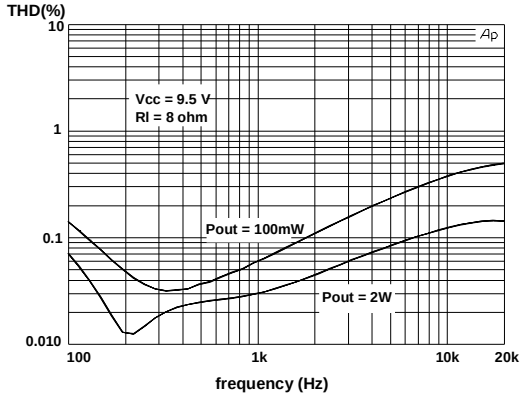

Figure 7. Gain vs Frequency

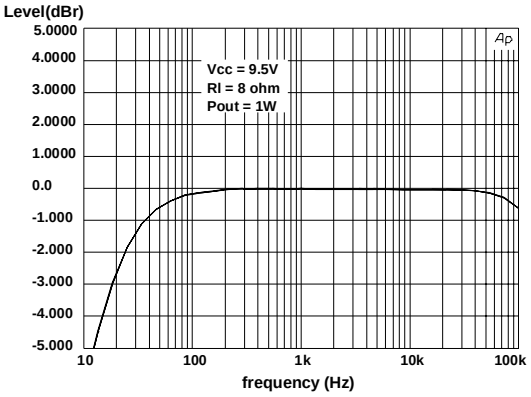

Figure 8. Mute Attenuation vs Vpin.8

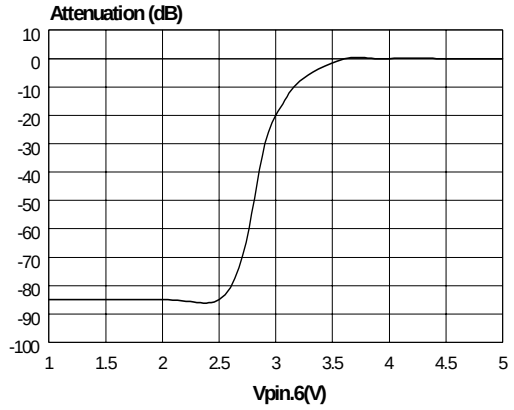

Figure 9. Stand-By attenuation vs Vpin 9

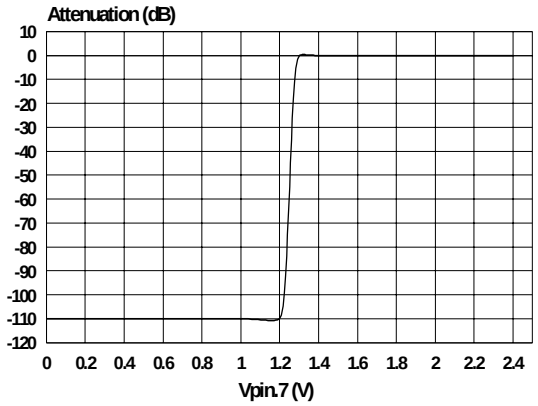

Figure 10. Quiescent Current vs Supply Voltage

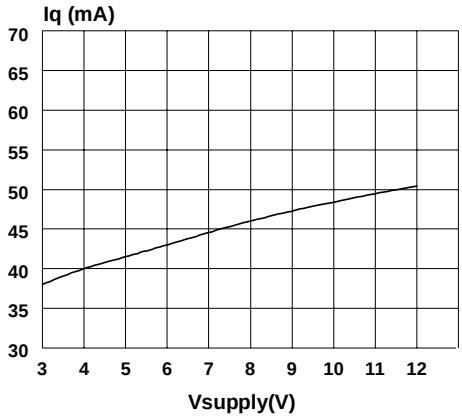

Figure 11. Total Power Dissipation & Efficiency vs Pout

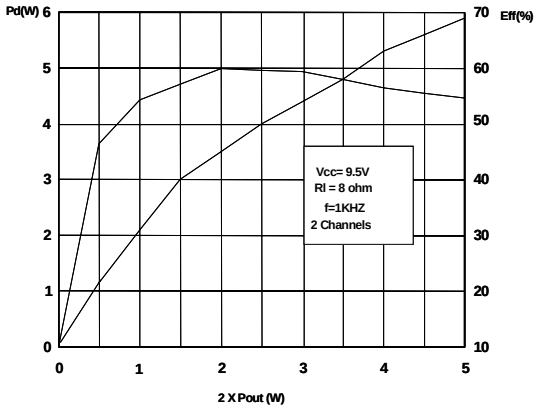

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Figure 12. THD+N vs Output Power

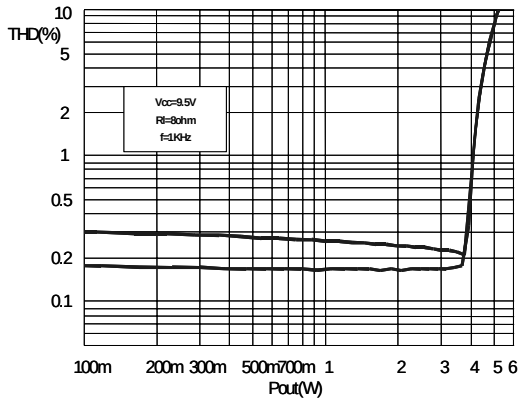

Figure 13. THD+N vs Output Power

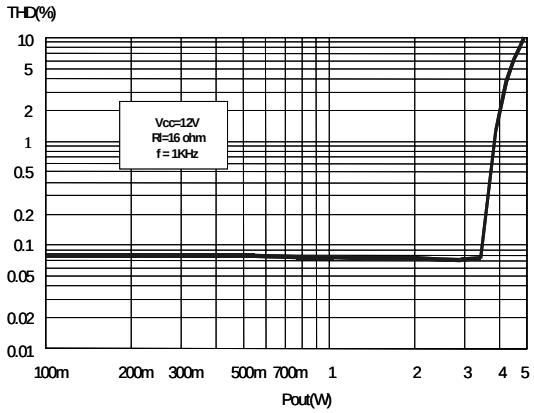

Figure 14. PC Board Component Layout

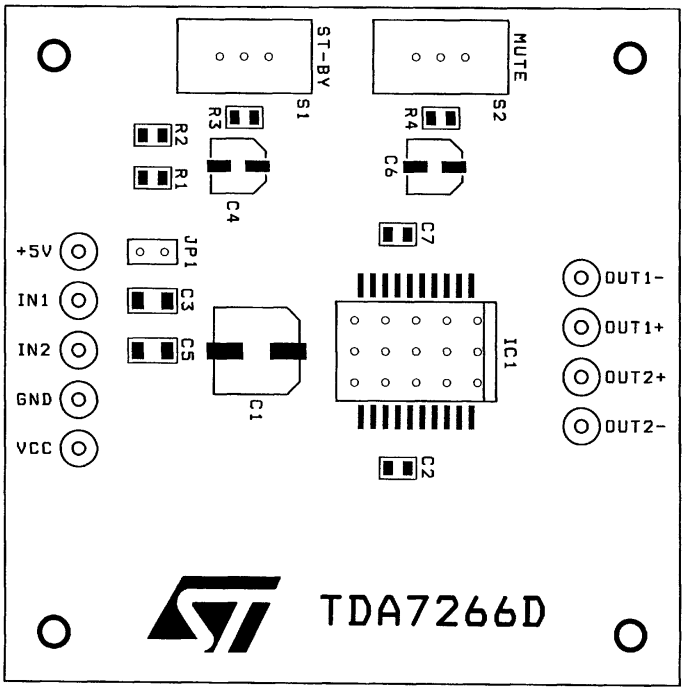

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Figure 15. Evaluation Board Top Layer Layout

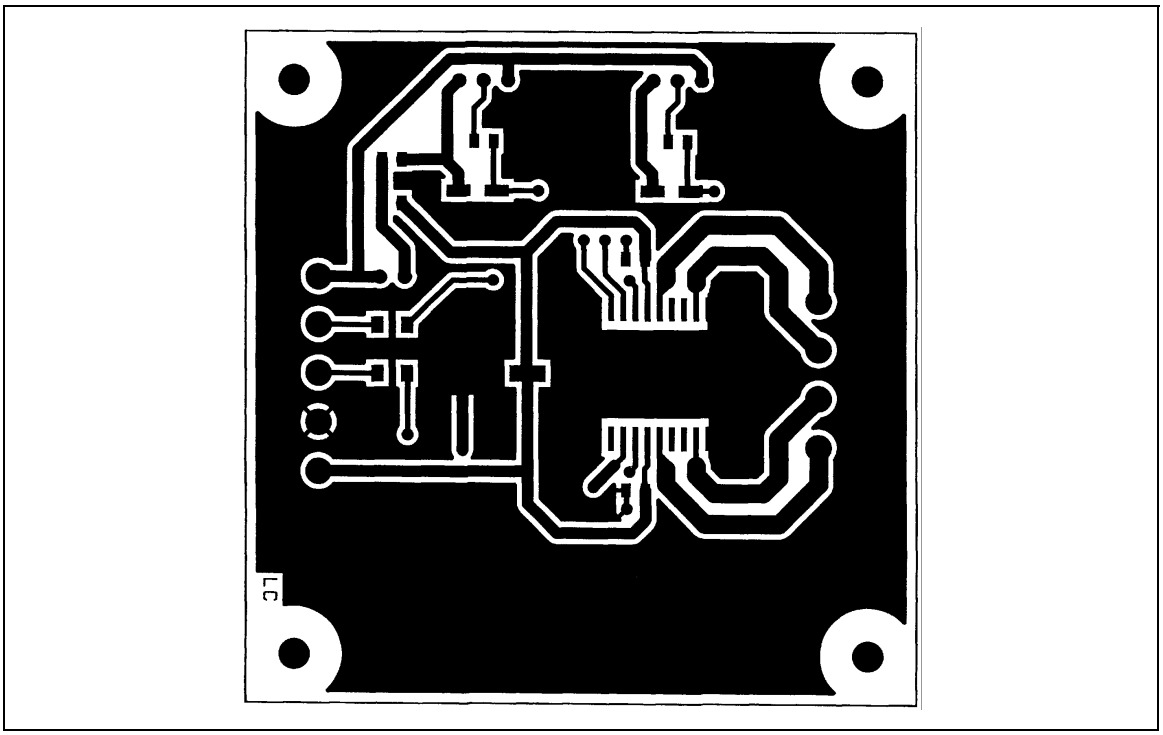
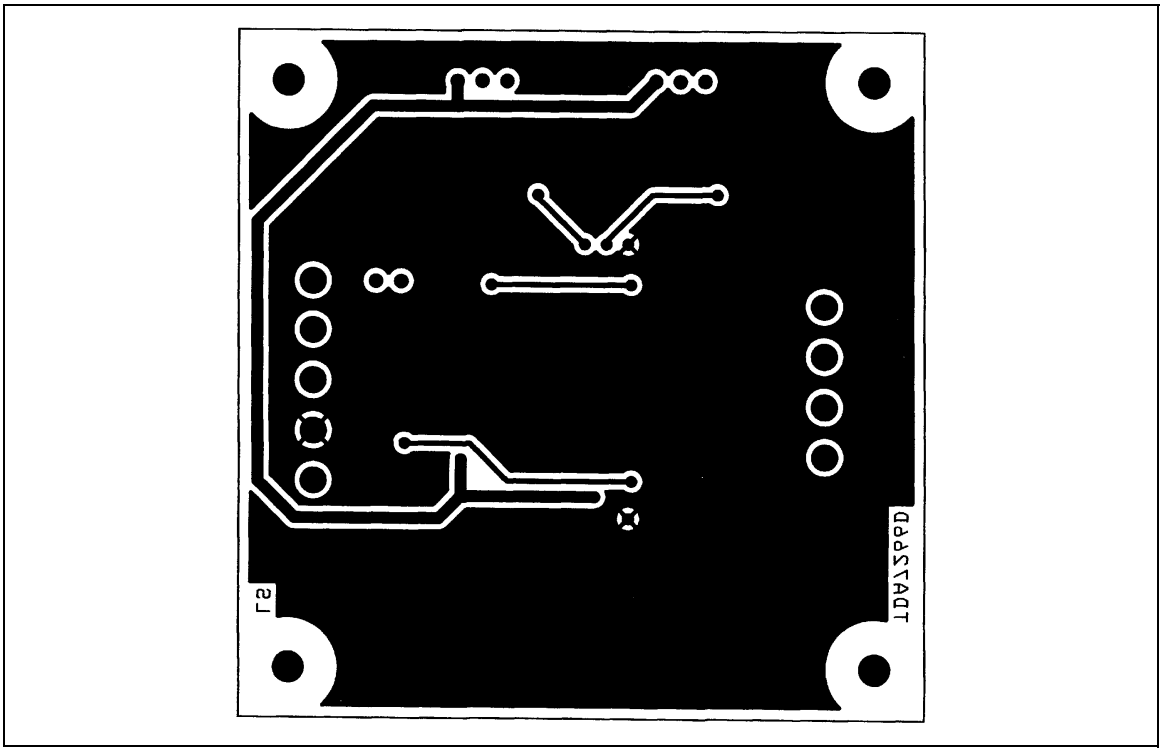


Figure 16. Evaluation Board Bottom Layer Layout



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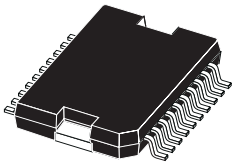
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8° (typ.)					
S	8° (max.)					
T		10			0.394	

(1) “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions: “E”, “G” and “a3”.

OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



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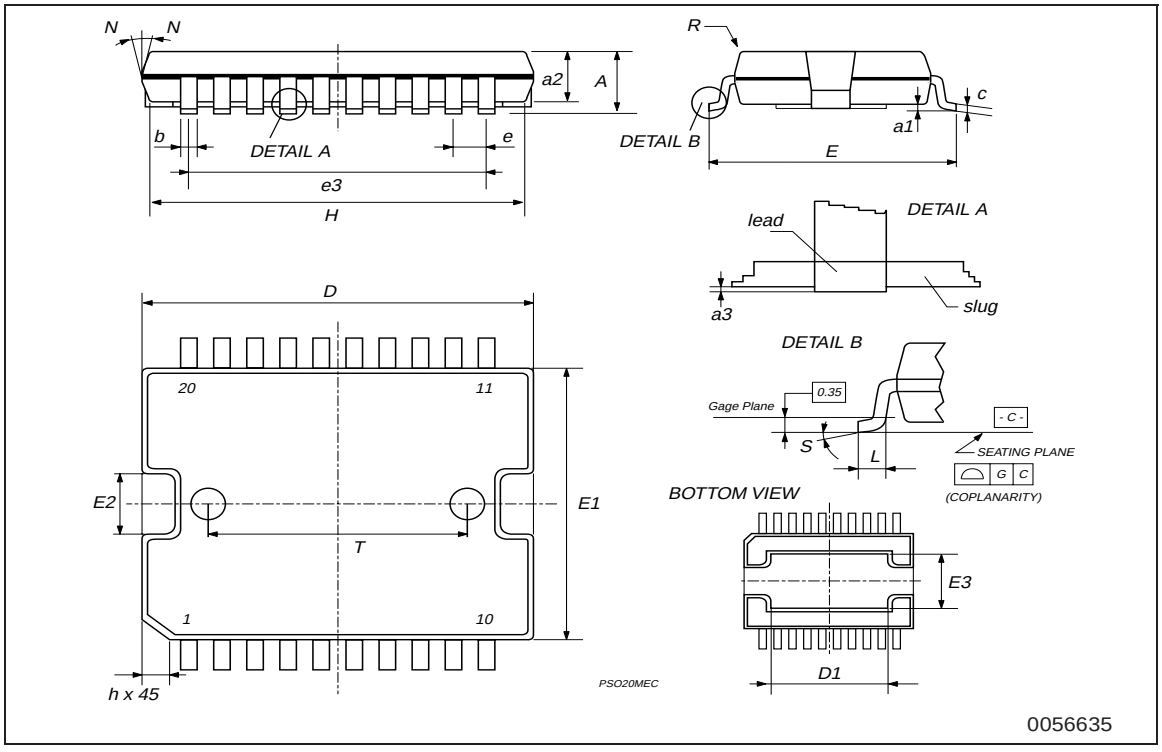
PowerSO20



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