

## 74F540 • 74F541 Octal Buffer/Line Driver with 3-STATE Outputs

### General Description

The 74F540 and 74F541 are similar in function to the 74F240 and 74F244 respectively, except that the inputs and outputs are on opposite sides of the package (see Connection Diagrams). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

### Features

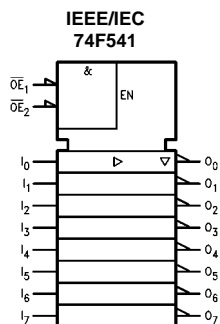
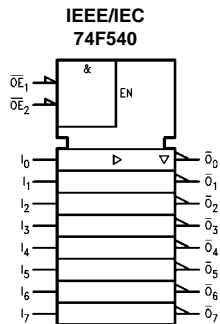
- 3-STATE outputs drive bus lines
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors

### Ordering Code:

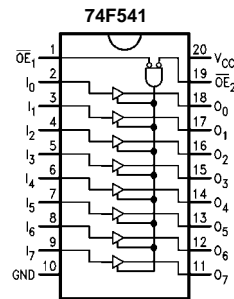
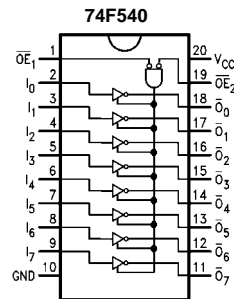
Order Number	Package Number	Package Description
74F540SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F540SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F540PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F541SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F541SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F541PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagrams



## Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$I_n$	Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$O_n, \overline{O}_n$	Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)

## Truth Table

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	I	74F540	74F541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.4 2.0 2.7		V	Min	I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -15 mA I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current (74F540)		11	20	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (74F540)		53	75	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current (74F540)		31	45	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current (74F541)		26	35	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (74F541)		55	75	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current (74F541)		31	55	mA	Max	V <sub>O</sub> = HIGH Z

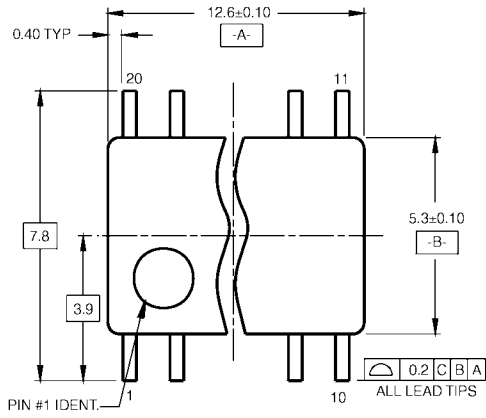
AC Electrical Characteristics									
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	1.5	3.0	5.0	1.0	6.0	1.0	5.5	ns
t <sub>PHL</sub>	Data to Output (74F540)	1.0	2.0	4.0	1.0	4.5	1.0	4.0	
t <sub>PZH</sub>	Output Enable Time (74F540)	2.5	4.9	8.0	2.5	9.0	2.5	8.5	ns
t <sub>PZL</sub>		3.5	5.8	10.0	3.5	11.0	3.5	10.5	
t <sub>PHZ</sub>	Output Disable Time (74F540)	1.5	3.4	6.0	1.5	7.0	1.5	6.5	
t <sub>PLZ</sub>		1.0	2.5	5.5	1.0	7.5	1.0	6.0	
t <sub>PLH</sub>	Propagation Delay	1.5	3.3	5.5			1.5	6.0	ns
t <sub>PHL</sub>	Data to Output (74F541)	1.5	2.7	5.5			1.5	6.0	
t <sub>PZH</sub>	Output Enable Time (74F541)	3.0	5.8	8.0			2.5	9.5	ns
t <sub>PZL</sub>		3.5	6.1	8.5			3.0	9.5	
t <sub>PHZ</sub>	Output Disable Time (74F541)	1.5	3.4	6.0			1.5	6.5	
t <sub>PLZ</sub>		1.5	2.9	5.5			1.5	6.0	

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B**

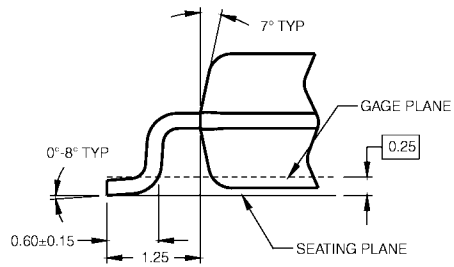
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

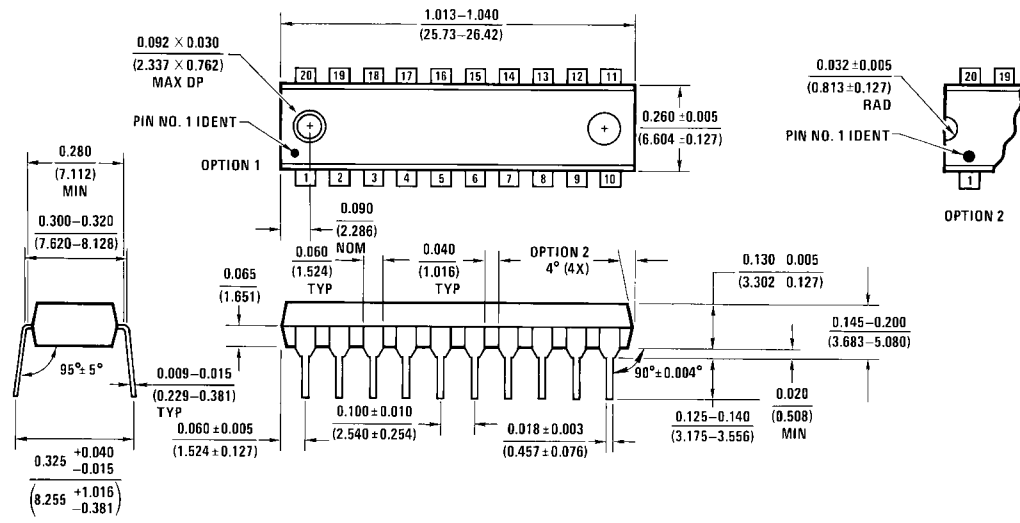
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

N20A (REV G)

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