

# 74LCX07

## Low Voltage Hex Buffer with Open Drain Outputs

### Features

- 5V tolerant inputs
- 2.3V to 5.5V  $V_{CC}$  specifications provided
- 2.9ns  $t_{PD}$  max. ( $V_{CC} = 3.3V$ ), 10 $\mu$ A  $I_{CC}$  max.
- Power down high impedance inputs and outputs
- +24mA output drive ( $V_{CC} = 3.0V$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Leadless DQFN package

### General Description

The LCX07 contains six buffers. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The outputs of the LCX07 are open drain and can be connected to other open drain outputs to implement active HIGH wire AND or active LOW wire OR functions.

The 74LCX07 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.


### Ordering Information

Order Number	Package Number	Package Description
74LCX07M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX07SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX07BQX <sup>(1)</sup>	MLP14A	14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
74LCX07MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

#### Note:

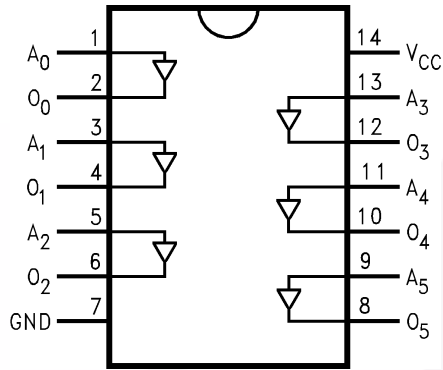
1. DQFN package available in Tape and Reel only.

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

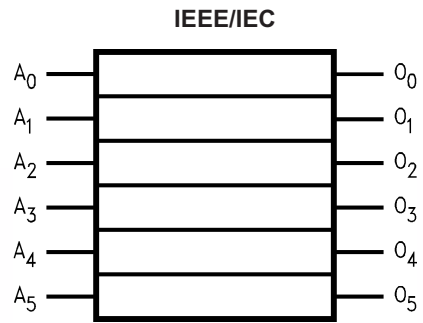
 All packages are lead free per JEDEC: J-STD-020B standard.

### Connection Diagram

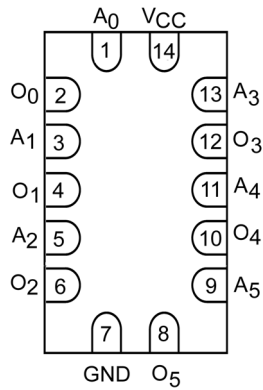
Pin Assignments for SOIC, SOP, and TSSOP



### Logic Symbol



Pad Assignments for DQFN



(Top Through View)

### Pin Description

Pin Names	Description
$A_n$	Inputs
$O_n$	Outputs



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$V_I$	DC Input Voltage	-0.5V to +7.0V
$V_O$	DC Output Voltage, Output in HIGH or LOW State <sup>(2)</sup>	-0.5V to +7.0V
$I_{IK}$	DC Input Diode Current, $V_I < GND$	-50mA
$I_{OK}$	DC Output Diode Current $V_O < GND$	-50mA
	$V_O > V_{CC}$	+50mA
$I_O$	DC Output Current	$\pm 50$ mA
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$ mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$ mA
$T_{STG}$	Storage Temperature	-65°C to +150°C

**Note:**

2.  $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions<sup>(3)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Supply Voltage Operating	2.0	5.5	V
	Data Retention	1.5	5.5	
$V_I$	Input Voltage	0	5.5	V
$V_O$	Output Voltage	0	5.5	V
$I_{OL}$	Output Current $V_{CC} = 4.5V-5.5V$		+32	mA
	$V_{CC} = 3.0V-3.6V$		+24	
	$V_{CC} = 2.7V-3.0V$		+12	
	$V_{CC} = 2.3V-2.7V$		+8	
$T_A$	Free-Air Operating Temperature	-40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V

**Note:**

3. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Max.	
V <sub>IH</sub>	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6		2.0		
		4.5–5.5		0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	LOW Level Input Voltage	2.3–2.7			0.7	V
		2.7–3.6			0.8	
		4.5–5.5			0.3 × V <sub>CC</sub>	
V <sub>OL</sub>	LOW Level Output Voltage	2.3–5.5	I <sub>OL</sub> = 100μA		0.2	V
		2.3	I <sub>OL</sub> = 8mA		0.6	
		2.7	I <sub>OL</sub> = 12mA		0.4	
		3.0	I <sub>OL</sub> = 16mA		0.4	
		3.0	I <sub>OL</sub> = 24mA		0.55	
		4.5	I <sub>OL</sub> = 32mA		0.55	
I <sub>I</sub>	Input Leakage Current	2.3–5.5	0 ≤ V <sub>I</sub> ≤ 5.5V		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	0	V <sub>I</sub> or V <sub>O</sub> = 5.5V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.3–5.5	V <sub>I</sub> = V <sub>CC</sub> or GND		10	μA
		2.3–5.5	3.6V ≤ V <sub>I</sub> ≤ 5.5V		±10	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3–3.6	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500	μA
		4.5–5.5				
I <sub>OHZ</sub>	Off State Current	2–5.5	V <sub>O</sub> = 5.5V		10	μA

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω								Units
		V <sub>CC</sub> = 5.0V ± 0.5V, C <sub>L</sub> = 50pF		V <sub>CC</sub> = 3.3V ± 0.3V, C <sub>L</sub> = 50pF		V <sub>CC</sub> = 2.7V, C <sub>L</sub> = 50pF		V <sub>CC</sub> = 2.5V ± 0.2V, C <sub>L</sub> = 30pF		
		Min.	Max.	Min.	Max.	Min	Max	Min	Max	
t <sub>PZL</sub> , t <sub>PLZ</sub>	Propagation Delay Time	0.5	3.0	0.8	3.7	1.0	4.4	0.8	3.8	ns

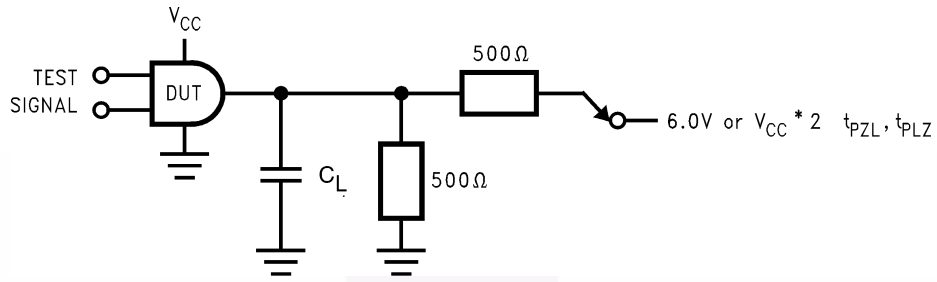
**Dynamic Switching Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C	
				Typical	Unit
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	0.9	V
		2.5	C <sub>L</sub> = 30pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	0.7	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	-0.8	V
		2.5	C <sub>L</sub> = 30pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	-0.6	

**Capacitance**

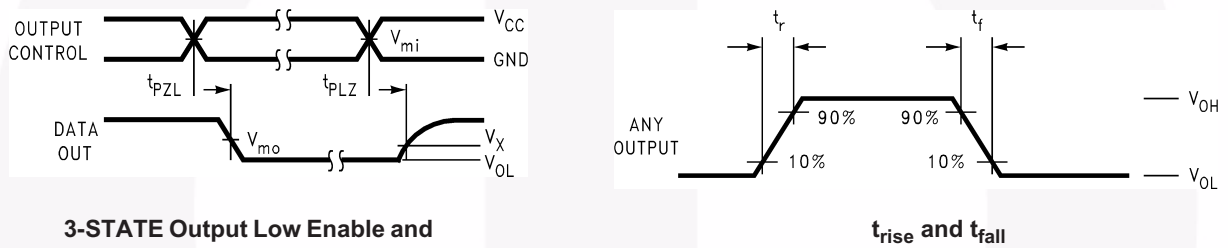
Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10MHz	25	pF

### AC Loading and Waveforms



Test	Switch
$t_{PZL}, t_{PLZ}$	$V_{CC} \times 2$ at $V_{CC} = 5.0 \pm 0.5V$
	6V at $V_{CC} = 3.3 \pm 0.3V$
	$V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$

Figure 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)



#### 3-STATE Output Low Enable and Disable Times for Logic

Symbol	$V_{CC}$			
	$5.0V \pm 0.5V$	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
$V_{mi}$	$V_{CC} / 2$	1.5V	1.5V	$V_{CC} / 2$
$V_{mo}$	$V_{CC} / 2$	1.5V	1.5V	$V_{CC} / 2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

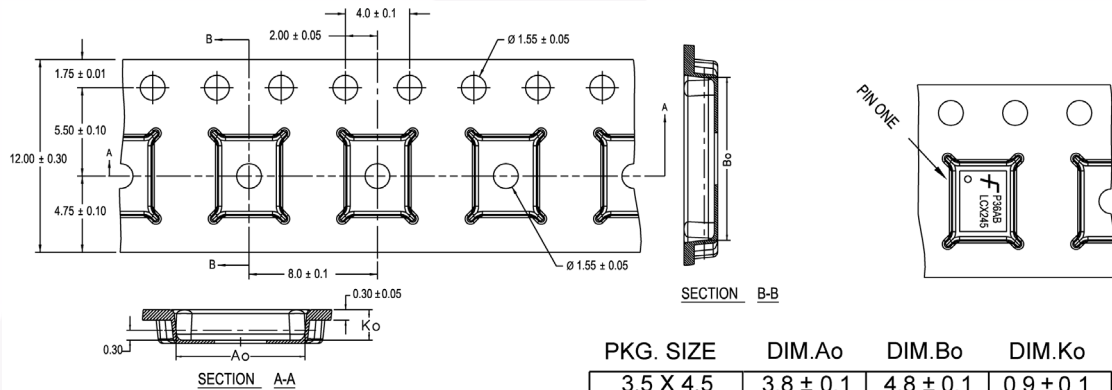
Figure 2. Waveforms (Input Pulse Characteristics;  $f = 1MHz, t_r = t_f = 3ns$ )

## Tape and Reel Specification

### Tape Format for DQFN

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (Typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typ.)	Empty	Sealed

### Tape Dimensions inches (millimeters)



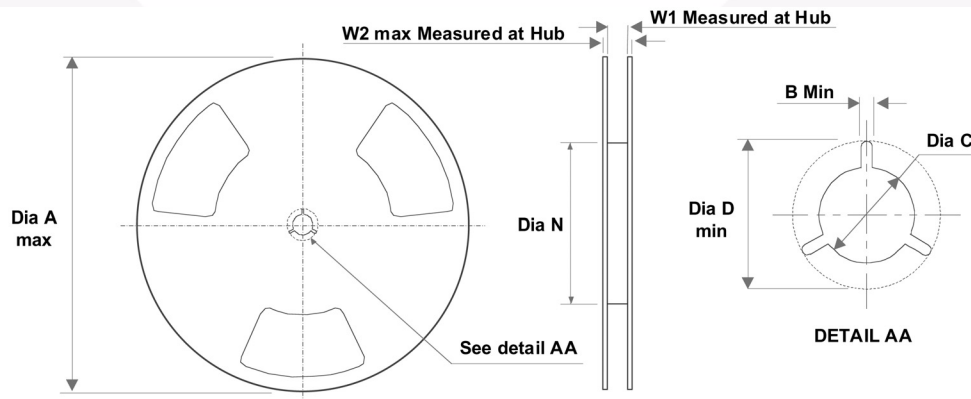
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

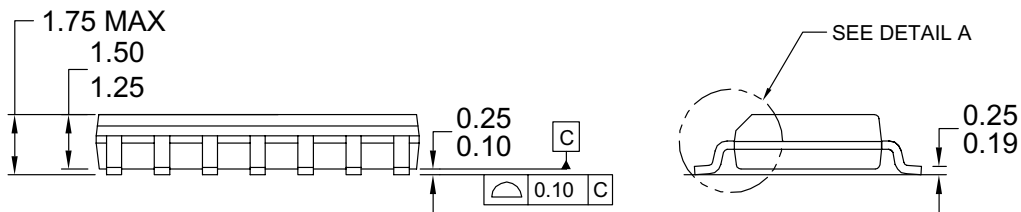
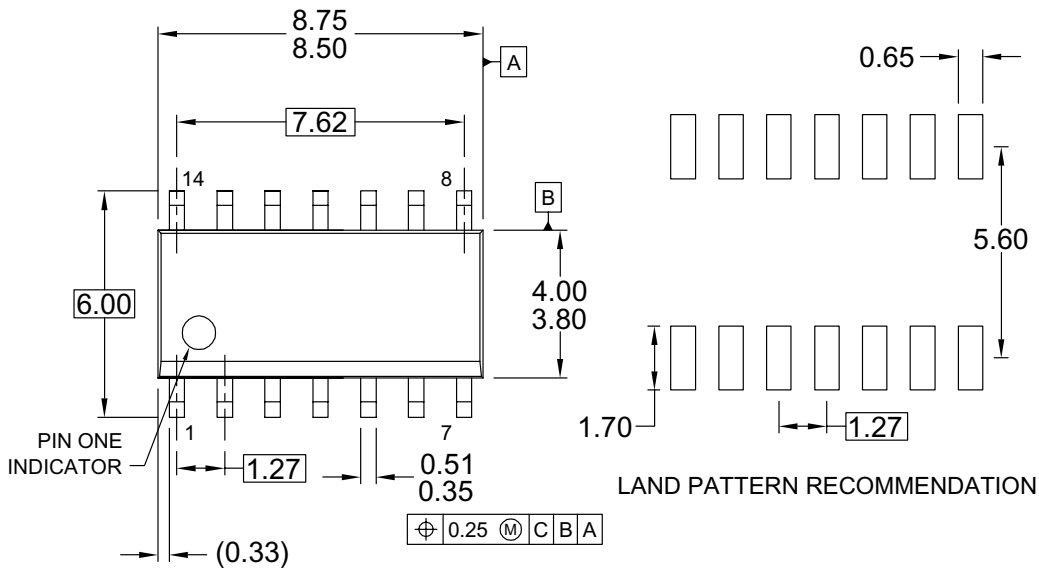
1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is  $\pm 0.002[0.05]$  for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

### Reel Dimensions inches (millimeters)



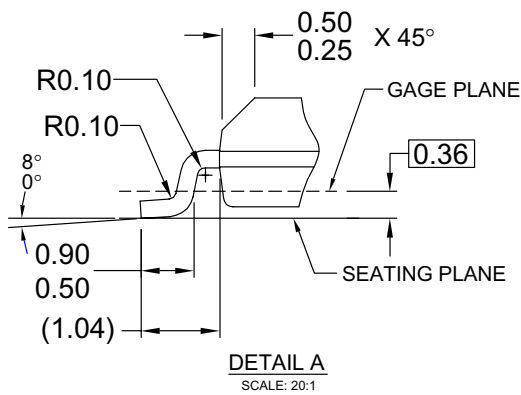
Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)

### Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13



**Figure 3. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**

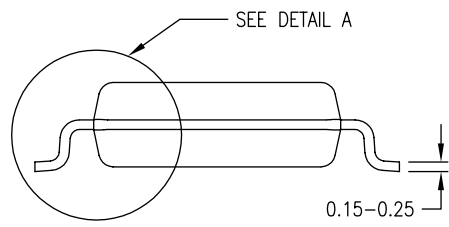
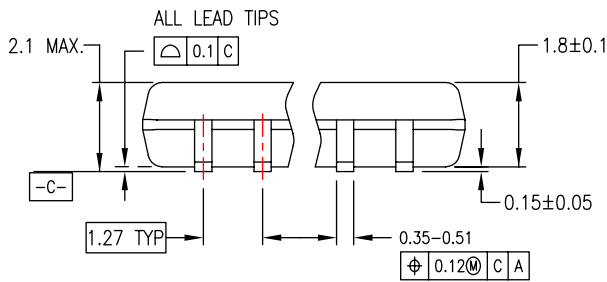
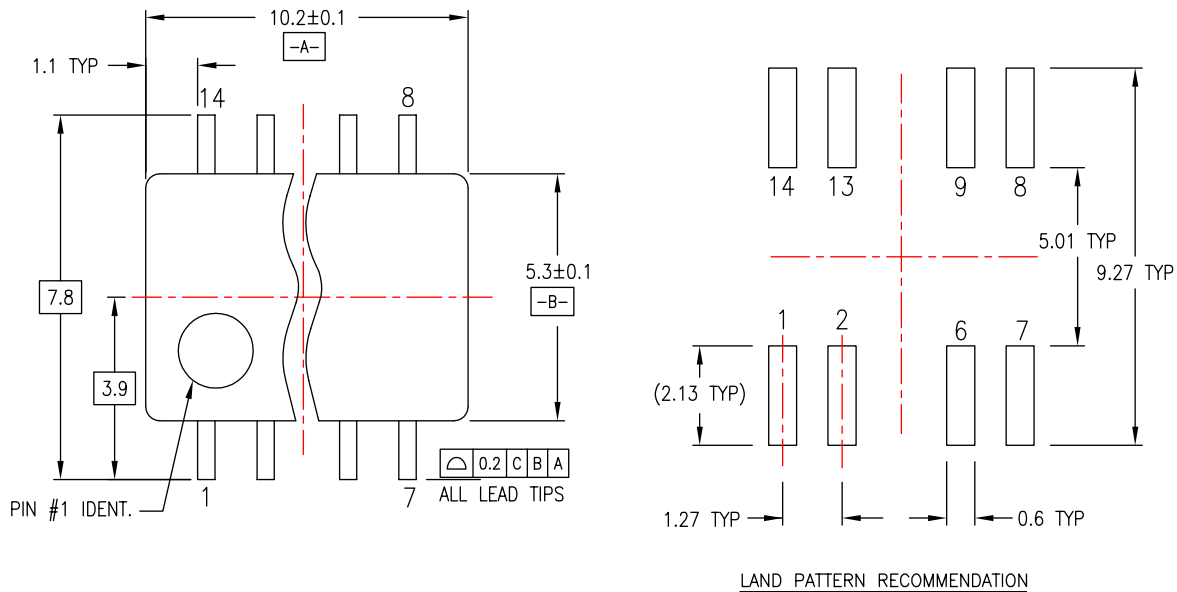
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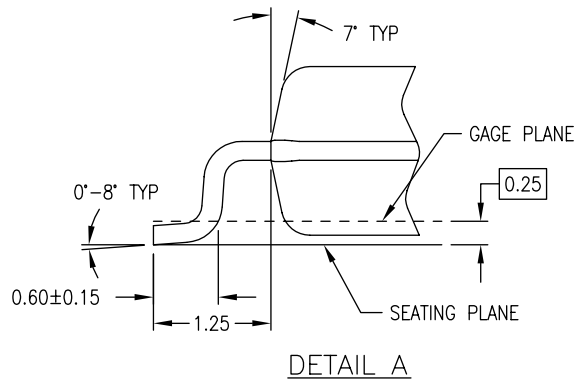
**Physical Dimensions (Continued)**



DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



M14DREVC

**Figure 4. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

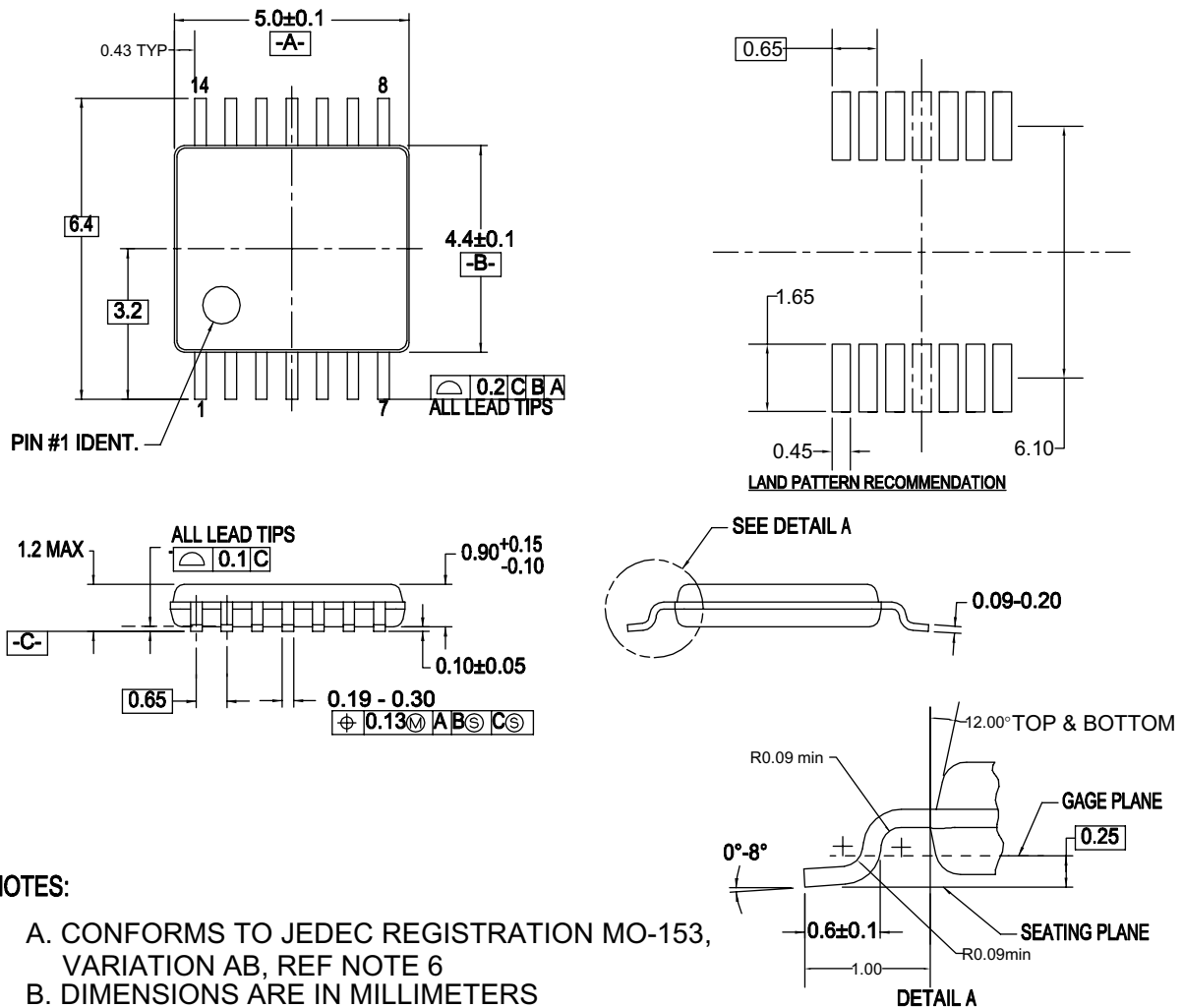
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Physical Dimensions (Continued)



NOTES:

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- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 6. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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
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| FastvCore <sup>™</sup>  | OPTOLOGIC <sup>®</sup>                       | SuperSOT <sup>™</sup> 3                | UHC <sup>®</sup>                 |
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|   |  | SuperSOT <sup>™</sup> 8                | UniFET <sup>™</sup>              |
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