19-3624; Rev 0; 3/05

EVALUATION KIT AVAILABLE

EEPROM-Programmable TFT VCOM Calibrator with I²C Interface

General Description

The MAX8738 is an I²C-programmable VCOM-adjustment solution for thin-film transistor (TFT) liquid-crystal displays (LCDs). The MAX8738 simplifies the labor-intensive VCOM-adjustment process and replaces mechanical potentiometers, which significantly reduces labor costs, increases reliability, and enables automation.

The MAX8738 attaches to an external resistive voltage-divider and sinks a programmable current to set the VCOM voltage level. An internal 7-bit digital-to-analog converter (DAC) controls the sink current. The DAC is ratiometric relative to AVDD and is guaranteed to be monotonic over all operating conditions. This VCOM calibrator IC includes an EEPROM to store the desired VCOM voltage level. The EEPROM can be programmed repeatedly, giving TFT LCD manufacturers the flexibility to calibrate the display panel as many times as the manufacturing process requires.

The MAX8738 features a 2-wire I²C interface for DAC-adjustment commands and EEPROM programming. The interface utilizes the existing I²C bus on the LCD panel connector so no additional panel connector pins are required. The MAX1512 is a similar product with a 1-wire interface and is recommended for applications with no existing I²C interface.

The MAX8738 is available in an 8-pin µMAX® package. A complete evaluation kit is available to simplify evaluation and production development.

Applications

LCD Panels

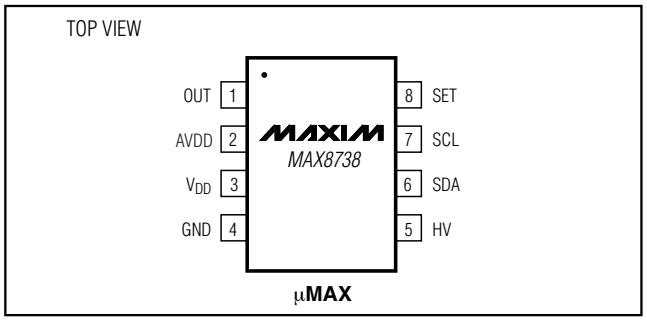
Notebook Computers

Display Products

LCD TVs

µMAX is a registered trademark of Maxim Integrated Products, Inc.

Pin Configuration



Features

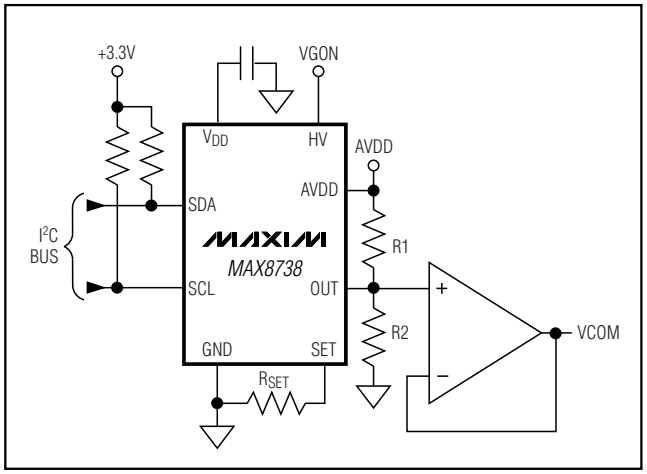
- ♦ 7-Bit Adjustable Sink-Current Output
- ♦ Resistor-Adjustable, Full-Scale Range
- ♦ Guaranteed Monotonic Output Over Operating Range
- ♦ 2-Wire I²C Interface
- ♦ EEPROM Stores VCOM Setting
- ♦ 4.5V to 20V Analog Supply Voltage Range (V_{AVDD})
- ♦ 60µA (max) AVDD Supply Current
- ♦ 16.1V to 28V EEPROM Programming Supply Voltage Range (V_{HV})
- ♦ <1µA HV Supply Current (Not in Program Mode)
- ♦ 8-Pin µMAX

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8738EUA	-40°C to +85°C	8 µMAX
MAX8738EUA+	-40°C to +85°C	8 µMAX

+Denotes lead-free package.

Typical Operating Circuit



EEPROM-Programmable TFT VCOM Calibrator with I²C Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD}, SET, SCL, SDA to GND .....-0.3V to +6V
OUT to GND .....-0.3V to +18V
AVDD, HV to GND .....-0.3V to +30V
Continuous Power Dissipation
8-Pin µMAX (derate 4.5mW/ °C above +70°C) 362mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 15V, V_{HV} = 20V, V_{OUT} = 6.75V, R_{SET} = 30.1kΩ, **T_A = 0°C to +85°C**, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINK CURRENT ADJUSTMENT						
SET Voltage Resolution			7			Bits
SET Differential Nonlinearity		Monotonic overtemperature	-1		+1	LSB
SET Zero-Scale Error			-1	+1	+2	LSB
SET Full-Scale Error			-4		+4	LSB
SET Current	I_{SET}				120	µA
SET External Resistance (Note 1)	R_{SET}	To GND, V_{AVDD} = 20V	10		200	kΩ
		To GND, V_{AVDD} = 4.5V	2.25		45.00	
V_{SET}/V_{AVDD} Voltage Ratio		DAC full scale		0.05		V/V
		Factory set	0.024	0.025	0.026	
2-WIRE INTERFACE						
Logic-Input Low Voltage	V_{IL}	SDA, SCL			0.8	V
Logic-Input High Voltage	V_{IH}	SDA, SCL	2.1			V
Logic-Output Low Sink Current		SDA forced to 0.4V	6			mA
Logic-Input Current		V_{SDA} = +3.3V or GND, V_{SCL} = +3.3V or GND	-1		+1	µA
SDA and SCL Input Capacitance		SDA, SCL		5		pF
SCL Frequency	f_{CLK}		DC		100	kHz
SCL High Time	t_{CLH}		4000			ns
SCL Low Time	t_{CLL}		4700			ns
SDA and SCL Rise Time	t_R	(Note 2)			1000	ns
SDA and SCL Fall Time	t_F	(Note 2)			300	ns
START Condition Hold Time	t_{HDSTT}	10% of SDA to 90% of SCL	4000			ns
START Condition Setup Time	t_{SUSTT}		4700			ns
Data Input Hold Time	t_{HDDAT}		0			ns
Data Input Setup Time	t_{SUDAT}		250			ns
STOP Condition Setup Time	t_{SUSTP}		4000			ns
Bus Free Time	t_{BF}		4700			ns
Input Filter Spike Suppression	t_{SP}	SDA, SCL (Note 2)		1		µs
V_{DD} REGULATOR						
V_{DD} Output Voltage	V_{DD}	4.5V < V_{AVDD} < 20V, I_{VDD} = 0	3.1	3.6	4.5	V
V_{DD} Power-On Reset Threshold		Rising edge, 100mV hysteresis			3.0	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 15V, V_{HV} = 20V, V_{OUT} = 6.75V, R_{SET} = 30.1kΩ, **T_A = 0°C to +85°C**, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AVDD SUPPLY						
AVDD Supply Range	V_{AVDD}		4.5		20.0	V
AVDD Operating Current	I_{AVDD}	V_{AVDD} = 20V		25	60	µA
HV SUPPLY						
HV Input Voltage Range	V_{HV}		16.1		28.0	V
HV Power-On Reset Threshold		Rising edge, 60mV hysteresis		15.6	16.0	V
HV Input Bias Current	I_{HV}	Not in program mode (Note 3)		0.1	1	µA
		Program mode (Note 3)		15	30	
		During program (Note 4)			60	
OUTPUT VOLTAGE						
OUT Leakage Current				±100		nA
OUT Settling Time		To ±0.5 LSB error band		20		µs
OUT Voltage Range	V_{OUT}		V_{SET} + 0.5V		13	V

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 15V, V_{HV} = 20V, V_{OUT} = 6.75V, R_{SET} = 30.1kΩ, **T_A = -40°C to +85°C**, unless otherwise noted.) (Figure 1) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINK CURRENT ADJUSTMENT						
SET Differential Nonlinearity		Monotonic overtemperature	-1		+1	LSB
SET Zero-Scale Error			-1		+2	LSB
SET Full-Scale Error			-4		+4	LSB
SET Current	I_{SET}				120	µA
SET External Resistance (Note 1)	R_{SET}	To GND, V_{AVDD} = 20V	10		200	kΩ
		To GND, V_{AVDD} = 4.5V	2.25		45.00	
2-WIRE INTERFACE						
Logic-Input Low Voltage	V_{IL}	SDA, SCL			0.8	V
Logic-Input High Voltage	V_{IH}	SDA, SCL	2.1			V
Logic-Output Low Sink Current		SDA forced to 0.4V	6			mA
Logic-Input Current	I_{LI}	V_{SDA} = +3.3V or GND, V_{SCL} = +3.3V or GND	-1		+1	µA
SCL Frequency	f_{CLK}		DC		100	kHz
SCL High Time	t_{CLH}		4000			ns
SCL Low Time	t_{CLL}		4700			ns
SDA and SCL Rise Time	t_R	(Note 2)			1000	ns
SDA and SCL Fall Time	t_F	(Note 2)			300	ns

EEPROM-Programmable TFT VCOM Calibrator with I²C Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 15V, V_{HV} = 20V, V_{OUT} = 6.75V, R_{SET} = 30.1kΩ, **T_A = -40°C to +85°C**, unless otherwise noted.) (Figure 1) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
START Condition Hold Time	t_{HDSTT}	10% of SDA to 90% of SCL	4000			ns
START Condition Setup Time	t_{SUSTT}		4700			ns
Data Input Hold Time	t_{HDDAT}		0			ns
Data Input Setup Time	t_{SUDAT}		250			ns
STOP Condition Setup Time	t_{SUSTP}		4000			ns
Bus Free Time	t_{BF}		4700			ns
V_{DD} REGULATOR						
V_{DD} Output Voltage	V_{DD}	4.5V < V_{AVDD} < 20V, I_{VDD} = 0	3.1		4.5	V
V_{DD} Power-On Reset Threshold		Rising edge, 100mV hysteresis			3.0	V
AVDD SUPPLY						
AVDD Supply Range	V_{AVDD}		4.5		20.0	V
AVDD Operating Current	I_{AVDD}	V_{AVDD} = 20V			60	µA
HV SUPPLY						
HV Input Voltage Range	V_{HV}		16.1		28.0	V
HV Power-On Reset Threshold		Rising edge, 60mV hysteresis			16.0	V
HV Input Bias Current	I_{HV}	Not in program mode (Note 3)			1	µA
		Program mode (Note 3)			30	
		During program (Note 4)			60	
OUTPUT VOLTAGE						
OUT Voltage Range	V_{OUT}		V_{SET} + 0.5V		13	V

Note 1: SET resistors are only checked at full scale.
Note 2: Guaranteed by design. Not production tested.
Note 3: The MAX8738 enters program mode after any valid command is received, except the AAh command.
Note 4: Program time lasts for 11ms.
Note 5: Specifications from 0°C to -40°C are guaranteed by design, not production tested.

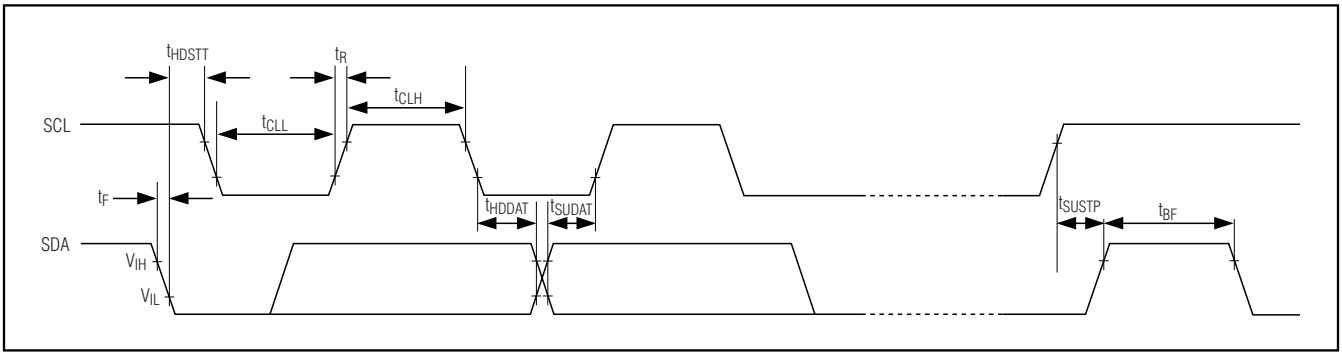
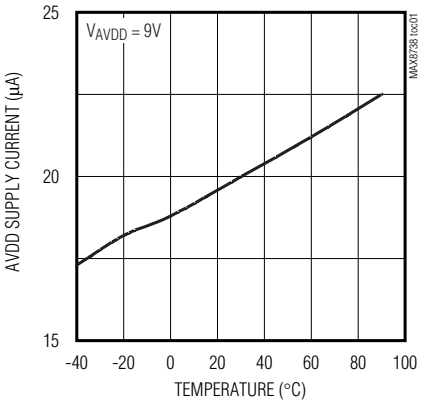


Figure 1. Timing Definitions Used in the Electrical Characteristics

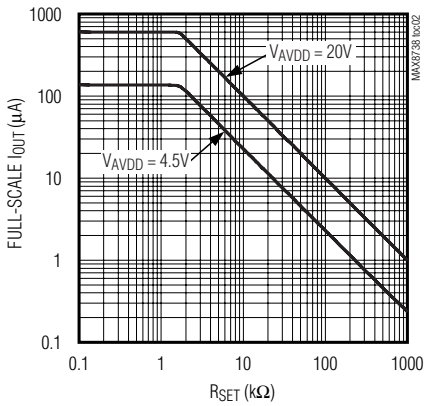
Typical Operating Characteristics

(V_{AVDD} = 9V, V_{HV} = 18V, R_{SET} = 24.9kΩ, T_A = +25°C, unless otherwise noted.)

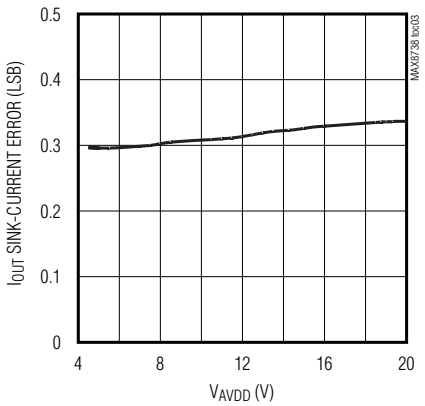
AVDD SUPPLY CURRENT vs. TEMPERATURE



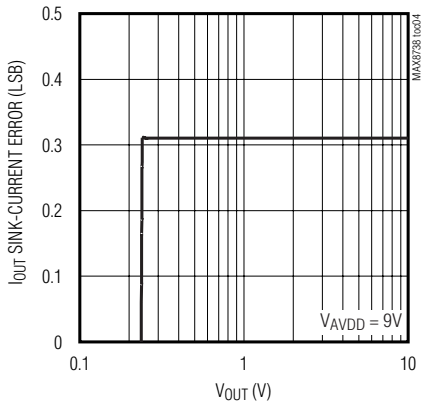
FULL-SCALE I_{OUT} vs. R_{SET}



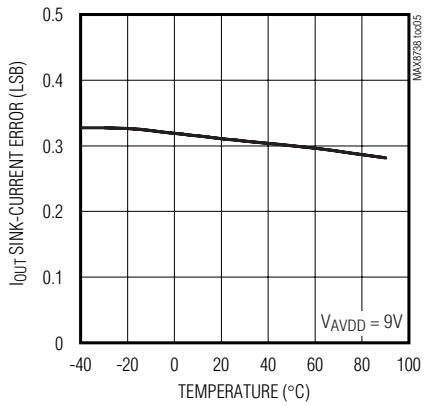
I_{OUT} SINK-CURRENT ERROR vs. V_{AVDD}



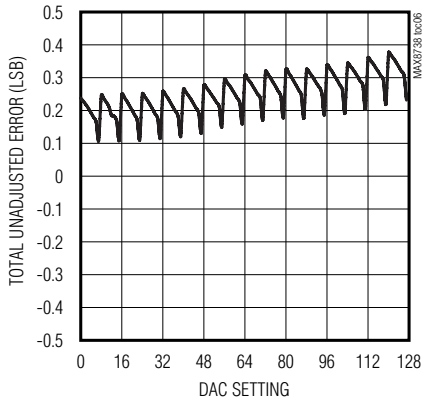
I_{OUT} SINK-CURRENT ERROR vs. V_{OUT}



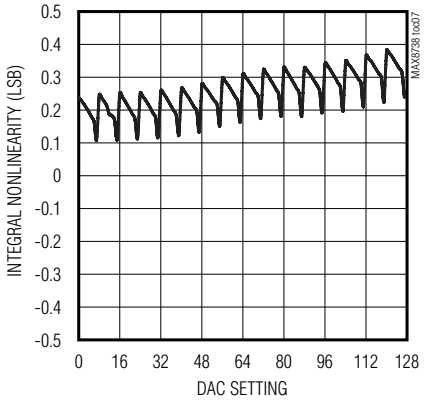
I_{OUT} SINK-CURRENT ERROR vs. TEMPERATURE



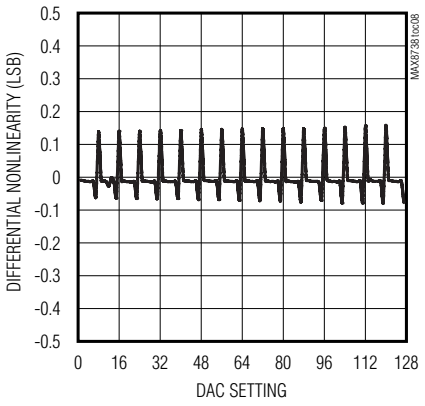
TOTAL UNADJUSTED ERROR vs. DAC SETTING



INTEGRAL NONLINEARITY vs. DAC SETTING



DIFFERENTIAL NONLINEARITY vs. DAC SETTING

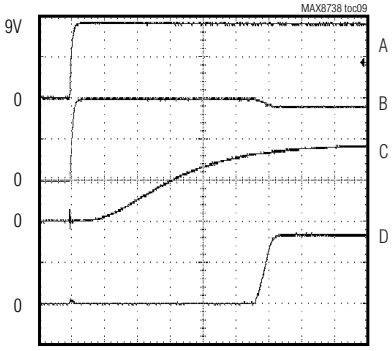


EEPROM-Programmable TFT VCOM Calibrator with I²C Interface

Typical Operating Characteristics (continued)

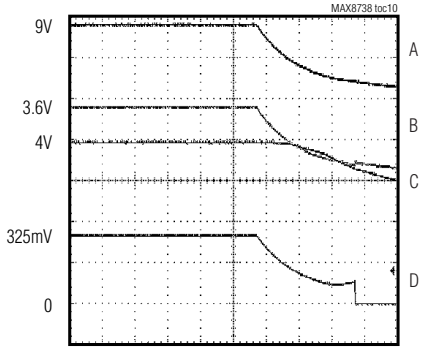
(V_{AVDD} = 9V, V_{HV} = 18V, R_{SET} = 24.9kΩ, T_A = +25°C, unless otherwise noted.)

AVDD POWER-UP RESPONSE



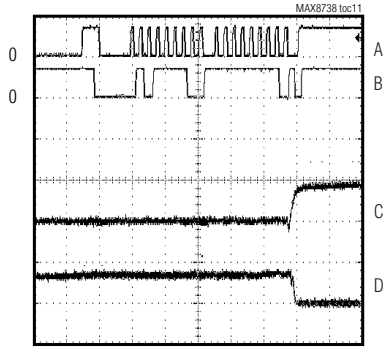
A. V_{AVDD}, 5V/div
B. V_{OUT}, 2V/div
C. V_{DD}, 2V/div
D. V_{SET}, 0.2V/div

AVDD POWER-DOWN RESPONSE



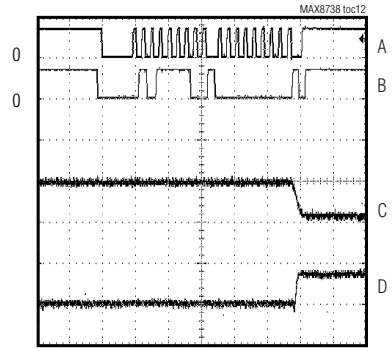
A. V_{AVDD}, 5V/div
B. V_{OUT}, 2V/div
C. V_{DD}, 2V/div
D. V_{SET}, 0.2V/div

SINGLE LSB STEP-UP RESPONSE



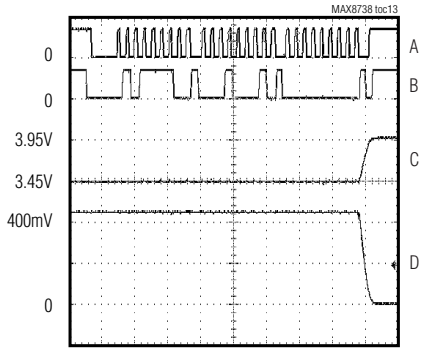
A. SCL, 5V/div
B. SDA, 5V/div
C. V_{SET}, 5mV/div
D. V_{OUT}, 5mV/div

SINGLE LSB STEP-DOWN RESPONSE



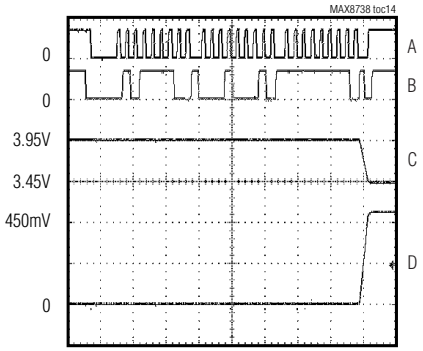
A. SCL, 5V/div
B. SDA, 5V/div
C. V_{SET}, 5mV/div
D. V_{OUT}, 5mV/div

WRITE 00H RESPONSE



A. SCL, 5V/div
B. SDA, 5V/div
C. V_{OUT}, 500mV/div
D. V_{SET}, 200mV/div

WRITE FFH RESPONSE



A. SCL, 5V/div
B. SDA, 5V/div
C. V_{OUT}, 500mV/div
D. V_{SET}, 200mV/div

Pin Description

PIN	NAME	FUNCTION
1	OUT	Adjustable Sink-Current Output. OUT connects to the resistive voltage-divider between AVDD and GND that sets the VCOM voltage. I_{OUT} lowers the divider voltage by an adjustable amount. See the SET pin description.
2	AVDD	High-Voltage Analog Supply. Bypass to GND with a 0.1µF capacitor.
3	V_{DD}	3.6V Regulator Output. V_{DD} provides the supply voltage to the entire IC. V_{DD} is not for external use. Bypass to GND with a 0.1µF capacitor.
4	GND	Ground. Connect to system ground.
5	HV	EEPROM High-Voltage Programming Supply. Bypass to GND with a 0.1µF capacitor. Connect this pin to the TFT LCD VGON supply. VGON should be between 16.1V and 28V. The HV pin supplies the power for the internal EEPROM writing cycle. The internal writing circuits are disabled when HV is less than 15.6V (typ).
6	SDA	I²C-Compatible Clock Input
7	SCL	I²C-Compatible Serial Bidirectional Data Line
8	SET	Full-Scale Sink-Current Adjustment Input. Connect a resistor, R_{SET}, from SET to GND to set the full-scale adjustable sink current. The full-scale adjustable sink current is equal to: $\left(\frac{V_{AVDD}}{20 \times R_{SET}}\right)$ I_{OUT} is equal to the current through R_{SET}.

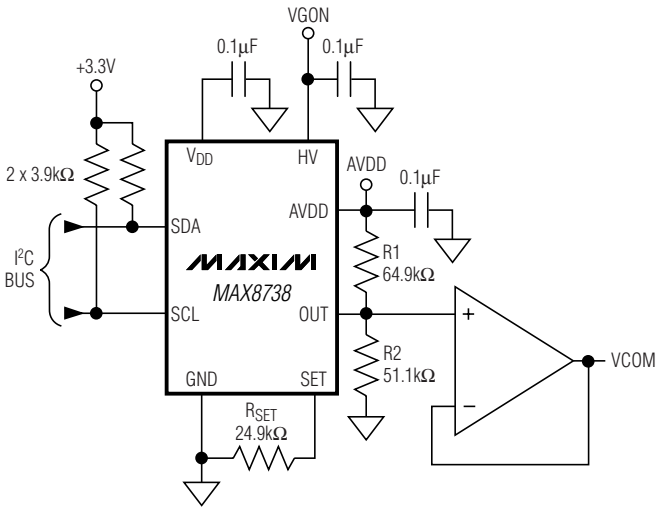


Figure 2. Standard Application Circuit

EEPROM-Programmable TFT VCOM Calibrator with I²C Interface

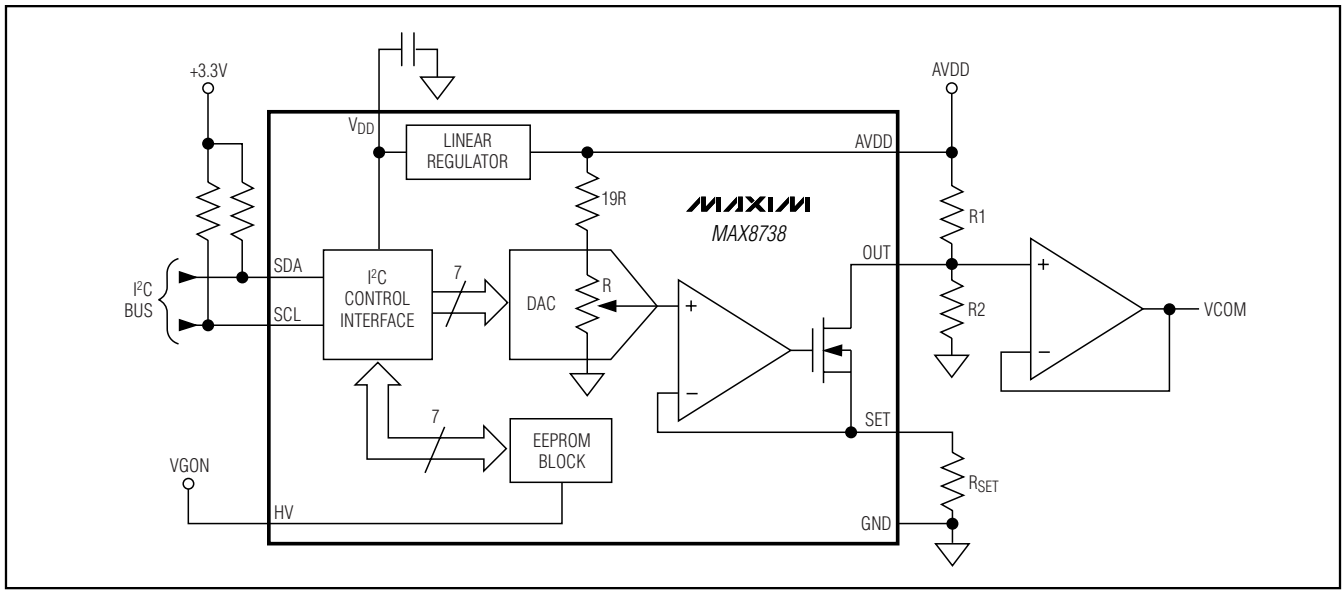


Figure 3. Simplified Functional Diagram

Detailed Description

The MAX8738 is a solid-state alternative to mechanical potentiometers used for adjusting the LCD backplane voltage (VCOM) in TFT LCD displays. The MAX8738 attaches to an external resistive voltage-divider and sinks a programmable current (I_{OUT}), which sets the VCOM level (Figure 2). An internal 7-bit DAC controls the sink current and allows the user to increase or decrease the VCOM level (Figure 3). The DAC is ratiometric relative to V_{AVDD} and is monotonic over all operating conditions. The user can store the DAC setting in an internal EEPROM. On power-up, the EEPROM presets the DAC to the last stored setting. The 2-wire I²C interface between the LCD panel and the programming circuit adjusts the DAC and programs the EEPROM.

The resistive voltage-divider and the AVDD supply set the maximum value of VCOM. The MAX8738 sinks current from the voltage-divider to reduce the VCOM level. The external resistor R_{SET} sets the full-scale sink current and the minimum value of VCOM.

Supply Voltages

AVDD and V_{DD}

The MAX8738 has an internal linear regulator that generates a 3.6V V_{DD} voltage from the AVDD supply voltage. The V_{DD} voltage supplies power to the MAX8738 and should not be used for external loads. AVDD accepts voltages from 4.5V to 20V. Bypass AVDD and V_{DD} to GND with a 0.1µF capacitor each.

HV

The HV input provides the high voltage required to program the EEPROM. The HV pin is typically connected to the TFT LCD positive gate driver supply (VGON) supply. VGON should be between 16.1V and 28V. EEPROM programming is disabled when HV is below 15.6V (typ). Bypass HV to GND with a 0.1µF capacitor.

The EEPROM programming block is turned off when the MAX8738 first powers up, and also immediately after the EEPROM is programmed. When the EEPROM programming block is off, the HV supply current is less than 1µA.

After the MAX8738 receives any command that changes the DAC value, the EEPROM programming block is enabled, and the HV supply current increases to 15µA (typ). During the programming of the EEPROM, the HV supply current may draw up to 60µA (max).

Setting the VCOM Adjustment Range (R_{SET})

The external resistive voltage-divider sets the maximum value of the VCOM adjustment range. R_{SET} sets the full-scale sink current, I_{OUT}, which determines the minimum value of the VCOM adjustment range. Large R_{SET} values increase resolution but decrease the VCOM adjustment range. Calculate R1, R2, and R_{SET} using the following procedure:

1) Choose the maximum VCOM level (V_{MAX}), the minimum VCOM level (V_{MIN}), and the AVDD supply voltage (V_{AVDD}).
2) Select R1 between 10kΩ and 500kΩ based on the acceptable power loss from the AVDD supply rail.
3) Calculate R2:

$$R2 \cong \frac{V_{MAX}}{(V_{AVDD} - V_{MAX})} \times R1$$

4) Calculate R_{SET}:

$$R_{SET} = \frac{V_{MAX}}{20 \times (V_{MAX} - V_{MIN})} \times R1$$

5) Verify that $I_{SET(MAX)}$ does not exceed 120µA:

$$I_{SET(MAX)} = \frac{V_{AVDD}}{20 \times R_{SET}} \leq 120\mu A$$

6) If I_{SET} exceeds 120µA, return to step 2 and choose a larger value for R1.
7) The resulting resolution is:

$$\frac{(V_{MAX} - V_{MIN})}{127}$$

A complete design example is given below:

1) V_{MAX} = 5V, V_{MIN} = 3V, V_{AVDD} = 10V.
2) If R1 = 200kΩ, then R2 = 200kΩ and R_{SET} = 24.9kΩ.
3) $I_{SET(MAX)}$ = 20µA.
4) Resolution = 15.75mV.

Translating Existing Potentiometer Circuits

Existing VCOM adjustment circuits using conventional mechanical potentiometers can be translated into MAX8738 circuits. Figures 4 and 5 show two common adjustment circuits and their equivalent MAX8738 circuits.

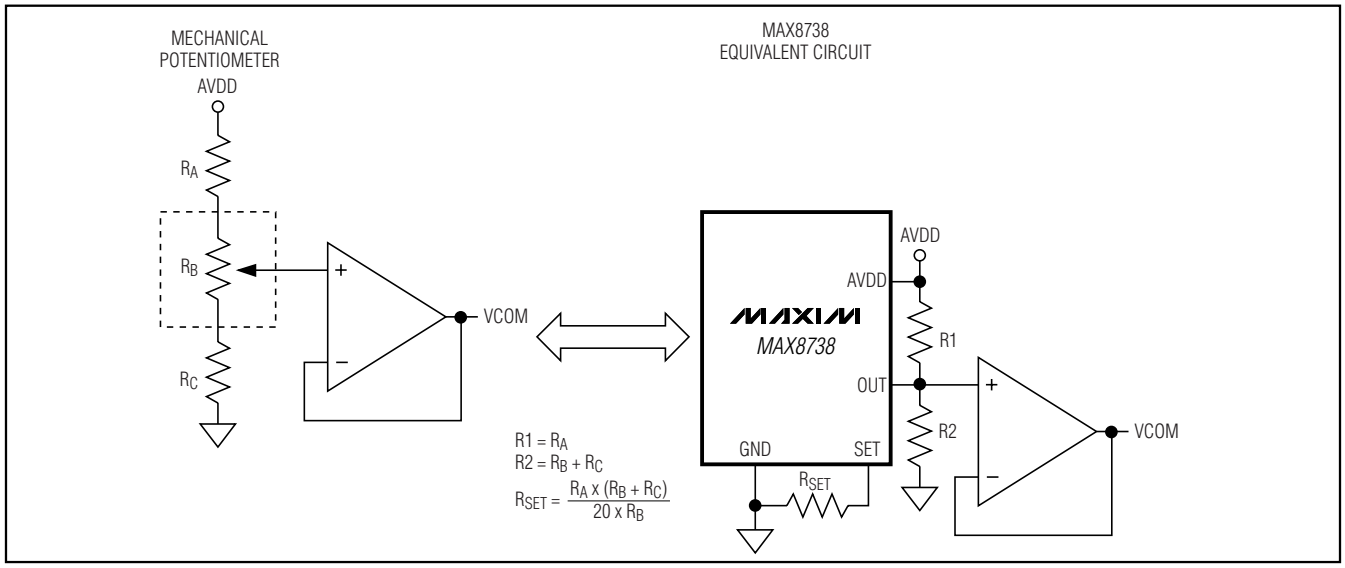


Figure 4. Replacement of Mechanical Potentiometer Circuit

EEPROM-Programmable TFT VCOM Calibrator with I²C Interface

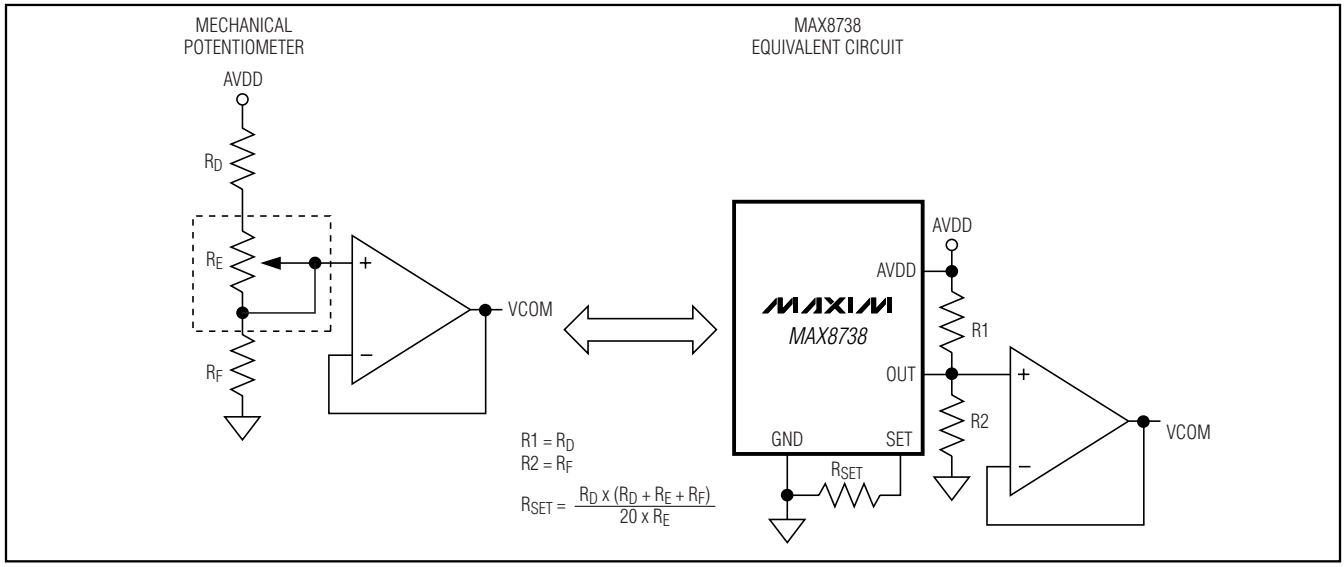


Figure 5. Replacement of Mechanical Potentiometer Circuit

Applications Information

I²C-Bus-Compatible Interface

The MAX8738 is a receive-only device with an I²C address of 5Eh. The 2-wire, I²C-bus-compatible serial interface (pins SCL and SDA) is designed to attach to a I²C bus. Connect both SCL and SDA lines to the positive bus supply through individual pullup resistors. Calculate the required value of the pullup resistors using:

$$R_{PULLUP} \leq \frac{t_R}{C_{BUS}}$$

where t_R is the rise time in the *Electrical Characteristics*, and C_{BUS} is the total capacitance on the bus.

The MAX8738 is compatible with the standard I²C interface protocol as defined in the following subsections. See Figure 6.

Bus Not Busy

The I²C bus is not busy when both data and clock lines remain HIGH. Data transfers may be initiated only when the bus is not busy.

START Data Transfer (S)

Starting from an idle bus state (both SDA and SCL are high), a START condition consists of a HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH. All commands must be preceded by a START condition.

STOP Data Transfer (P)

A STOP condition consists of a LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH. All operations must be ended with a STOP condition.

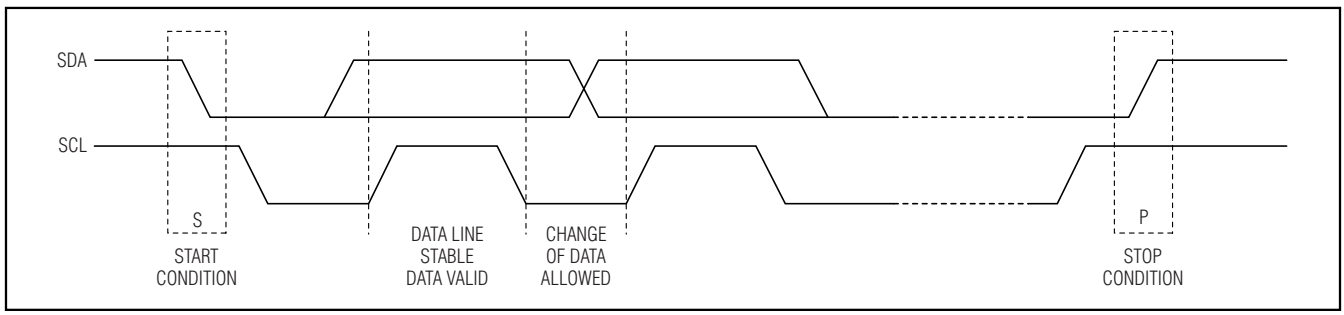


Figure 6. I²C Bus START, STOP, and Data Change Conditions

Slave Address

After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (0b0101111 or 5Eh) for the MAX8738. Since the MAX8738 is a write-only device, the eighth bit of the slave address is zero. The MAX8738 monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit when it recognizes its address.

SDA Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. See Figure 7.

The MAX8738 does not acknowledge the program EEPROM command (AAh) if HV is below 15.6V (typ) or if the MAX8738 is not in program mode.

The MAX8738 does not acknowledge any command while an internal programming cycle is in progress. Once the internally timed EEPROM write cycle has started, acknowledge polling can be initiated. This involves repeatedly sending a 55h command. Only if the internal write cycle has completed does the MAX8738 acknowledge the command.

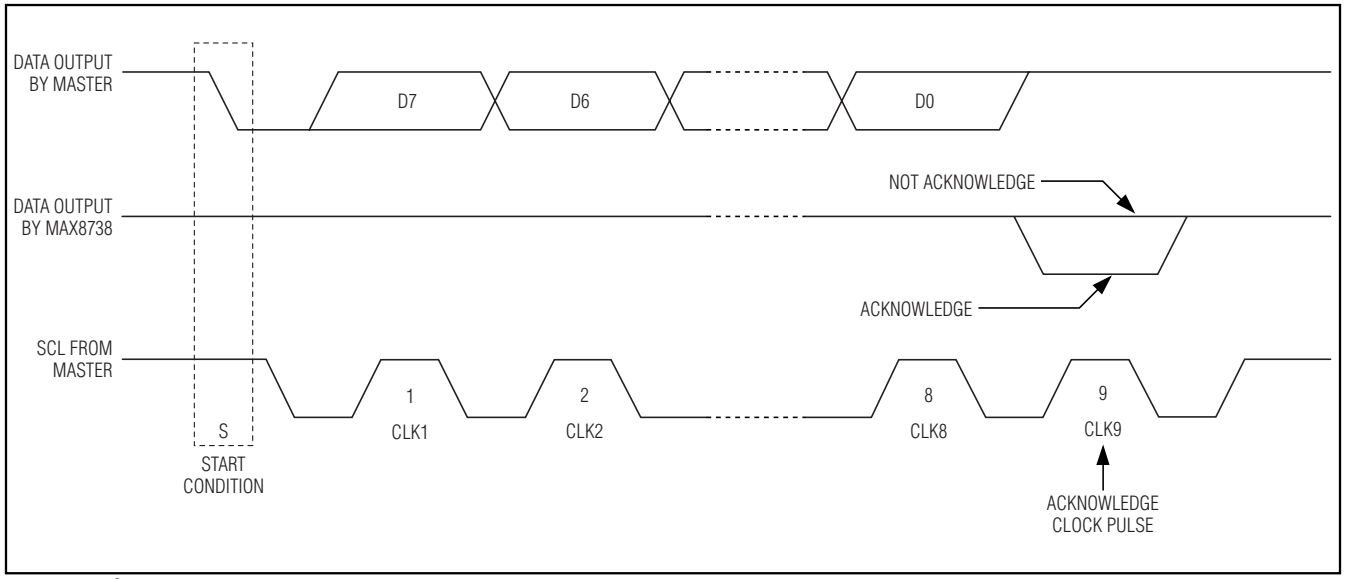


Figure 7. I²C Bus Acknowledge

EEPROM-Programmable TFT VCOM Calibrator with I²C Interface

Table 1. Command Byte Functions

BYTE	FUNCTION	FIGURE
00h	Decrement the DAC setting by 1 LSB	8A
FFh	Increment the DAC setting by 1 LSB	8A
AAh	Write the current DAC setting to EEPROM	8A
55h	Load the EEPROM setting to the DAC	8A
11h	Write a specific value to the DAC	8B

Command Byte

A complete command consists of a START condition (S) followed by the MAX8738's slave address (5Eh) and a command byte, or a command byte and a DAC value, followed by a STOP condition (P). There are five commands, and their functions are listed in Table 1.

DAC Values

Table 2 lists the DAC values and the corresponding I_{SET}, V_{SET}, and V_{OUT} values.

Layout Information

Use the following guidelines for good layout:

1) Place the VCOM buffer and the R1/R2 voltage-divider close to the OUT pin (Figure 2).
2) Place R_{SET} close to SET.

Table 2. DAC Settings

DAC VALUE	I_{SET}	V_{SET} (V)	V_{OUT} (V)
FFh	$I_{SET(MAX)}$	$V_{SET(MAX)}$	V_{MIN}
FEh	$I_{SET(MAX)}$ - 1 LSB	$V_{SET(MAX)}$ - 1 LSB	V_{MIN} + 1 LSB
. . .	. . .	. . .	. . .
01h	$I_{SET(MIN)}$ + 1 LSB	$V_{SET(MIN)}$ + 1 LSB	V_{MAX} - 1 LSB
00h	$I_{SET(MIN)}$	$V_{SET(MIN)}$	V_{MAX}

3) Bypass V_{DD} and AVDD with 0.1µF capacitors placed close to the IC with short connections to the pins.
4) Refer to the MAX8738 evaluation kit for an example of proper board layout.

Chip Information

TRANSISTOR COUNT: 6198

PROCESS: BiCMOS

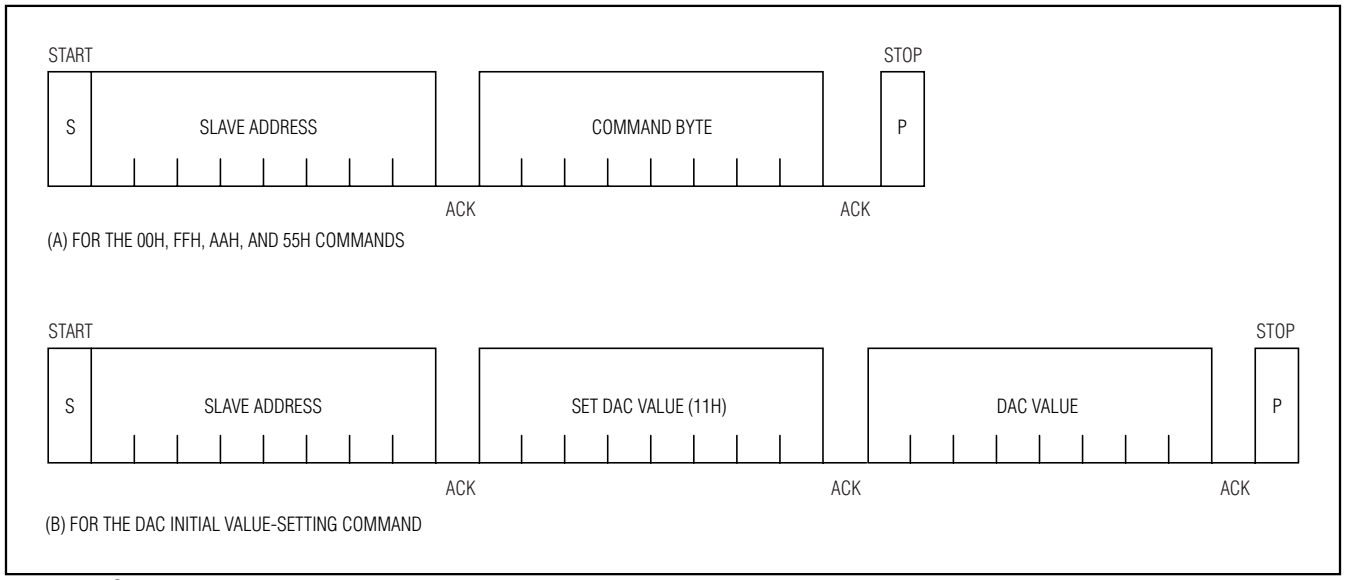
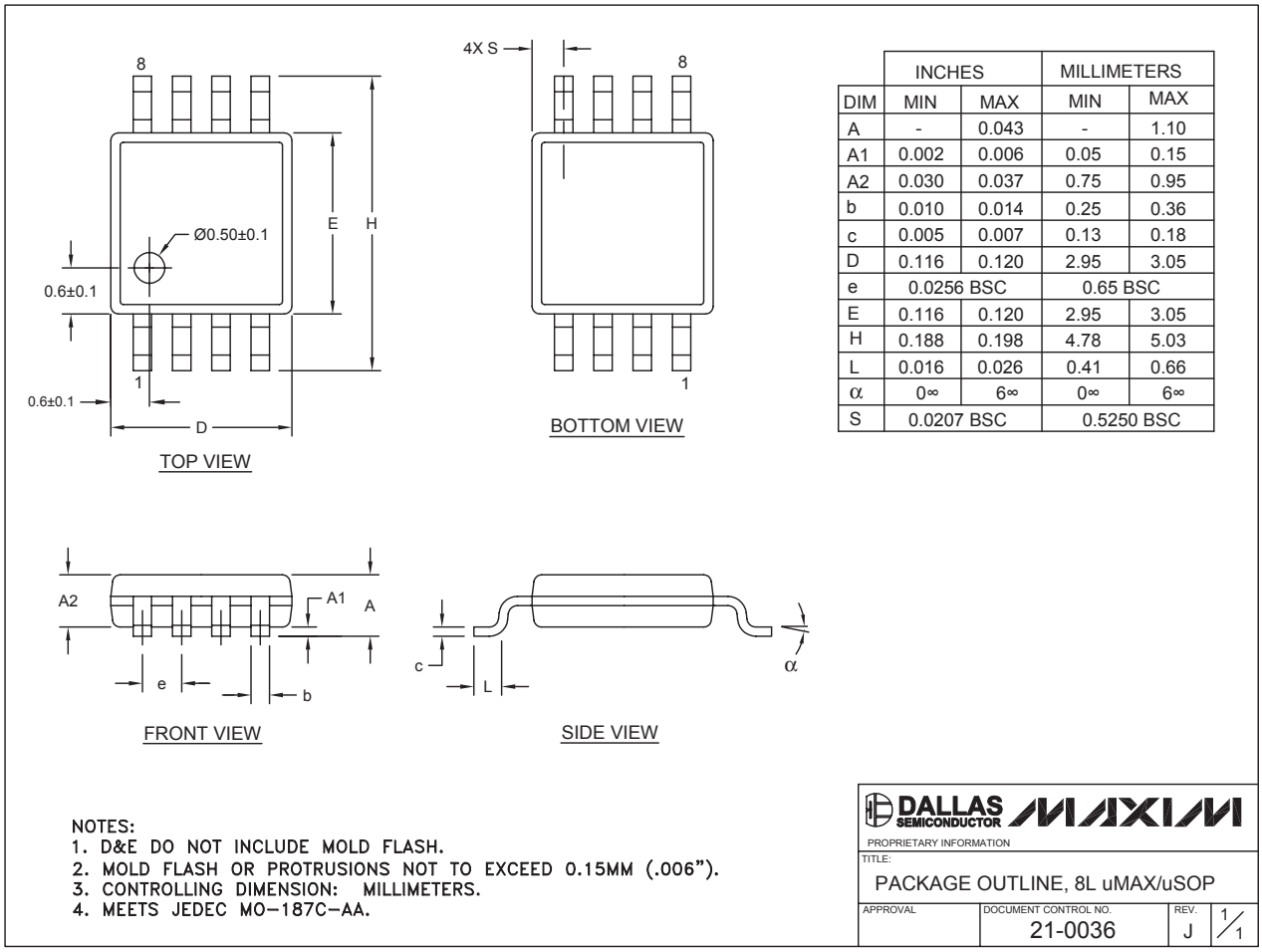


Figure 8. I²C Bus Data Transfer Summary

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0∞	6∞	0∞	6∞
S	0.0207 BSC		0.5250 BSC	

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1