Image Correction ICs

Image Correction IC for Camera

BU1571KN

No.10060ECT01

●Description

BU1571KN is AIE : Adaptive Image Enhancer (image processing technology by ROHM's hardware).
Provides unprecedented visibility under severe conditions, such as darkness or extreme backlighting.

●Features

1) UXGA size (1600×1200) for input of image data up to 7.5 fps, SXGA size (1280×1024) for input of image data up to 15 fps and VGA size (640×480) for input of image data up to 30 fps.
2) Input data format for YUV=4:2:2 8bit. Order of components may be adjusted by the register.
3) Operation modes are image enhance mode, through mode, and sleep mode.
4) Strength of image correction can be set to linear.
5) Register can be set up with a 2-line serial interface.
*Extra document is prepared separately about each register setup. Please refer to the Development Scheme on page 6.

●Application

Security camera, Intercom with camera, Drive recorder, and Web camera etc.

●Lineup matrix

Parameter	Supply power source voltage	Camera Interface	Control Interface	Output Interface	Interrupt output	Package
BU1571KN	1.45-1.55(V_{DD}Core) 2.7-3.6(V_{DD}Io)	Supported up to Max 2M pixels. (1600 × 1200)	I^2C BUS	8bit YUV=4:2:2 Camera interface	-	VQFN36

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply power source voltage 1	VDDIO	-0.3 ~ +4.2	V
Supply power source voltage 2	VDD	-0.3 ~ +2.1	V
Input voltage	VIN	-0.3 ~ VDDIO+0.3	V
Storage temperature range	Tstg	-40 ~ +125	℃
Power dissipation	PD	450	mW

*In the case exceeding 25℃, 4.5mW should be reduced at the rating 1℃.

●Recommended operating range

Parameter	Symbol	Ratings	Unit
Supply power source voltage 1(IO)	VDDIO	2.70 ~ 3.60(Typ:3.3V)	V
Supply power source voltage 2(CORE)	VDD	1.45 ~ 1.55(Typ:1.50V)	V
Input voltage range	VIN-VDDIO	0 ~ VDDIO	V
Operating temperature range	Topr	-40 ~ +85	℃

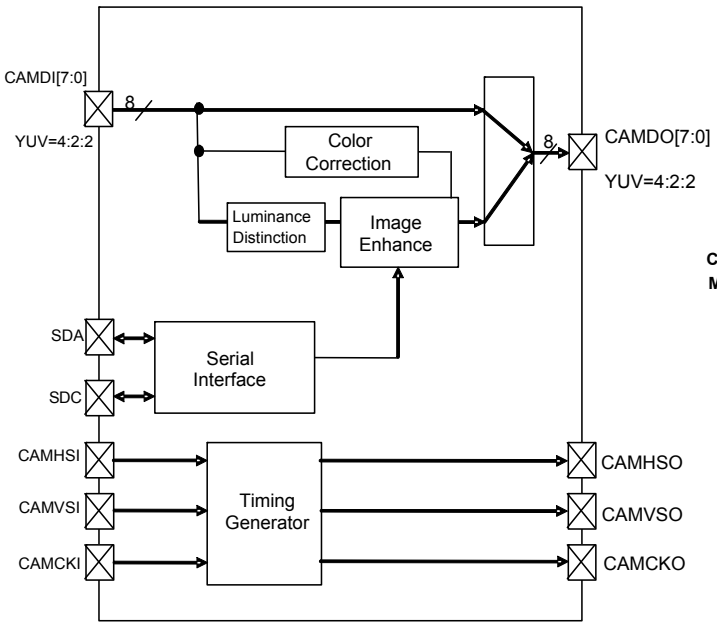
*Please supply power source in order of VDD→VDDIO.

●Electric characteristics

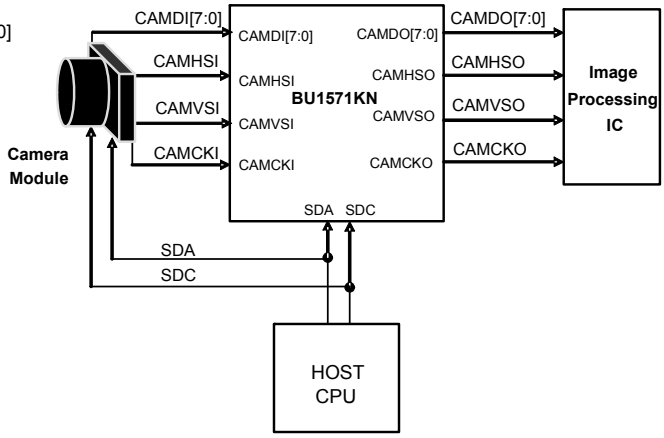
(Unless otherwise specified, VDD=1.50V,VDDIO=3.3V,GND=0.0V,Ta=25℃,f_{IN}=52.0MHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input frequency	f_{IN}	10.0	-	52.0	MHz	CAMCKI(DUTY45% ~ 55%)
Operating consumption current	IDD1	-	15	-	mA	At enhance mode setting
Static consumption current	IDDst	-	-	30	μA	At sleep mode setting, input terminal=GND setting
Input ”H” current 1	IIH1	-10	-	10	μA	VIH=VDDIO
Input ”H” current 2	IIH2	35	70	140	μA	Pull-Down terminal, VIH=VDDIO
Input ”L” current 1	IIL1	-10	-	10	μA	VIL=GND
Input ”L” current 2	IIL2	-10	-	10	μA	Pull-Down terminal, VIL=GND
Input ”H” voltage 1	VIH1	VDDIO ×0.8	-	VDDIO +0.3	V	Normal input (including input mode of I/O terminal)
Input ”L” voltage 1	VIL1	-0.3	-	VDDIO ×0.2	V	Normal input (including input mode of I/O terminal)
Input ”H” voltage 2	VIH2	VDDIO ×0.85	-	VDDIO +0.3	V	Hysteresis input (RESETB, CAMCKI, SDA, SDC)
Input ”L” voltage 2	VIL2	-0.3	-	VDDIO ×0.15	V	Hysteresis input (RESETB, CAMCKI, SDA, SDC)
Hysteresis voltage width	Vhys	-	0.5	-	V	Hysteresis input (RESETB, CAMCKI, SDA, SDC)
Output ”H” voltage	VOH	VDDIO -0.4	-	VDDIO	V	IOH=-1.0mA(DC) (including input mode of I/O terminal)
Output ”L” voltage	VOL	0.0	-	0.4	V	IOL=1.0mA(DC) (including input mode of I/O terminal)

●Block Diagram



●Recommended Application Circuit



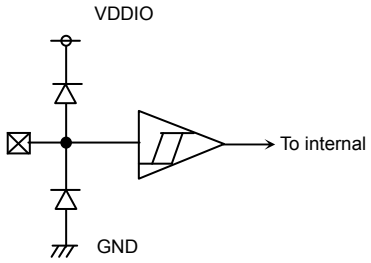
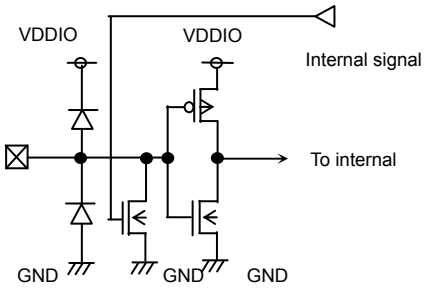
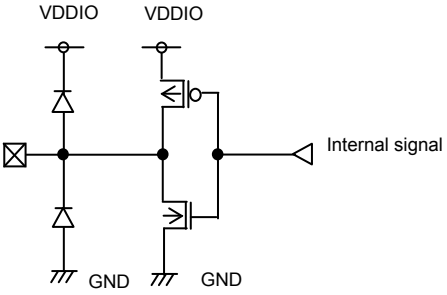
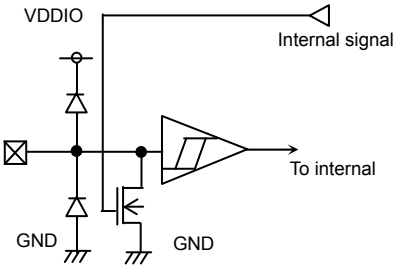
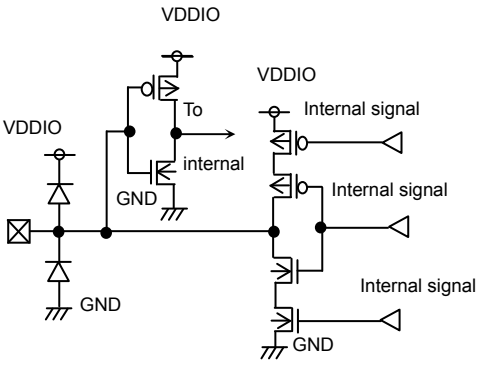
*Extra document is prepared separately about system evaluation. Please refer to the Development Scheme on page 6.

●**Terminal functions**

PIN No.	PIN Name	In/Out	Active Level	Init	Function explanation	I/O type
1	CAMVSI	In	*	-	Vertical Timing Input (pull-down at sleep mode)	B*1
2	N.C.					
3	CAMHSI	In	*	-	Horizontal Timing Input (pull-down at sleep mode)	B*1
4	CAMDI0	In	DATA	-	Data Input Bit 0 (pull-down at sleep mode)	B*1
5	CAMDI1	In	DATA	-	Data Input Bit 1 (pull-down at sleep mode)	B*1
6	CAMDI2	In	DATA	-	Data Input Bit 2 (pull-down at sleep mode)	B*1
7	CAMDI3	In	DATA	-	Data Input Bit 3 (pull-down at sleep mode)	B*1
8	CAMDI4	In	DATA	-	Data Input Bit 4 (pull-down at sleep mode)	B*1
9	CAMDI5	In	DATA	-	Data Input Bit 5 (pull-down at sleep mode)	B*1
10	CAMDI6	In	DATA	-	Data Input Bit 6 (pull-down at sleep mode)	B*1
11	CAMDI7	In	DATA	-	Data Input Bit 7 (pull-down at sleep mode)	B*1
12	VDDIO	-	PWR	-	DIGITAL IO Power Source	-
13	CAMCKI	In	CLK	-	Clock Input (pull-down at sleep mode)	D*1
14	GND	-	GND	-	Common GROUND	-
15	VDD	-	PWR	-	CORE Power Source	-
16	SDA	In/Out	DATA	In	In/Output Serial Data	E
17	SDC	In/Out	CLK	In	In/Output Serial Clock	E
18	TESTOUT	Out	High	-	TEST Out Pin (Keep Open)	-
19	CAMVSO	Out	-	-	Vertical Timing Signal Output	C
20	N.C.					
21	CAMHSO	Out	-	-	Horizontal Timing Signal Output	C
22	CAMDO0	Out	DATA	-	Data Output: Bit 0	C
23	CAMDO1	Out	DATA	-	Data Output: Bit 1	C
24	CAMDO2	Out	DATA	-	Data Output: Bit 2	C
25	CAMDO3	Out	DATA	-	Data Output: Bit 3	C
26	CAMDO4	Out	DATA	-	Data Output: Bit 4	C
27	CAMDO5	Out	DATA	-	Data Output: Bit 5	C
28	CAMDO6	Out	DATA	-	Data Output: Bit 6	C
29	CAMDO7	Out	DATA	-	Data Output: Bit 7	C
30	TEST1	In	Low	-	Test Mode Terminal 1 (Connect to GND)	B
31	TEST2	In	Low	-	Test Mode Terminal 2 (Connect to GND)	B
32	RESETB	In	Low	-	System Reset Signal	A
33	VDDIO	-	PWR	-	DIGITAL IO Power Source	-
34	CAMCKO	Out	CLK	-	Clock Output	C
35	GND	-	GND	-	Common GROUND	-
36	VDD	-	PWR	-	CORE Power Source	-

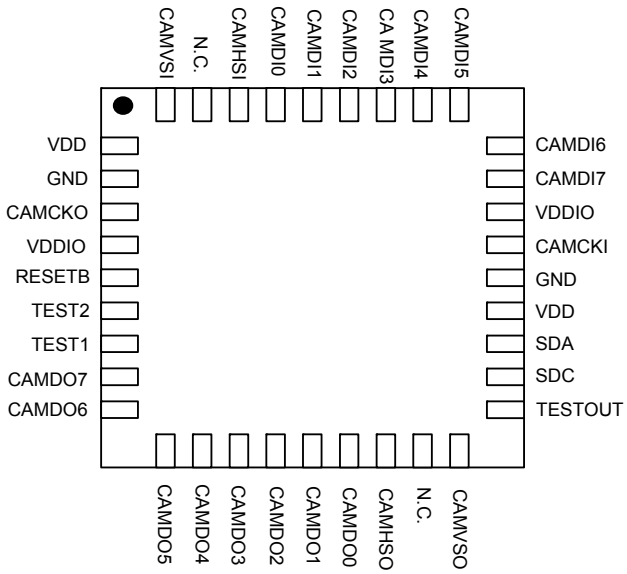
"" in the Active Level column indicates that it may be changed during set-up of the register. Init indicates pin status when released from reset.
*1: Pull-down is ON during reset (initial status).

●**Equivalent Circuit Structures of input / output pins**

Type	The equivalent circuit structure	Type	The equivalent circuit structure
A	 Input terminal with Schmitt	**B**	 Input terminal with PULL-DOWN
C	 Output terminal	**D**	 Hysteresis input terminal with PULL-DOWN
E	 Hysteresis input / output terminal		

●**Terminal Layout**

(Bottom View)



●Timing Chart

1. Two-line serial interface
   1.1 Two-line serial interface timing

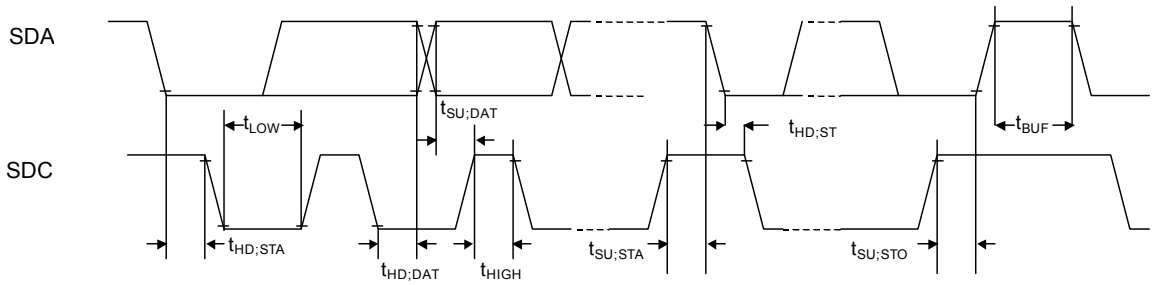


Table 1 I^2C Interface timing

Symbol	Parameter	MIN.	TYP.	MAX.	Unit
f_{SCL}	SDC Clock Frequency	0	-	400	kHz
$t_{HD;STA}$	Hold-time(repetition) 『START』 conditions (The first clock pulse is generated after this period.)	0.6	-	-	μs
f_{LOW}	The "L" period of SDC clock	1.3	-	-	μs
t_{HIGH}	The "H" period of SDC clock	0.6	-	-	μs
$t_{SU;STA}$	Setup time of repetitive 『START』 conditions	0.6	-	-	μs
$t_{HD;DAT}$	Hold time of SDA	0	-		μs
$t_{SU;DAT}$	Setup time of SDA	100	-	-	ns
$t_{SU;STO}$	Setup time of the 『STOP』 conditions	0.6	-	-	μs
t_{BUF}	BUS free time between 『STOP』 conditions and the 『START』 conditions	1.3	-	-	μs

2. Camera module interface
   2.1. Camera module interface timing
   The input timing of camera image signal on camera I/F is shown in Table 2.

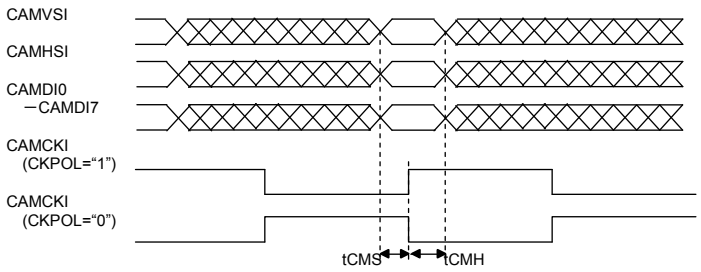


Table 2. BU1571KN timing (Camera data input)

Symbol	Explanation	MIN.	TYP.	MAX.	UNIT
tCMS	CAMCKI Rise / Fall Camera set-up Time	4	-	-	ns
tCMH	CAMCKI Rise / Fall Camera Hold Time	4	-	-	ns

The input timing of camera image signal on camera I/F is shown in Table 2.1-2.

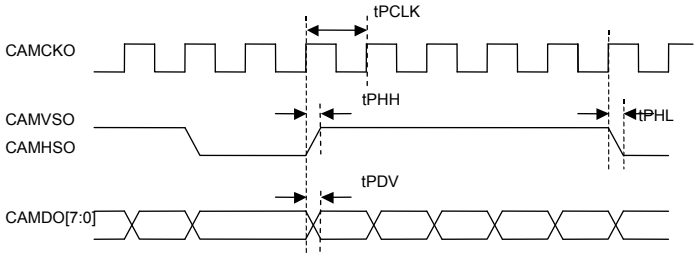


Table 2. Camera data output timing

Symbol	Explanation	MIN.	TYP.	MAX.	UNIT
tPCLK	Clock Cycle	19.2	-	-	ns
dPCLK	Clock Duty	45	50	55	%
tPDV	Decision of CAMDO from CAMCKO	-	-	5	ns
tPHL, tPHH	Decision of CAMVSO or CAMHSO from CAMCKO	-	-	5	ns

●Development Scheme

This technical note is aimed at trying the connectivity in the hardware between customer's system and our AIE Adaptive Image Enhancer series.
We prepare various data and tools for every development STEP as follows other than this technical note, please contact the sales staff in your duty also including the support system.

(1) Demonstration STEP

(You can try the standard image processing functions by the standard Demonstration kit at once.)

You can confirm on TV screen what carried out AIE processing of a camera image and the DVD video image.

・Standard Demonstration board kit

◎Demonstration board(TV-IN→BU1571KN→TV-OUT board)
◎Demonstration board operation manual
◎Demonstration software
If the software for the trial board is installed in your Windows PC(Windows 2000/XP), more detailed setting is possible.
◎USB cable

(2) Confirmation STEP

(We will respond to customer's camera module.)

・Specifications
We will provide specifications for AIE Adaptive Image Enhancer according to customer's requirements.

・Function explanation
We will deliver you the function explanation describing detailed functions, register settings, external interfaces, timing, and so forth of AIE Adaptive Image Enhancer according to your requests.

・Application note
We will deliver you the detailed explanation data on application development of AIE Adaptive Image Enhancer according to your requests.

(3) System check STEP

(You can check the application operation as a system by the kit of system check tools and your camera module.)

You can check the interface with your camera module and the application operation on the system check board using the tools for user's only.

・System check tools kit

◎Board for system evaluation
◎Manual for system evaluation
◎Macro command file for reference

*You can check the detailed functions of the application operation by your PC using the macro command file.

(4) Integrated check STEP with user's system

(You can check the application operation as a system on your system check board using the integrated check software.)

You can check the application operation on the sample LSI-equipped system check board by your camera module using the integrated check software.

・On line Support ; We will answer your questions about the software development.

●Notes for use

(1)Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2)Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3)Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4)Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5)GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6)Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7)Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8)Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9)Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10)Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11)External capacitor

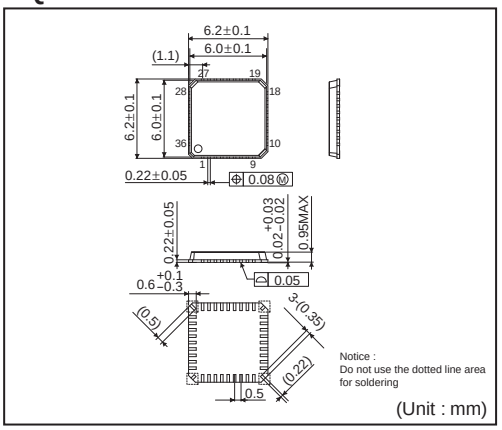
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

●Ordering part number

B	D	1	5	7	1	K	N	-	E	2

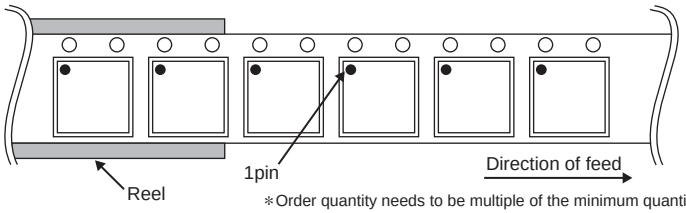
Part No. | Part No. | Package KN:VQFN36 | Packaging and forming specification E2: Embossed tape and reel

VQFN36



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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ROHM SEMICONDUCTOR

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