Integrated Video Filter with Selectable Cutoff Frequencies for RGB, HD/SD Y, C, and CV

ADA4410-6

FEATURES

- Sixth-order filters with selectable cutoff frequencies
  - 36 MHz, 18 MHz, 9 MHz
- Many video standards supported
  - RGB/YPbPr/YUV/SD/YC/CV
- Ideal for resolutions up to 1080i
  - −1 dB bandwidth of 30 MHz for HD
- 2:1 multiplexers on all inputs
- Selectable gain: ×2 or ×4
- DC output offset adjust: ±0.5 V, input referred
- Excellent video specifications
  - NTSC differential gain: 0.11%
  - NTSC differential phase: 0.25°
- Low input bias current: 6.6 µA
- Wide supply range: +4.5 V to ±5 V
- Rail-to-rail output
  - Typical output swing of 4.5 V p-p on single 5 V supply
- Disable feature

APPLICATIONS

- Set-top boxes
- DVD players and recorders
- HDTVs

GENERAL DESCRIPTION

The ADA4410-6 is a comprehensive integrated filtering solution that is carefully designed to give designers the flexibility to easily filter and drive many types of video signals, including high definition video. In the RGB/component channels, the cutoff frequencies of the sixth-order filters can be selected by two logic pins to obtain four filter combinations that are tuned for RGB, high definition, and standard definition video. Cutoff frequencies range from 9 MHz to 36 MHz.

The ADA4410-6 also provides filtering for the legacy standard S-video and composite video signals. With a differential gain of 0.11% and a differential phase of 0.25°, the ADA4410-6 is an excellent choice for any composite video (CV) application.

The ADA4410-6 offers gain and output offset voltage adjustments. With a single logic pin, the gain of the part can be selected to be ×2 or ×4. Output offset voltage is continuously adjustable over an input-referred range of ±500 mV by applying a differential voltage to an independent offset control input.

FUNCTIONAL BLOCK DIAGRAM

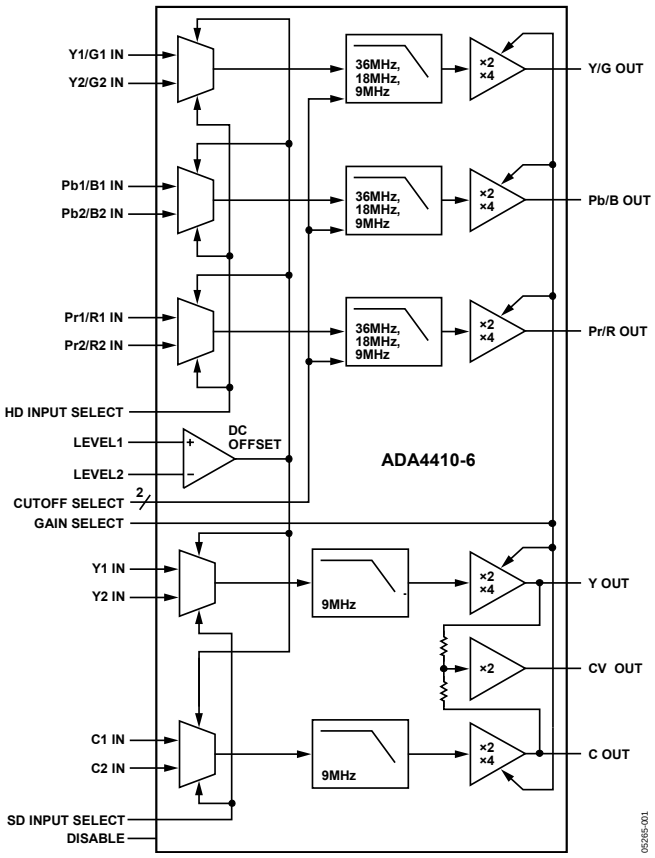

Figure 1.

The ADA4410-6 offers 2:1 multiplexers on its inputs that can be used in applications where multiple sources of video exist.

The ADA4410-6 can operate on a single +5 V supply as well as ±5 V supplies. Single-supply operation is ideal for applications where power consumption is critical. The disable feature allows for further power conservation by reducing the supply current to typically 15 µA when a particular device is not in use.

Dual-supply operation is best for applications where the negative-going excursions of the signal must swing at or below ground while maintaining excellent video performance. The output buffers have the ability to drive two 75 Ω doubly terminated cables that are either dc- or ac-coupled.

The ADA4410-6 is available in a 32-lead LFCSP and operates in the extended industrial temperature range of −40°C to +85°C.

Rev. B

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SPECIFICATIONS

V_S = 5 V, @ T_A = 25°C, V_O = 1.4 V p-p, G = ×2, R_L = 150 Ω, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL PERFORMANCE					
Offset Error	Input referred, all channels except CV		10	32	mV
	Input referred, CV		12	40	mV
Max Voltage Across LEVEL1 and LEVEL2 Inputs			±500		mV
Input Voltage Range, All Inputs		V_{S-} − 0.1		V_{S+} − 2.0	V
Output Voltage Swing, All Outputs	Positive swing	V_{S+} − 0.35	V_{S+} − 0.25		V
	Negative swing		V_{S-} + 0.10	V_{S-} + 0.3	V
Linear Output Current per Channel			30		mA
Integrated Voltage Noise, Referred to Input	All channels except CV		500		μV_{rms}
Filter Input Bias Current	All channels		6.6	15	µA
Total Harmonic Distortion at 1 MHz	F_C = 36 MHz, F_C = 18 MHz/F_C = 9 MHz		0.01/0.07		%
RGB/YPbPr CHANNEL DYNAMIC PERFORMANCE					
−1 dB Bandwidth	Cutoff frequency select = 36 MHz		31		MHz
	Cutoff frequency select = 18 MHz		15		MHz
	Cutoff frequency select = 9 MHz		8		MHz
−3 dB Bandwidth	Cutoff frequency select = 36 MHz	34	36		MHz
	Cutoff frequency select = 18 MHz	16	18		MHz
	Cutoff frequency select = 9 MHz	8	9		MHz
Out-of-Band Rejection	f = 75 MHz	−33	−42		dB
Crosstalk	f = 5 MHz, F_C = 36 MHz		−68		dB
Input Mux Isolation	f = 1 MHz, R_{SOURCE} = 300 Ω		86		dB
Propagation Delay	f = 16 MHz, F_C = 36 MHz		20.5		ns
Group Delay Variation	Cutoff frequency select = 36 MHz		9.5		ns
	Cutoff frequency select = 18 MHz		16.5		ns
	Cutoff frequency select = 9 MHz		29.5		ns
Y/C SD CHANNEL DYNAMIC PERFORMANCE					
−1 dB Bandwidth			7.5		MHz
−3 dB Bandwidth		8	9		MHz
Out-of-Band Rejection	f = 27 MHz		−56		dB
Propagation Delay	f = 1 MHz		72		ns
Group Delay Variation			30		ns
Crosstalk	f = 1 MHz		−72		dB
Input Mux Isolation	f = 1 MHz, R_{SOURCE} = 75 Ω		77		dB
Y/C, CV OUTPUT VIDEO PERFORMANCE					
Differential Gain	NTSC		0.09		%
Differential Phase	NTSC		0.37		Degrees
CONTROL INPUT PERFORMANCE					
Input Logic 0 Voltage	All inputs except DISABLE			0.8	V
Input Logic 1 Voltage	All inputs except DISABLE	2.0			V
Input Bias Current	All inputs except DISABLE		7	15	µA
DISABLE PERFORMANCE					
DISABLE Assert Voltage			V_{S+} − 0.5		V
DISABLE Assert Time			100		ns
DISABLE Deassert Time			130		ns
DISABLE Input Bias Current			12	20	µA
Input-to-Output Isolation—Disabled			100		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		4.5		12	V
Quiescent Current			82	88	mA
Quiescent Current—Disabled			15	150	µA
PSRR, Positive Supply	All channels except CV	62	72		dB
	CV channel	59	66		dB
PSRR, Negative Supply	All channels except CV	55	62		dB
	CV channel	52	56		dB

V_S = ±5 V, @ T_A = 25°C, V_O = 1.4 V p-p, G = ×2, R_L = 150 Ω, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL PERFORMANCE					
Offset Error	Input referred, all channels except CV		14	33.5	mV
	Input referred, CV		15	42.5	mV
Max Voltage Across LEVEL1 and LEVEL2 Inputs			±500		mV
Input Voltage Range, All Inputs		V_{S-} − 0.1		V_{S+} − 2.0	V
Output Voltage Swing, All Outputs	Positive swing	V_{S+} − 0.35	V_{S+} − 0.25		V
	Negative swing		V_{S-} + 0.3	V_{S-} + 0.5	V
Linear Output Current per Channel			30		mA
Integrated Voltage Noise, Referred to Input	All channels except CV		500		μV_{rms}
Filter Input Bias Current	All channels		6.3	15	µA
Total Harmonic Distortion at 1 MHz	F_C = 36 MHz, F_C = 18 MHz/F_C = 9 MHz		0.01/0.07		%
RGB/YPbPr CHANNEL DYNAMIC PERFORMANCE					
−1 dB Bandwidth	Cutoff frequency select = 36 MHz		29		MHz
	Cutoff frequency select = 18 MHz		15		MHz
	Cutoff frequency select = 9 MHz		8		MHz
−3 dB Bandwidth	Cutoff frequency select = 36 MHz	33.0	35.5		MHz
	Cutoff frequency select = 18 MHz	16.5	18		MHz
	Cutoff frequency select = 9 MHz	8	9.5		MHz
Out-of-Band Rejection	f = 75 MHz	−33	−41.5		dB
Crosstalk	f = 5 MHz, F_C = 36 MHz		−68		dB
Input Mux Isolation	f = 1 MHz, R_{SOURCE} = 300 Ω		86		dB
Propagation Delay	f = 5 MHz, F_C = 36 MHz		21		ns
Group Delay Variation	Cutoff frequency select = 36 MHz		7.5		ns
	Cutoff frequency select = 18 MHz		14		ns
	Cutoff frequency select = 9 MHz		26		ns
Y/C SD CHANNEL DYNAMIC PERFORMANCE					
−1 dB Bandwidth			7.5		MHz
−3 dB Bandwidth		8	9		MHz
Out-of-Band Rejection	f = 27 MHz		−57		dB
Propagation Delay	f = 1 MHz		64		ns
Group Delay Variation			26		ns
Crosstalk	f = 1 MHz		−72		dB
Input Mux Isolation	f = 1 MHz, R_{SOURCE} = 75 Ω		77		dB
Y/C, CV OUTPUT VIDEO PERFORMANCE					
Differential Gain	NTSC		0.11		%
Differential Phase	NTSC		0.25		Degrees
CONTROL INPUT PERFORMANCE					
Input Logic 0 Voltage	All inputs except DISABLE			0.8	V
Input Logic 1 Voltage	All inputs except DISABLE	2.0			V
Input Bias Current	All inputs except DISABLE		7	15	µA
DISABLE PERFORMANCE					
DISABLE Assert Voltage			V_{S+} − 0.5		V
DISABLE Assert Time			75		ns
DISABLE Deassert Time			125		ns
DISABLE Input Bias Current			35	45	µA
Input-to-Output Isolation—Disabled			100		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		4.5		12	V
Quiescent Current			86	93	mA
Quiescent Current—Disabled			15	150	µA
PSRR, Positive Supply	All channels except CV	62	72		dB
	CV channel	59	66		dB
PSRR, Negative Supply	All channels except CV	55	62		dB
	CV channel	52	56		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12 V
Power Dissipation	See Figure 2
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in the circuit board with its exposed paddle soldered to a pad on the PCB surface that is thermally connected to a copper plane.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5 mm × 5 mm, 32-Lead LFCSP	43	5.1	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADA4410-6 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4410-6. Exceeding a junction temperature of 150°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. The power dissipated due to all of the loads is equal to the sum of the power dissipations due to each individual load. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through-holes, ground, and power planes, reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a copper plane to achieve the specified θ_{JA}.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 32-lead LFCSP (43°C/W) on a JEDEC standard 4-layer board with the underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

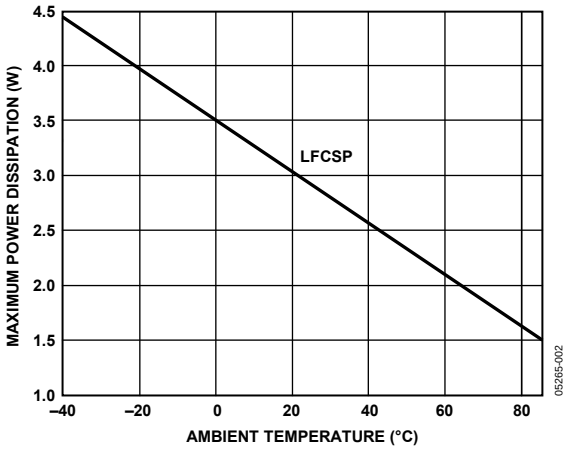

Figure 2. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

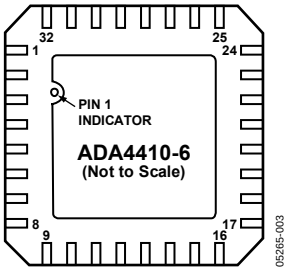

Figure 3. 32-Lead LFCSP Pin Configuration, Top View

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Pb1/B1_HD	Channel 1 Pb/B High Definition Input
2	GND	Signal Ground Reference
3	Pr1/R1_HD	Channel 1 Pr/R High Definition Input
4	F_SEL_A	Filter Cutoff Select Input A
5	F_SEL_B	Filter Cutoff Select Input B
6	Y2/G2_HD	Channel 2 Y/G High Definition Input
7	GND	Signal Ground Reference
8	Pb2/B2_HD	Channel 2 Pb/B High Definition Input
9	GND	Signal Ground Reference
10	Pr2/R2_HD	Channel 2 Pr/R High Definition Input
11	MUX_SD	Standard Definition Input Mux Select Line
12	Y1_SD	Channel 1 Y Standard Definition Input
13	Y2_SD	Channel 2 Y Standard Definition Input
14	C1_SD	Channel 1 C Standard Definition Input
15	C2_SD	Channel 2 C Standard Definition Input
16	VCC	Positive Power Supply
17	VEE	Negative Power Supply
18	CV_OUT	Composite Video Output
19	C_SD_OUT	C Standard Definition Output
20	Y_SD_OUT	Y Standard Definition Output
21	G_SEL	Gain Select
22	Pr/R_HD_OUT	Pr/R High Definition Output
23	Pb/B_HD_OUT	Pb/B High Definition Output
24	Y/G_HD_OUT	Y/G High Definition Output
25	VEE	Negative Power Supply
26	VCC	Positive Power Supply
27	DISABLE	Disable/Power Down/Logic Reference
28	LEVEL2	DC Level Adjust Pin 2
29	LEVEL1	DC Level Adjust Pin 1
30	MUX_HD	High Definition Input Mux Select Line
31	Y1/G1_HD	Channel 1 Y/G High Definition Input
32	GND	Signal Ground Reference

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, G = ×2, R_L = 150 Ω, V_O = 1.4 V p-p, V_S = 5 V, T_A = 25°C.

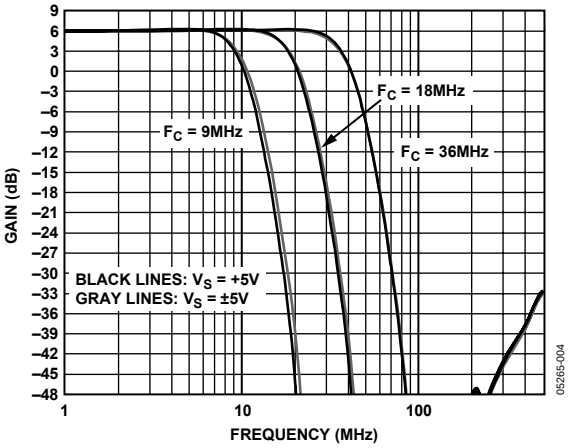

Figure 4. Frequency Response vs. Power Supply and Cutoff Frequency (G = ×2)

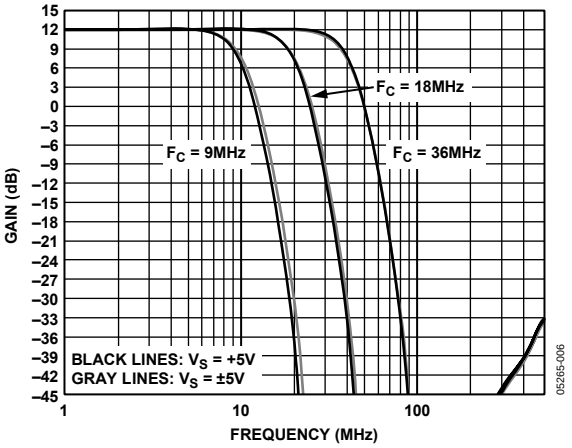

Figure 7. Frequency Response vs. Power Supply and Cutoff Frequency (G = ×4)

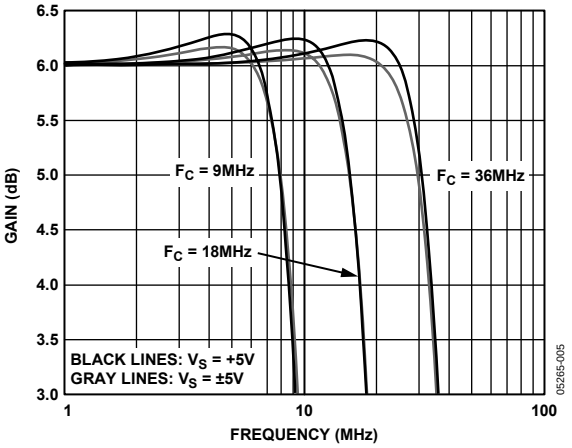

Figure 5. Frequency Response Flatness vs. Cutoff Frequency (G = ×2)

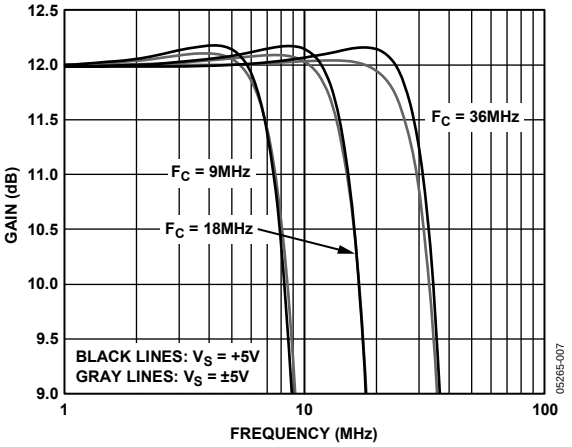

Figure 8. Frequency Response Flatness vs. Cutoff Frequency (G = ×4)

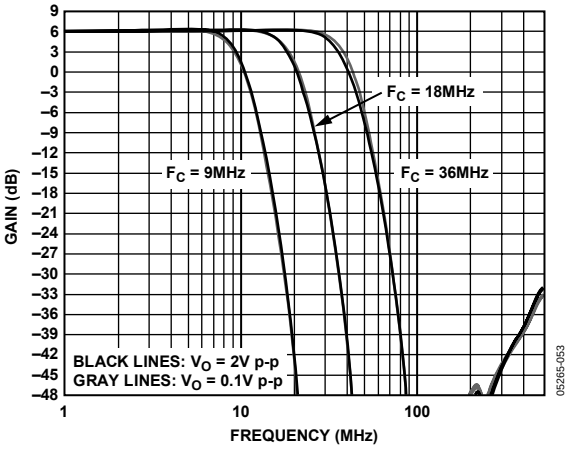

Figure 6. Frequency Response vs. Cutoff Frequency and Output Amplitude

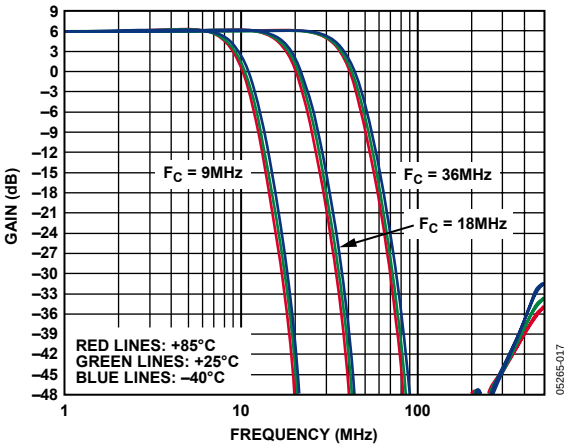

Figure 9. Frequency Response vs. Temperature and Cutoff Frequency

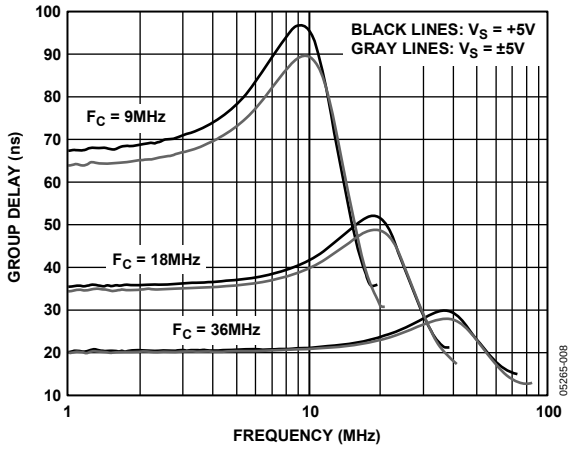

Figure 10. Group Delay vs. Frequency, Power Supply, and Cutoff Frequency

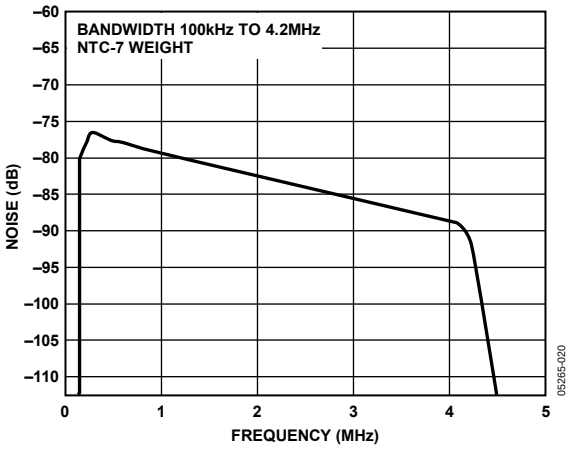

Figure 13. CV Noise Spectrum

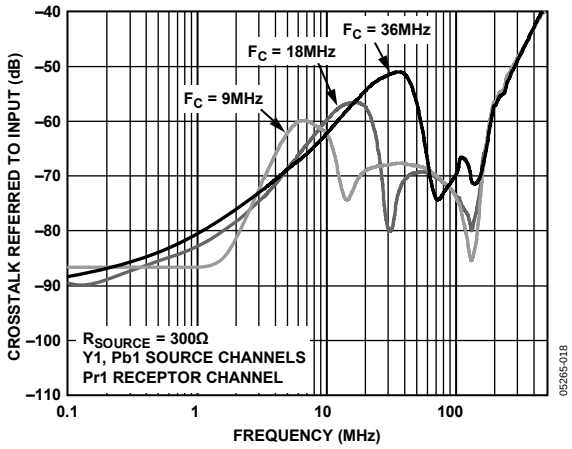

Figure 11. HD Channel Crosstalk vs. Frequency and Cutoff Frequency

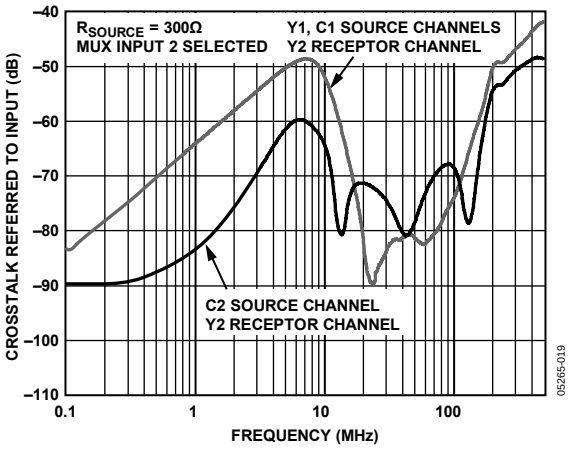

Figure 14. SD Channel Crosstalk vs. Frequency

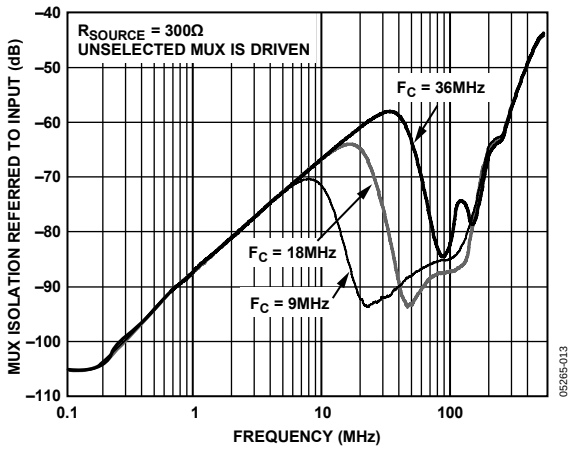

Figure 12. HD Mux Isolation vs. Frequency and Cutoff Frequency

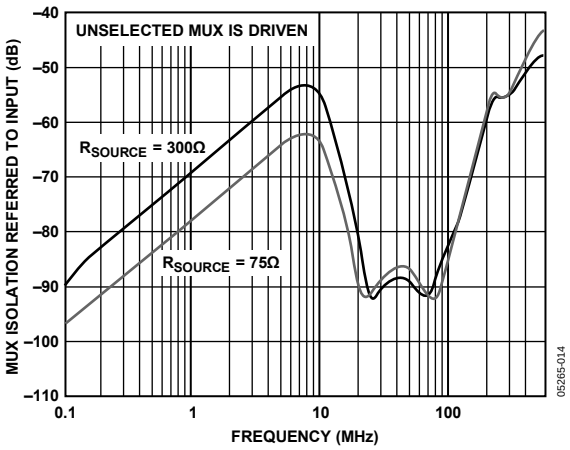

Figure 15. SD Mux Isolation vs. Frequency and Source Resistance

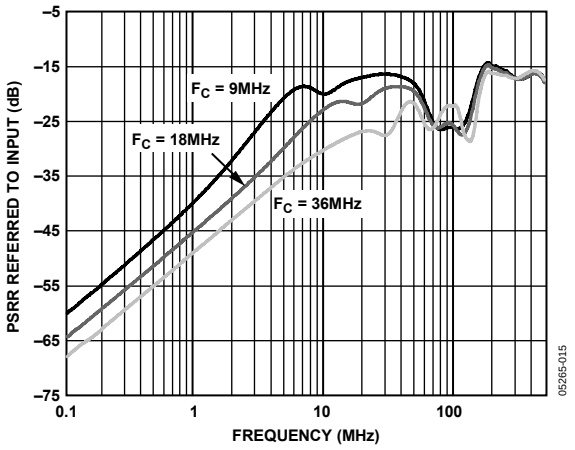

Figure 16. Positive Supply PSRR vs. Frequency and Cutoff Frequency

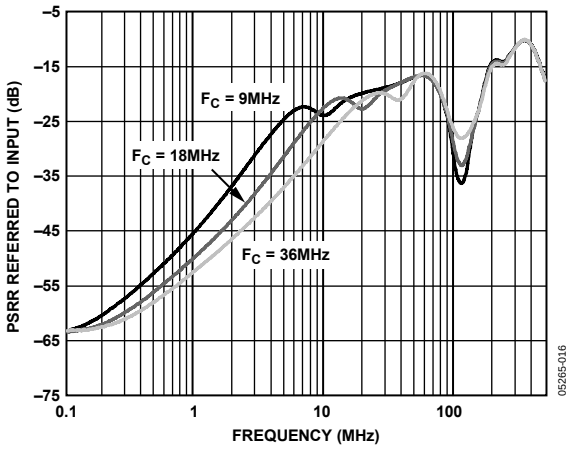

Figure 19. Negative Supply PSRR vs. Frequency and Cutoff Frequency

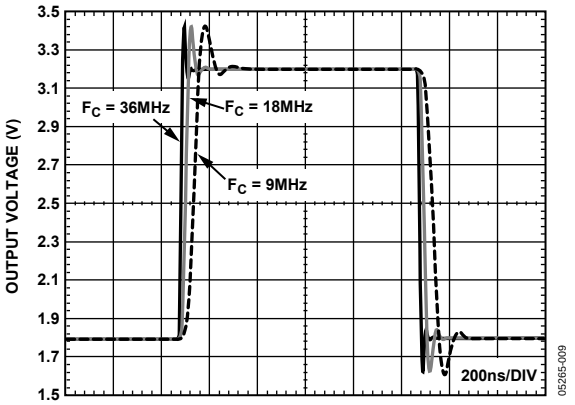

Figure 17. Transient Response vs. Cutoff Frequency (G = ×2)

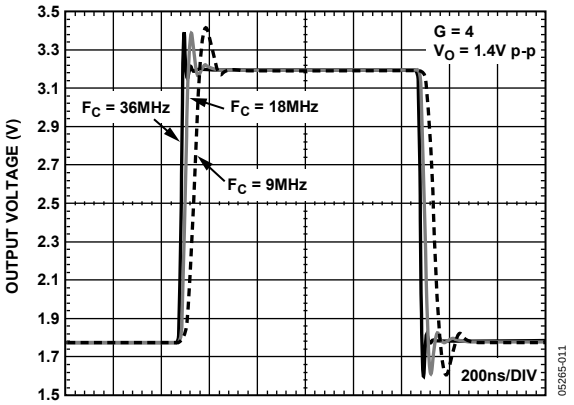

Figure 20. Transient Response vs. Cutoff Frequency (G = ×4)

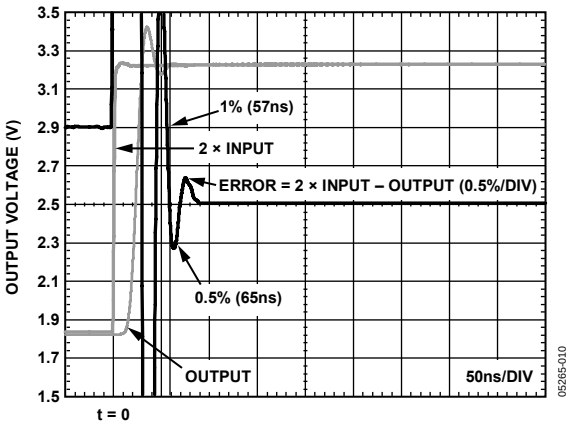

Figure 18. Settling Time

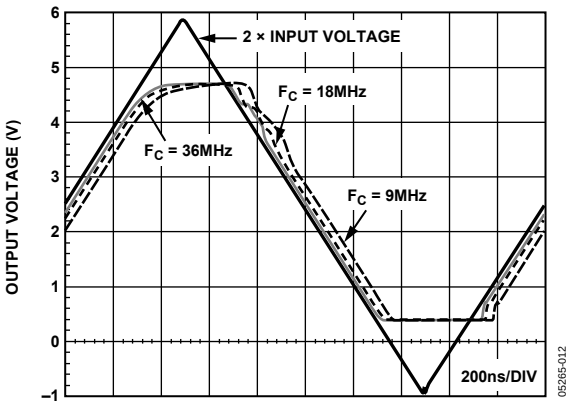

Figure 21. Overdrive Recovery vs. Cutoff Frequency

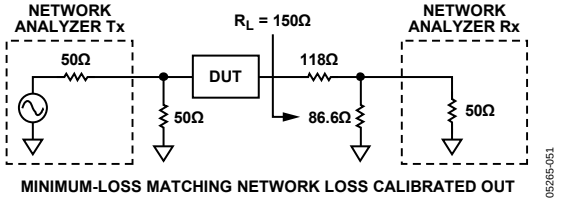

Figure 22. Basic Test Circuit for Swept Frequency Measurements

THEORY OF OPERATION

The ADA4410-6 is an integrated video filtering and driving solution that offers variable bandwidth to meet the needs of several different video formats. There are a total of five filter sections, three for component video and two for Y/C and composite video. The component video filters have switchable bandwidths for standard definition interlaced, progressive, and high definition systems. The Y/C channels have fixed 9 MHz, 3 dB cutoff frequencies and include a summing circuit that feeds an additional buffer for a composite video output. Each filter section has a sixth-order Butterworth response that includes group delay optimization. The group delay variation from 100 kHz to 36 MHz in the 36 MHz section is 8 ns, which produces a fast settling pulse response.

The ADA4410-6 is designed to operate in many different video environments. The supply range is 5 V to 12 V, single supply or dual supply, and requires a relatively low quiescent current of 15 mA per channel. In single-supply applications, the PSRR is greater than 70 dB, providing excellent rejection in systems with supplies that are noisy or under-regulated. In applications where power consumption is critical, the part can be powered down to draw 15 μA by pulling the DISABLE pin to the most positive rail. The ADA4410-6 is also well suited for high encoding frequency applications because it maintains a stop-band attenuation of 50 dB beyond 200 MHz.

The ADA4410-6 is intended to take dc-coupled inputs from an encoder or other ground-referenced video signals. The ADA4410-6 input is high impedance. No minimum or maximum input termination is required, though input terminations above 1 kΩ can degrade crosstalk performance at high frequencies. No clamping is provided internally. For applications where dc restoration is required, dual supplies work best. Using a termination resistance of less than a few hundred ohms to ground on the inputs and suitably adjusting the level shift circuitry provides precise placement of the output voltage.

For single-supply applications (V_{S-} = GND), the input voltage range extends from 100 mV below ground to within 2.0 V of the most positive supply. Each filter section has a 2:1 input multiplexer that includes level-shifting circuitry. The level-shifting circuitry adds a dc component to ground-referenced input signals so that they can be reproduced accurately without the output buffers hitting the negative rail. Because the filters have negative rail input and rail-to-rail output, dc level shifting is generally not necessary, unless accuracy greater than that of the saturated output of the driver is required at the most negative edge. This varies with load but is typically 100 mV in a dc-coupled, single-supply application. If ac coupling is used, the saturated output level is higher because the drivers have to sink more current on the low side. If dual supplies are used (V_{S-} < GND), no level shifting is required. In dual-supply applications, the level shifting circuitry can be used to take a ground-referenced signal and put the blanking level at ground while the sync level is below ground.

The output drivers on the ADA4410-6 have rail-to-rail output capabilities. They provide either 6 dB or 12 dB of gain with respect to the ground pins. Gain is controlled by the external gain select pin. Each output is capable of driving two ac- or dc-coupled 75 Ω source-terminated loads. If a large dc output level is required while driving two loads, ac coupling should be used to limit the power dissipation.

Input mux isolation is primarily a function of the source resistance driving into the ADA4410-6. Higher resistances result in lower isolation over frequency, while a low source resistance, such as 75 Ω, has the best isolation performance. In the SD channels, the isolation variation is most pronounced due to the stray capacitance that exists between the adjacent input pins. The HD input pins are not adjacent; therefore, this effect is less pronounced on the HD channels. See Figure 15 for a performance comparison of the different source resistances feeding the SD inputs.

APPLICATIONS

OVERVIEW

With its high impedance multiplexed inputs and high output drive, the ADA4410-6 is ideally suited to video reconstruction and antialias filtering applications. The high impedance inputs give designers flexibility with regard to how the input signals are terminated. Devices with DAC current source outputs that feed the ADA4410-6 can be loaded in whatever resistance provides the best performance, and devices with voltage outputs can be optimally terminated as well. The ADA4410-6 outputs can each drive up to two source-terminated 75 Ω loads and can therefore directly drive the outputs from set-top boxes, DVD players, and the like without the need for a separate output buffer.

Binary control inputs are provided to select cutoff frequency, throughput gain, and input signal. These inputs are compatible with 3 V and 5 V TTL and CMOS logic levels, referenced to GND. The disable feature is asserted by pulling the DISABLE pin to the positive supply.

The LEVEL1 and LEVEL2 inputs comprise a differential input that controls the dc level at the output pins.

MULTIPLEXER SELECT INPUTS

Selection between the two multiplexer inputs is controlled by the logic signals applied to the MUX_SD and MUX_HD inputs. The MUX_SD input controls the standard definition (SD) inputs, and the MUX_HD input controls the high definition (HD) inputs. Table 6 summarizes the multiplexer operation.

THROUGHPUT GAIN

The throughput gain of the ADA4410-6 signal paths can be ×2 or ×4. Gain selection is controlled by the logic signal applied to the G_SEL pin. Table 6 summarizes how the gain is selected.

Composite Video Path Gain

The composite video signal is produced by passively summing the C and V outputs (see Figure 1), which have been amplified by their respective gain stages. Each signal experiences a 6 dB loss as it passes through the passive summer and is subsequently amplified by 6 dB in the fixed ×2 stage following the summer. The net signal gain through the composite video path is therefore 0 dB, and the resulting composite signal present at the ADA4410-6 output is the sum of Y and C with unity gain. The offset voltage at the composite video output is twice that of the offset on the Y or C outputs because the offsets on the Y and C outputs are the same and appear as a common-mode input to the summer. The voltage between the summing resistors due to the offset voltages is therefore equal to the output offset voltage on the Y and C outputs and appears at the composite video output with a gain of 2 after passing through the fixed ×2 gain stage.

DISABLE

The ADA4410-6 includes a disable feature that can be used to save power when a particular device is not in use. As indicated in the Overview section, the disable feature is asserted by pulling the DISABLE pin to the positive supply. Table 6 summarizes the disable feature operation. The DISABLE pin also functions as a reference level for the logic inputs and, therefore, must be connected to ground when the device is not disabled.

Table 6. Logic Pin Function Description

DISABLE	MUX_HD	MUX_SD	G_SEL
V_{S+} = Disabled	1 = HD Channel 1 Selected	1 = SD Channel 1 Selected	1 = ×4 Gain
GND = Enabled	0 = HD Channel 2 Selected	0 = SD Channel 2 Selected	0 = ×2 Gain

CUTOFF FREQUENCY SELECTION

Four combinations of cutoff frequencies are provided for the HD video signals. The cutoff frequencies were selected to correspond with the most commonly deployed HD scanning systems. Selection between the cutoff frequency combinations is controlled by the logic signals applied to the F_SEL_A and F_SEL_B inputs. Table 7 summarizes cutoff frequency selection.

Table 7. Filter Cutoff Frequency Selection

F_SEL_A	F_SEL_B	Y/G Cutoff	Pb/B Cutoff	Pr/R Cutoff
0	0	36 MHz	36 MHz	36 MHz
0	1	36 MHz	18 MHz	18 MHz
1	0	18 MHz	18 MHz	18 MHz
1	1	9 MHz	9 MHz	9 MHz

OUTPUT DC OFFSET CONTROL

The LEVEL1 and LEVEL2 inputs work as a differential input-referred output offset control. In other words, the output offset voltage of a given channel (with the exception of the CV channel) is equal to the difference in voltage between the LEVEL1 and LEVEL2 inputs multiplied by the overall filter gain. This relationship is expressed in Equation 1.

$$V_{OS}(OUT) = (LEVEL1 - LEVEL2)(G) \quad (1)$$

where:

LEVEL1 and *LEVEL2* are the voltages applied to the respective inputs.

G is throughput gain.

For example, with the G_SEL input set for ×2 gain, setting LEVEL1 to 300 mV and LEVEL2 to 0 V shifts the offset voltages at the ADA4410-6 outputs to 600 mV. This particular setting can be used in most single-supply applications to keep the output swings safely above the negative supply rail.

As previously discussed, the composite video output is developed by passively summing the Y and C outputs that have passed through their respective output gain stages, then multiplying this sum by a factor of two to obtain the output (see Figure 1). The offset of this output is equal to 2× that of the other outputs. Because of this, in many cases, it is necessary to ac-couple the CV output or ensure that it is connected to an input that is ac-coupled. This is generally not an issue because it is common practice to employ ac coupling on composite video inputs.

The maximum differential voltage that can be applied across the LEVEL1 and LEVEL2 inputs is ±500 mV. From a single-ended standpoint, the LEVEL1 and LEVEL2 inputs have the same range as the filter inputs. See the Specifications tables for the limits. The LEVEL1 and LEVEL2 inputs must each be bypassed to GND with a 0.1 µF ceramic capacitor.

In single-supply applications, a positive output offset must be applied to keep the negative-most excursions of the output signals above the specified minimum output swing limit.

Figure 23 and Figure 24 illustrate several ways to use the LEVEL1 and LEVEL2 inputs. Figure 23 shows an example of how to generate fully adjustable LEVEL1 and LEVEL2 voltages from ±5 V and single +5 V supplies. These circuits show a general case, but a more practical approach is to fix one voltage and vary the other. Figure 24 illustrates an effective way to produce a 600 mV output offset voltage in a single-supply application. Although the LEVEL2 input could simply be connected to GND, Figure 24 includes bypassed resistive voltage dividers for each input so that the input levels can be changed, if necessary. Additionally, many in-circuit testers require that I/O signals not be tied directly to the supplies or GND. DNP indicates do not populate.

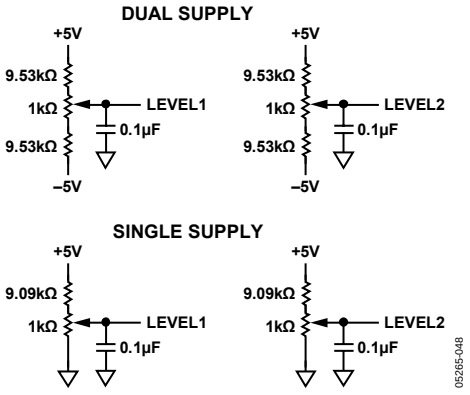

Figure 23. Generating Fully Adjustable Output Offsets

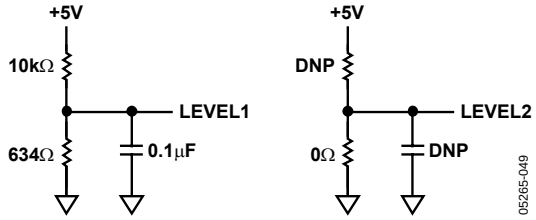

Figure 24. Flexible Circuits to Set the LEVEL1 and LEVEL2 Inputs to Obtain a 600 mV Output Offset on a Single Supply (G = ×2)

INPUT AND OUTPUT COUPLING

Inputs to the ADA4410-6 are normally dc-coupled. Ac coupling the inputs is not recommended; however, if ac coupling is necessary, suitable circuitry must be provided following the ac coupling element to provide proper dc level and bias currents at the ADA4410-6 input stages.

The ADA4410-6 outputs can be either ac- or dc-coupled. As discussed in the Output DC Offset Control section, the CV output offset is different from the other outputs, and the CV output is generally ac-coupled.

When driving single ac-coupled loads in standard 75 Ω video distribution systems, 220 µF coupling capacitors are recommended for use on all but the chrominance signal output. Because the chrominance signal is a narrow-band modulated carrier, it has no low frequency content and can therefore be coupled with a 0.1 µF capacitor.

There are two ac coupling options when driving two loads from one output. One is to simply use the same value capacitor on the second load, while the other is to use a common coupling capacitor that is at least twice the value used for the single load (see Figure 25 and Figure 26).

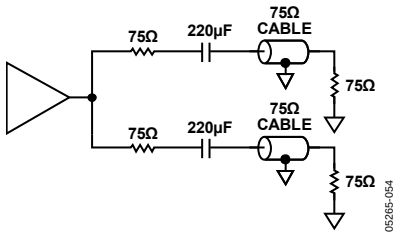

Figure 25. Driving Two AC-Coupled Loads with Two Coupling Capacitors

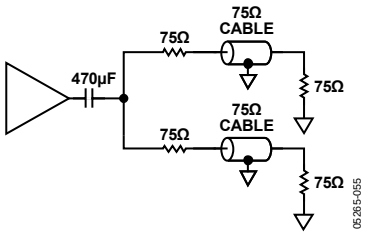

Figure 26. Driving Two AC-Coupled Loads with One Common Coupling Capacitor

PRINTED CIRCUIT BOARD LAYOUT

As with all high speed applications, attention to printed circuit board layout is of paramount importance. Standard high speed layout practices should be adhered to when designing with the ADA4410-6. A solid ground plane is recommended, and surface-mount ceramic power supply decoupling capacitors should be placed as close as possible to the supply pins. All of the ADA4410-6 GND pins should be connected to the ground plane with traces that are as short as possible. Controlled impedance traces of the shortest length possible should be used to connect to the signal I/O pins and should not pass over any voids in the ground plane. A 75 Ω impedance level is typically used in video applications. All signal outputs of the ADA4410-6 should include series termination resistors when driving transmission lines.

When the ADA4410-6 receives its inputs from a device with current outputs, the required load resistor value for the output current is often different from the characteristic impedance of the signal traces. In this case, if the interconnections are sufficiently short (<< 0.1 wavelength), the trace does not have to be terminated in its characteristic impedance. Figure 27 shows an example in which the ADA4410-6 input originates from DACs that require 300 Ω load resistors. Traces of 75 Ω can be used in this instance, provided their lengths are an inch or two at the most. This is easily achieved because the ADA4410-6 and the device feeding it are usually adjacent to each other, and connections can be made that are less than one inch in length.

VIDEO ENCODER RECONSTRUCTION FILTER

The ADA4410-6 is easily applied as a reconstruction filter at the DAC outputs of a video encoder. Figure 27 illustrates how to use the ADA4410-6 in this type of application with an ADV7314 video encoder in a single-supply application with ac-coupled outputs.

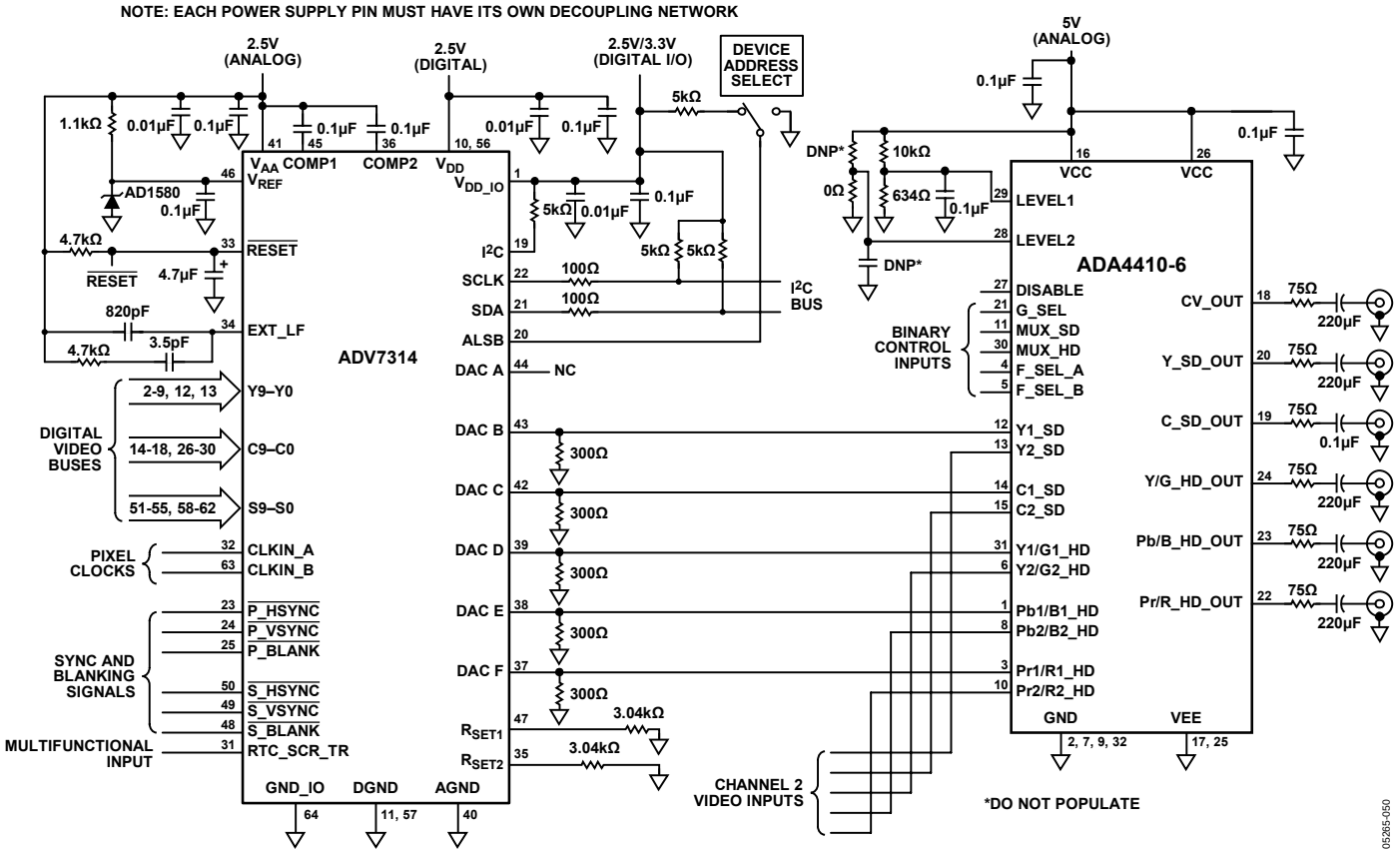

Figure 27. The ADA4410-6 Applied as a Reconstruction Filter Following the ADV7314

OUTLINE DIMENSIONS

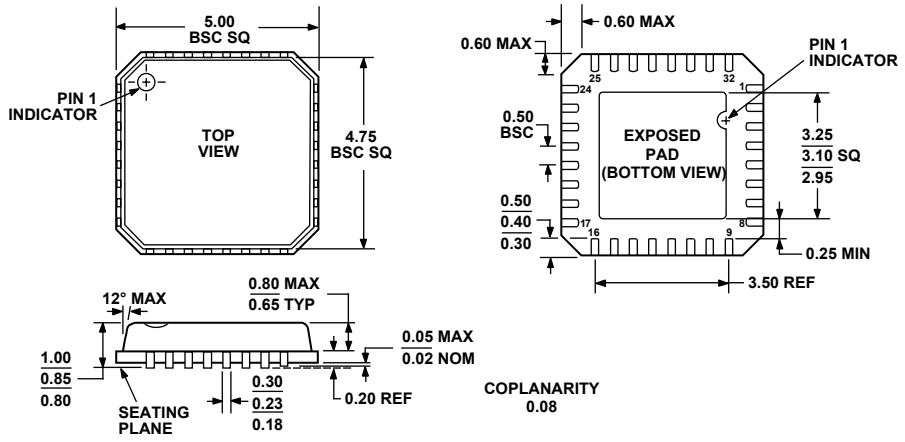

Figure 28. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4410-6ACPZ-R2[1]	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-2	250
ADA4410-6ACPZ-R7[1]	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-2	1,500
ADA4410-6ACPZ-RL[1]	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-32-2	5,000

[1] Z = Pb-free part.

D05265–0–3/06(B)