19-1547; Rev 3; 1/07

Low-Cost, Ultra-Small, 3μA Single-Supply Comparators

General Description

The MAX9075/MAX9077 single/dual comparators are optimized for 3V and 5V single-supply applications. These comparators have a 580ns propagation delay and consume just 3μA per comparator. The combination of low-power, single-supply operation down to 2.1V, and ultra-small footprint makes these devices ideal for all portable applications.

The MAX9075/MAX9077 have a common-mode input voltage range of -0.2V to V_{CC} - 1.2V. Unlike many comparators, there is no differential clamp between the inputs, allowing the differential input voltage range to extend rail-to-rail. All inputs and outputs tolerate a continuous short-circuit fault condition to either rail.

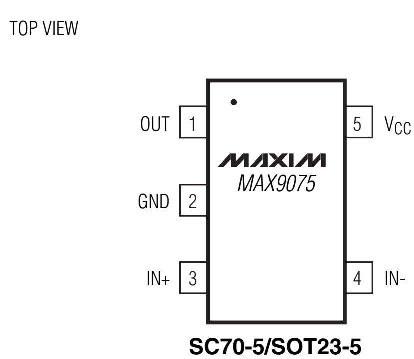
The design of the output stage limits supply-current surges while switching (typical of many other comparators), minimizing power consumption under dynamic conditions. Large internal push-pull output drivers allow rail-to-rail output swing with loads up to 2mA, making these devices ideal for interface with TTL/CMOS logic.

The MAX9075 single comparator is available in 5-pin SC70 and SOT23 packages, while the MAX9077 dual comparator is available in 8-pin SOT23, μMAX®, and SO packages.

Applications

Battery-Powered Systems
Threshold Detectors/Discriminators
Keyless Entry Systems
IR Receivers
Digital Line Receivers

Pin Configurations



Pin Configurations continued at end of data sheet.

Features

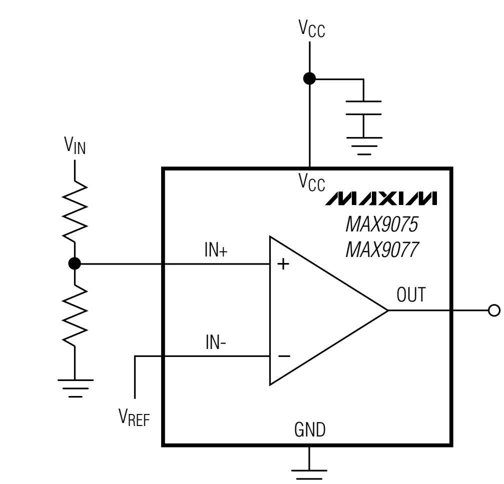
- ♦ **580ns Propagation Delay from Only 3μA**
- ♦ **2.1V to 5.5V Single-Supply Operation**
- ♦ **Ground-Sensing Inputs**
- ♦ **Rail-to-Rail Outputs**
- ♦ **No Output Phase Inversion for Overdriven Inputs**
- ♦ **No Differential Clamp Across Inputs**
- ♦ **Available in Ultra-Small Packages**
  5-Pin SC70 (MAX9075)
  8-Pin SOT23 (MAX9077)

Ordering Information

PART*	PIN-PACKAGE	TOP MARK	PKG CODE
MAX9075EXK-T	5 SC70-5	AAC	X5-1
MAX9075EUK-T	5 SOT23-5	ADLX	U5-1
MAX9077EKA-T	8 SOT23-8	AAAD	K8-2
MAX9077EUA	8 μMAX	—	U8-1
MAX9077ESA	8 SO	—	S8-4

**All devices are specified over the -40°C to +85°C temperature range.*

Typical Operating Circuit



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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Cost, Ultra-Small, 3µA Single-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_{CC} to GND..6V
- All Other Pins to GND...........................-0.3V to (V_{CC} + 0.3V)

Current into Input Pins..±20mA
Duration of Output Short-Circuit to GND or V_{CC}........Continuous
Continuous Power Dissipation (T_A = +70°C)
- 5-Pin SC70 (derate 2.5mW/°C above +70°C)............200mW
- 5-Pin SOT23 (derate 7.1mW/°C above +70°C)..........571mW
- 8-Pin SOT23 (derate 5.3mW/°C above +70°C)..........421mW
- 8-Pin µMAX (derate 4.5mW/°C above +70°C)...........362mW
- 8-Pin SO (derate 5.88mW/°C above +70°C).............471mW

Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{CM} = -0.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

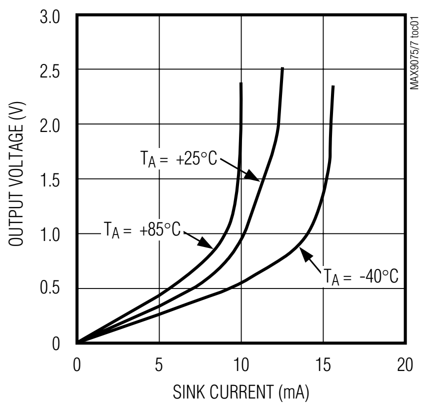
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC}	Inferred from PSRR		2.1		5.5	V
Supply Current per Comparator	I_{CC}	V_{CC} = 5V	T_A = +25°C		3	5.2	µA
			T_A = T_{MIN} to T_{MAX}			6.6	
		V_{CC} = 3V			2.4		
Power-Supply Rejection Ratio	PSRR	2.1V ≤ V_{CC} ≤ 5.5V		54	77		dB
Common-Mode Voltage Range	V_{CMR}	(Note 2)		-0.2		V_{CC} - 1.2	V
Input Offset Voltage	V_{OS}				±1	±8	mV
Input Offset Current	I_{OS}				1		nA
Input Bias Current	I_B	V_{CM} = 0V (Note 3)			-5	-20	nA
Input Capacitance	C_{IN}				3		pF
Common-Mode Rejection Ratio	CMRR	-0.2V ≤ V_{CM} ≤ (V_{CC} - 1.2V)		60	82		dB
OUT_ Output-Voltage High	V_{OH}	I_{SOURCE} = 2mA		V_{CC} - 0.4			V
OUT_ Output-Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Propagation Delay Low to High	t_{PD+}	C_{LOAD} = 10pF, overdrive = 100mV			580		ns
Propagation Delay High to Low	t_{PD-}	C_{LOAD} = 10pF, overdrive = 100mV			250		ns
Rise/Fall Time		C_{LOAD} = 10pF			1.6		ns

Note 1: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: Inferred from CMRR. Either input can be driven to the absolute maximum limit without output inversion, as long as the other input is within the input voltage range.
Note 3: Guaranteed by design.

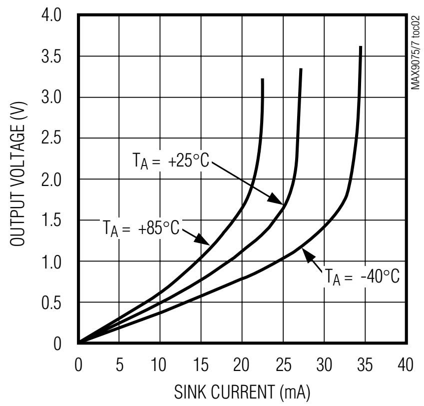
Typical Operating Characteristics

(V_{CC} = 5V, V_{CM} = 0, 100mV overdrive, T_A = +25°C, unless otherwise noted.)

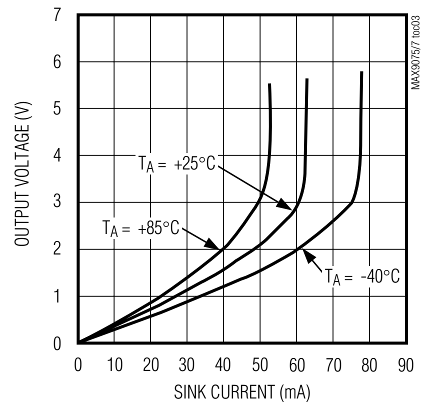
OUTPUT-VOLTAGE LOW vs. SINK CURRENT (V_{CC} = 2.1V)



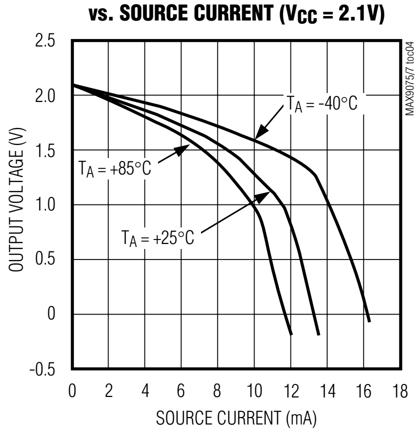
OUTPUT-VOLTAGE LOW vs. SINK CURRENT (V_{CC} = 3V)



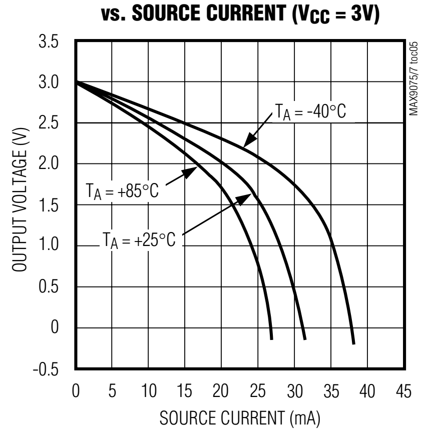
OUTPUT-VOLTAGE LOW vs. SINK CURRENT (V_{CC} = 5V)



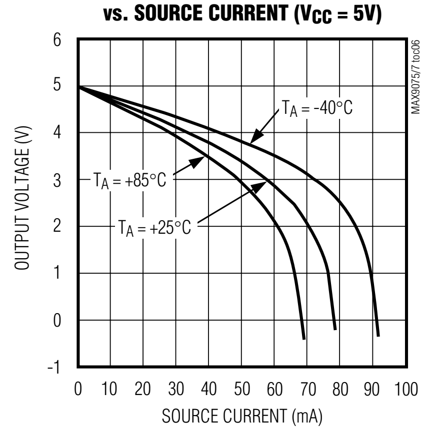
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (V_{CC} = 2.1V)



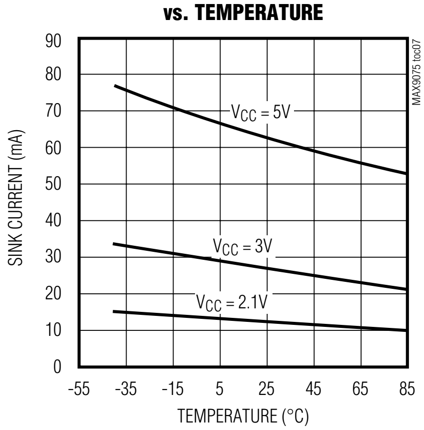
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (V_{CC} = 3V)



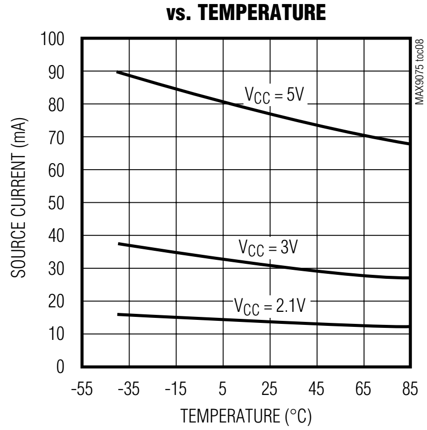
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (V_{CC} = 5V)



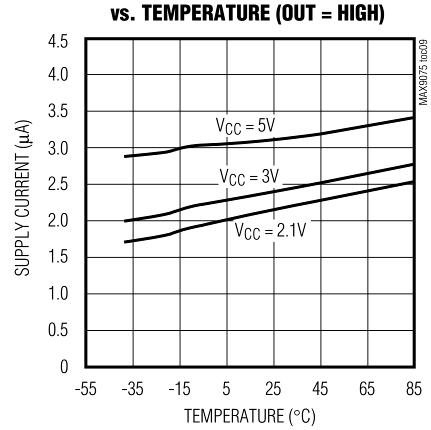
SHORT-CIRCUIT SINK CURRENT vs. TEMPERATURE



SHORT-CIRCUIT SOURCE CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE (OUT = HIGH)

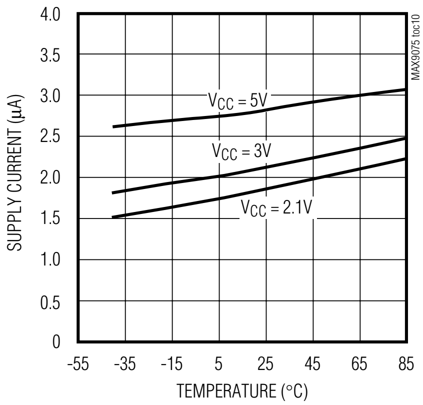


Low-Cost, Ultra-Small, 3µA Single-Supply Comparators

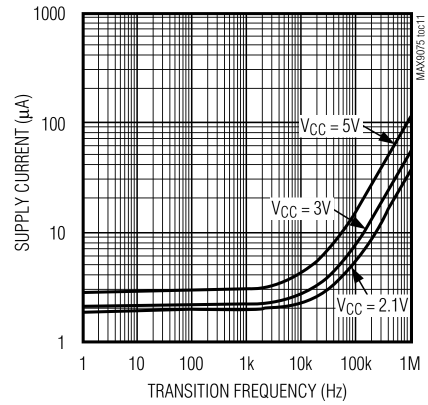
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{CM} = 0, 100mV overdrive, T_A = +25°C, unless otherwise noted.)

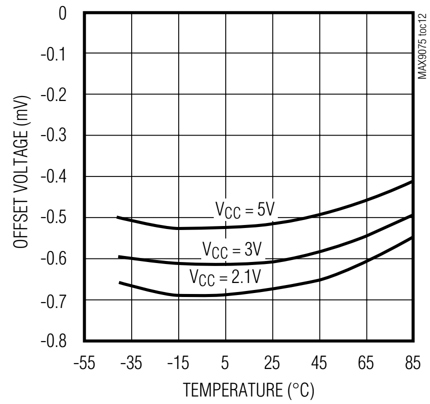
SUPPLY CURRENT vs. TEMPERATURE (OUT = LOW)



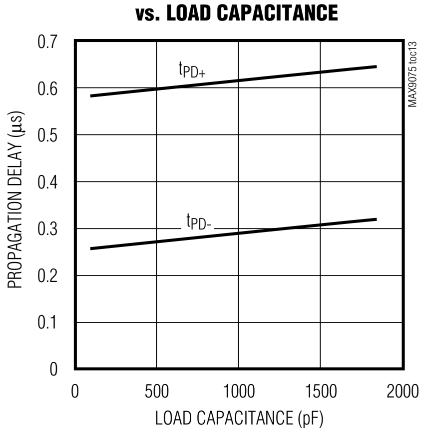
SUPPLY CURRENT vs. OUTPUT TRANSITION FREQUENCY



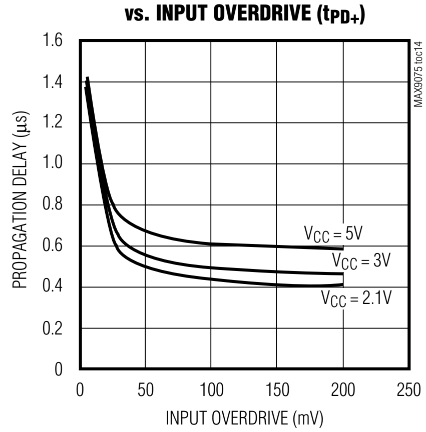
INPUT OFFSET VOLTAGE vs. TEMPERATURE



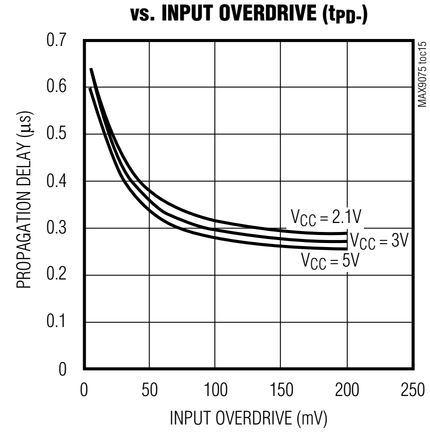
PROPAGATION DELAY vs. LOAD CAPACITANCE



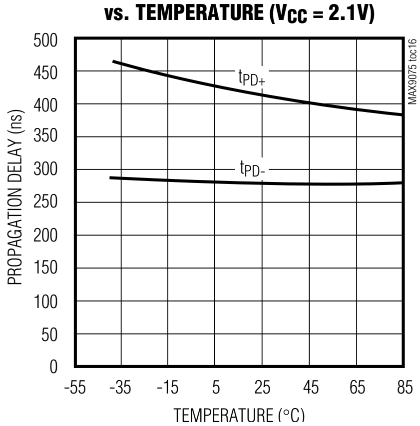
PROPAGATION DELAY vs. INPUT OVERDRIVE (t_{PD+})



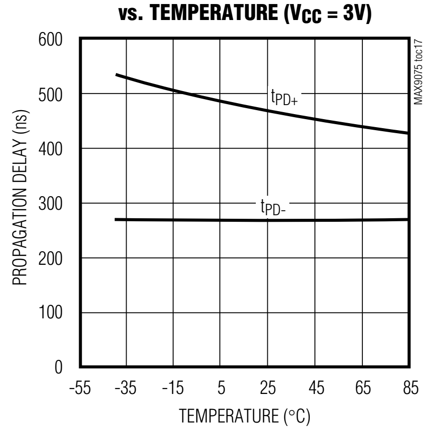
PROPAGATION DELAY vs. INPUT OVERDRIVE (t_{PD-})



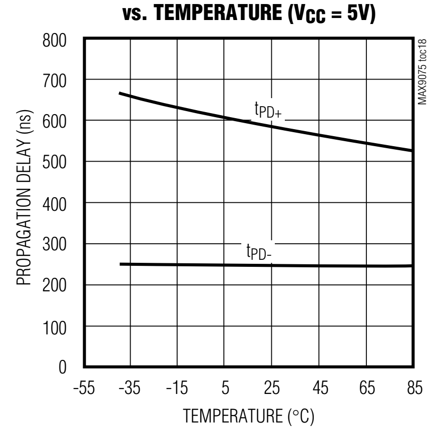
PROPAGATION DELAY vs. TEMPERATURE (V_{CC} = 2.1V)



PROPAGATION DELAY vs. TEMPERATURE (V_{CC} = 3V)



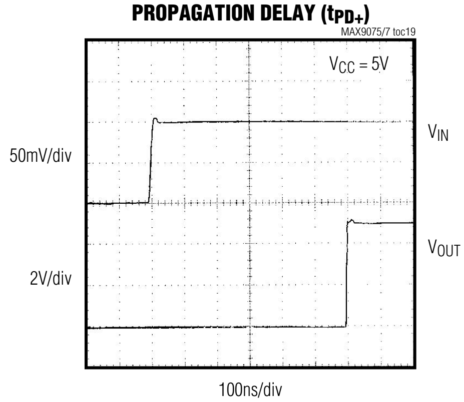
PROPAGATION DELAY vs. TEMPERATURE (V_{CC} = 5V)



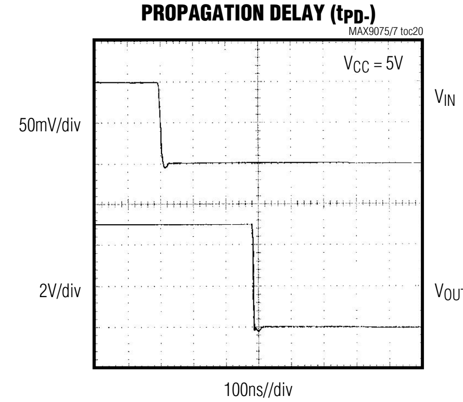
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{CM} = 0, 100mV overdrive, T_A = +25°C, unless otherwise noted.)

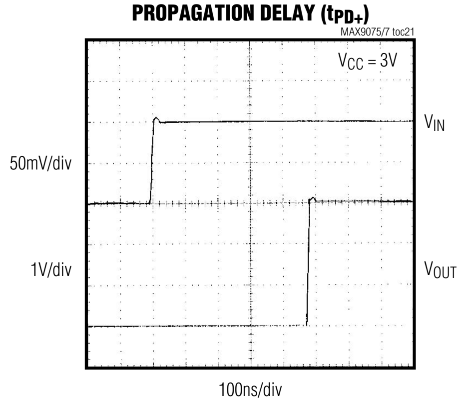
PROPAGATION DELAY (t_{PD+})



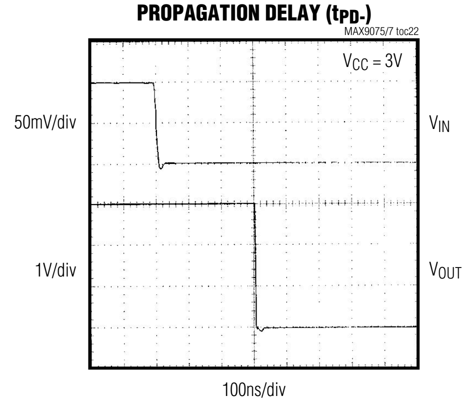
PROPAGATION DELAY (t_{PD-})



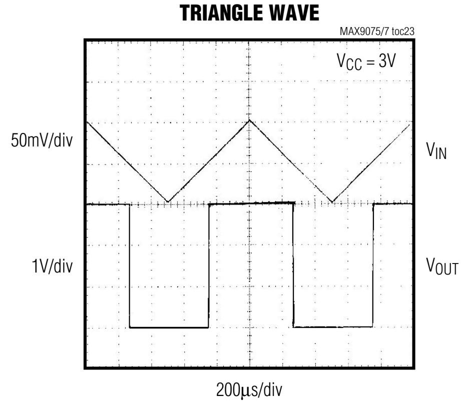
PROPAGATION DELAY (t_{PD+})



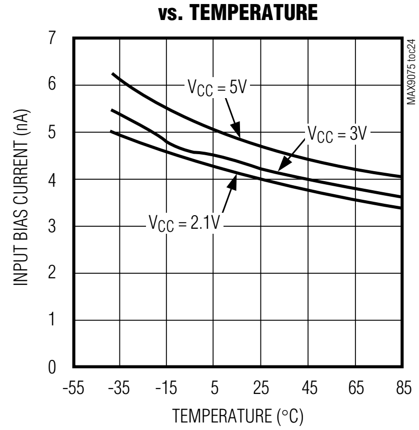
PROPAGATION DELAY (t_{PD-})



TRIANGLE WAVE



INPUT BIAS CURRENT vs. TEMPERATURE



MAX9075/MAX9077

Low-Cost, Ultra-Small, 3µA Single-Supply Comparators

Pin Description

PIN				NAME	FUNCTION
MAX9075		MAX9077			
SOT23	SC70	µMAX/SO	SOT23		
1	1	—	—	OUT	Comparator Output
—	—	1	1	OUTA	Output of Comparator A
2	2	4	2	GND	Ground
3	3	—	—	IN+	Noninverting Comparator Input
—	—	3	4	INA+	Noninverting Input of Comparator A
4	4	—	—	IN-	Inverting Comparator Input
—	—	2	3	INA-	Inverting Input of Comparator A
5	5	8	8	V_{CC}	Positive Supply Voltage
—	—	5	5	INB+	Noninverting Input of Comparator B
—	—	6	6	INB-	Inverting Input of Comparator B
—	—	7	7	OUTB	Output of Comparator B

Detailed Description

The MAX9075/MAX9077 feature a 580ns propagation delay from an ultra-low supply current of only 3µA per comparator. These devices are capable of single-supply operation in the 2.1V to 5.5V range. Large internal output drivers allow rail-to-rail output swing with up to 2mA loads. Both comparators offer a push-pull output that sinks and sources current.

Comparator Output

The MAX9075/MAX9077 are designed to maintain a low-supply current during repeated transitions by limiting the shoot-through current.

Noise Considerations, Comparator Input

The input common-mode voltage range for these devices extends from -0.2V to V_{CC} - 1.2V. Unlike many other comparators, the MAX9075/MAX9077 can operate at any differential input voltage within these limits. Input bias current is typically -5nA if the input voltage is between the supply rails.

Although the comparators have a very high gain, useful gain is limited by noise. The comparator has a wideband peak-to-peak noise of approximately 70µV.

Applications Information

Adding Hysteresis

Hysteresis extends the comparator's noise margin by increasing the upper threshold and decreasing the lower threshold. A voltage divider from the output of the comparator sets the trip voltage. Therefore, the trip voltage is related to the output voltage. Set the hysteresis with three resistors using positive feedback, as shown in Figure 1.

The design procedure is as follows:

1) Choose R3. The leakage current of IN+ may cause a small error; however, the current through R3 can be approximately 500nA and still maintain accuracy. The added supply current due to the circuit at the trip point is V_{CC}/R3; 10MΩ is a good practical value for R3, as this keeps the current well below the supply current of the chip.
2) Choose the hysteresis voltage (V_{HYS}), which is the voltage between the upper and lower thresholds. In this example, choose V_{HYS} = 50mV and assume V_{REF} = 1.2V and V_{CC} = 5V.
3) Calculate R1 as follows:

$$R1 = R3 \times V_{HYS} / V_{CC} = 10M\Omega \times 0.05 / 5 = 100k\Omega$$

4) Choose the threshold voltage for V_{IN} rising (V_{THR}). In this example, choose V_{THR} = 3V.

5) Calculate R2 as follows:

$$R2 = 1 / \{[V_{THR} / (V_{REF} \times R1)] - 1/R1 - 1/R3\} =$$
$$1 / \{[3 / (1.2 \times 100k\Omega)] - 1/100k\Omega - 1/10M\Omega\} = 67.114k\Omega$$

A 1% preferred value is 64.9kΩ.

6) Verify the threshold voltages with these formulas:

V_{IN} rising:

$$V_{THR} = V_{REF} \times R1\ (1/R1 + 1/R2 + 1/R3)$$

V_{IN} falling:

$$V_{THF} = V_{THR} - (R1 \times V_{CC}) / R3$$

7) Check the error due to input bias current (5nA). If the error is too large, reduce R3 and recalculate.

$$V_{TH} = I_B\ (R1 \times R2 \times R3) / (R1 + R2 + R3) = 0.2mV$$

Board Layout and Bypassing

Use 10nF power-supply bypass capacitors. Use 100nF bypass capacitors when supply impedance is high, when supply leads are long, or when excessive noise is expected on the supply lines. Minimize signal trace lengths to reduce stray capacitance. Minimize the capacitive coupling between IN- and OUT. For slow-moving input signals (rise time > 1ms) use a 1nF capacitor between IN+ and IN-.

Chip Information

MAX9075 TRANSISTOR COUNT: 86

MAX9077 TRANSISTOR COUNT: 142

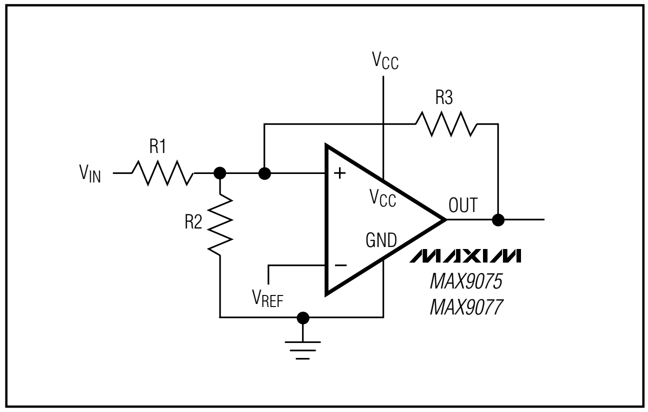
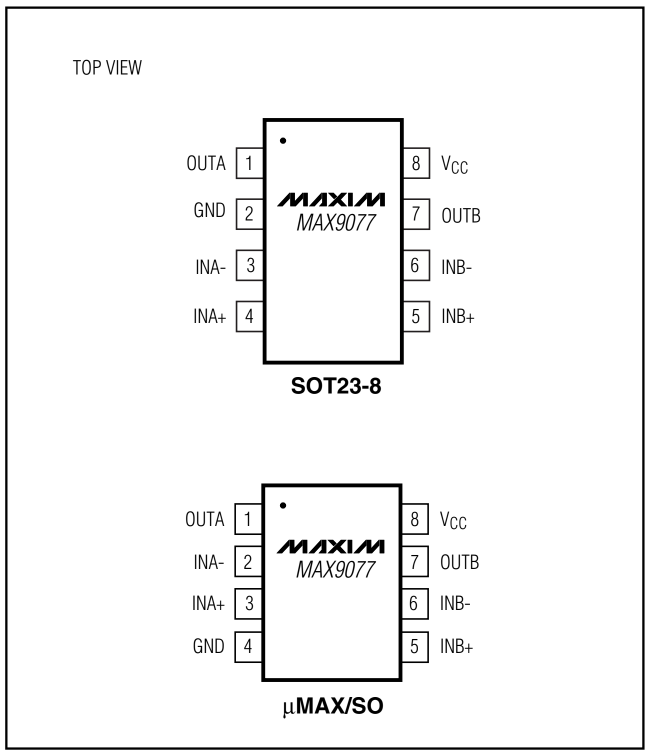


Figure 1. Adding Hysteresis

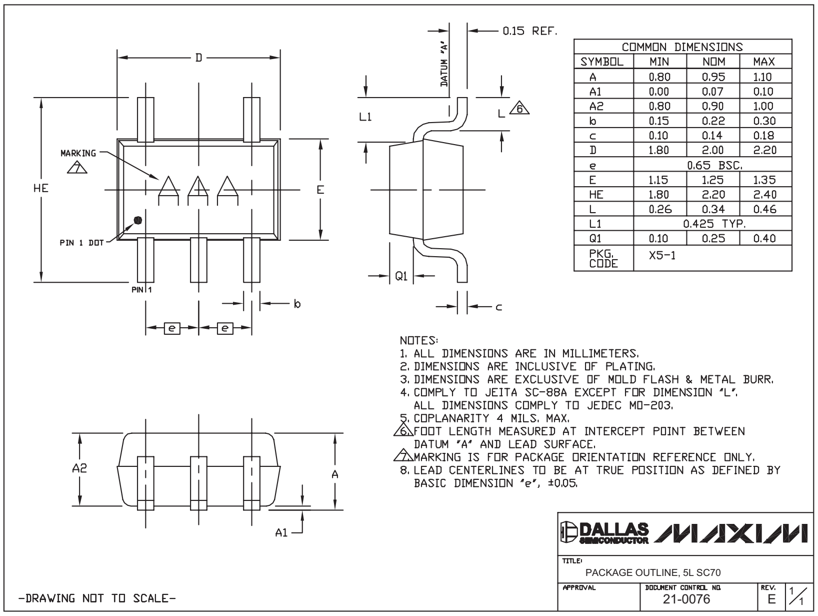
Pin Configurations (continued)



Low-Cost, Ultra-Small, 3µA Single-Supply Comparators

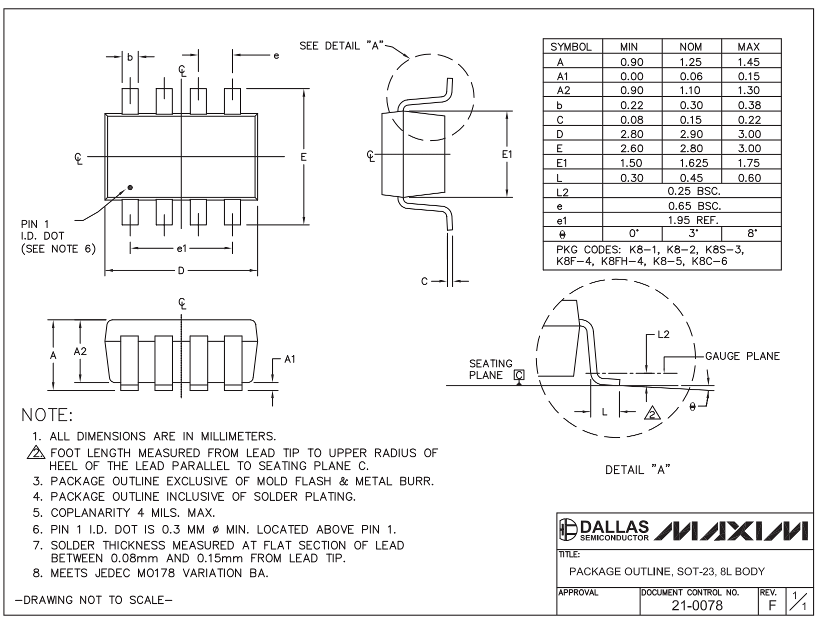
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODE	X5-1		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COMPLY TO JEITA SC-88A EXCEPT FOR DIMENSION "L". ALL DIMENSIONS COMPLY TO JEDEC MO-203.
5. COPLANARITY 4 MILS. MAX.
6. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2	0.25 BSC.		
e	0.65 BSC.		
e1	1.95 REF.		
θ	0°	3°	8°
PKG CODES: K8-1, K8-2, K8S-3, K8F-4, K8FH-4, K8-5, K8C-6			

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.

Revision History

Pages changed at Rev 3: 1–4, 6, 8