

100mW Stereo Headphone Amplifier

- Operating from **Vcc=2V to 5.5V**
- 100mW into 16Ω at 5V
- 38mW into 16Ω at 3.3V
- 11.5mW into 16Ω at 2V
- Switch ON/OFF click reduction circuitry
- High power supply rejection ratio: 85dB at 5V
- High signal-to-noise ratio: 110dB(A) at 5V
- High crosstalk immunity: 100dB (F=1kHz)
- Rail-to-rail input and output
- Unity-gain stable
- Available in **SO-8, MiniSO-8 & DFN8**

Description

The TS482 is a dual audio power amplifier able to drive a 16 or 32Ω stereo headset down to low voltages.

It is delivering up to 100mW per channel (into 16Ω loads) of continuous average power with 0.1% THD+N from a 5V power supply.

The unity gain stable TS482 can be configured by external gain-setting resistors.

Applications

- Stereo headphone amplifier
- Optical storage
- Computer motherboard
- PDA, organizers & notebook computers
- High-end TV, set-top box, DVD players
- Sound cards

Order Codes

Part Number	Temperature Range	Package	Packing	Marking
TS482ID/IDT	-40, +85°C	SO-8	Tube or Tape & Reel	482I
TS482IST		miniSO-8		
TS482IQT		DFN8	Tape & Reel	

1 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input Voltage	-0.3 to $V_{CC} + 0.3$	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient SO8 MiniSO8 DFN8	175 215 70	°C/W
Pd	Power Dissipation (2) SO-8 MiniSO-8 DFN8	0.71 0.58 1.79	W
ESD	Human Body Model (pin to pin)	2	kV
ESD	Machine Model - 220pF - 240pF (pin to pin)	200	V
Latch-up	Latch-up Immunity (all pins)	200	mA
	Lead Temperature (soldering, 10sec)	250	°C
	Lead Temperature (soldering, 10sec) for lead-free	260	°C
	Output Short-Circuit Duration	see note (3)	

1. All voltages values are measured with respect to the ground pin.
2. Pd has been calculated with $T_{amb} = 25^\circ\text{C}$, $T_{junction} = 150^\circ\text{C}$.
3. Attention must be paid to continuous power dissipation. Exposure of the IC to a short circuit on one or two amplifiers simultaneously can cause excessive heating and the destruction of the device.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 5.5	V
R_L	Load Resistor	≥ 16	Ω
C_L	Load Capacitor $R_L = 16 \text{ to } 100\Omega$ $R_L > 100\Omega$	400 100	pF
V_{icm}	Common Mode Input Voltage Range	G_{ND} to V_{CC}	V
R_{thja}	Thermal Resistance Junction to Ambient SO-8 MiniSO-8 DFN8 ⁽¹⁾	150 190 41	°C/W

1. When mounted on a 4-layer PCB.

2 Electrical Characteristics

Table 3. Electrical characteristics when $V_{CC} = +5V$, GND = 0V, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	7.2	mA
V_{IO}	Input Offset Voltage ($V_{ICM} = V_{CC}/2$)		1	5	mV
I_{IB}	Input Bias Current ($V_{ICM} = V_{CC}/2$)		200	500	nA
P_O	Output Power $THD+N = 0.1\% \text{ Max}, F = 1\text{kHz}, R_L = 32\Omega$	60	65		mW
	$THD+N = 1\% \text{ Max}, F = 1\text{kHz}, R_L = 32\Omega$		67.5		
	$THD+N = 0.1\% \text{ Max}, F = 1\text{kHz}, R_L = 16\Omega$		100		
	$THD+N = 1\% \text{ Max}, F = 1\text{kHz}, R_L = 16\Omega$		107		
THD + N	Total Harmonic Distortion + Noise ($A_v=-1$) $R_L = 32\Omega, P_{out} = 60\text{mW}, 20\text{Hz} \leq F \leq 20\text{kHz}$	0.03	0.03		%
	$R_L = 16\Omega, P_{out} = 90\text{mW}, 20\text{Hz} \leq F \leq 20\text{kHz}$				
PSRR	Power Supply Rejection Ratio ($A_v=1$), inputs floating $F = 100\text{Hz}, V_{ripple} = 100\text{mVpp}$		85		dB
I_O	Max Output Current $THD + N < 1\%, R_L = 16\Omega$ connected between out and $V_{CC}/2$	106	120		mA
V_O	Output Swing $V_{OL}: R_L = 32\Omega$	4.45	0.4	0.48	V
	$V_{OH}: R_L = 32\Omega$		4.6		
	$V_{OL}: R_L = 16\Omega$		0.55	0.65	
	$V_{OH}: R_L = 16\Omega$		4.4		
SNR	Signal-to-Noise Ratio (Filter Type A, $A_v=-1$) $R_L = 32\Omega, THD + N < 0.2\%, 20\text{Hz} \leq F \leq 20\text{kHz}$	95	110		dB
Crosstalk	Channel Separation, $R_L = 32\Omega$ $F = 1\text{kHz}$ $F = 20\text{Hz} \text{ to } 20\text{kHz}$		100		dB
	Channel Separation, $R_L = 16\Omega$ $F = 1\text{kHz}$ $F = 20\text{Hz} \text{ to } 20\text{kHz}$		80		
			100		
			80		
C_I	Input Capacitance		1		pF
GBP	Gain Bandwidth Product ($R_L = 32\Omega$)	1.35	2.2		MHz
SR	Slew Rate, Unity Gain Inverting ($R_L = 16\Omega$)	0.45	0.7		V/ μ s

1. Fig. 68 to 79 show dispersion of these parameters.

Table 4. Electrical characteristics when $V_{CC} = +3.3V$, GND = 0V, $T_{amb} = 25^\circ C$ (unless otherwise specified) ⁽¹⁾

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.3	7.2	mA
V_{IO}	Input Offset Voltage ($V_{ICM} = V_{CC}/2$)		1	5	mV
I_{IB}	Input Bias Current ($V_{ICM} = V_{CC}/2$)		200	500	nA
P_O	Output Power $THD+N = 0.1\% \text{ Max}, F = 1\text{kHz}, R_L = 32\Omega$ $THD+N = 1\% \text{ Max}, F = 1\text{kHz}, R_L = 32\Omega$ $THD+N = 0.1\% \text{ Max}, F = 1\text{kHz}, R_L = 16\Omega$ $THD+N = 1\% \text{ Max}, F = 1\text{kHz}, R_L = 16\Omega$	23 36	27 28 38 42		mW
THD + N	Total Harmonic Distortion + Noise ($A_v=-1$) ⁽¹⁾ $R_L = 32\Omega, P_{out} = 16\text{mW}, 20\text{Hz} \leq F \leq 20\text{kHz}$ $R_L = 16\Omega, P_{out} = 35\text{mW}, 20\text{Hz} \leq F \leq 20\text{kHz}$		0.03 0.03		%
PSRR	Power Supply Rejection Ratio ($A_v=1$), inputs floating $F = 100\text{Hz}, V_{ripple} = 100\text{mVpp}$		80		dB
I_O	Max Output Current $THD + N < 1\%, R_L = 16\Omega$ connected between out and $V_{CC}/2$	64	75		mA
V_O	Output Swing $V_{OL}: R_L = 32\Omega$ $V_{OH}: R_L = 32\Omega$ $V_{OL}: R_L = 16\Omega$ $V_{OH}: R_L = 16\Omega$	2.85 2.68	0.3 3 0.45 2.85	0.38 0.52	V
SNR	Signal-to-Noise Ratio (Filter Type A, $A_v=-1$) $R_L = 32\Omega, THD + N < 0.2\%, 20\text{Hz} \leq F \leq 20\text{kHz}$	92	107		dB
Crosstalk	Channel Separation, $R_L = 32\Omega$ $F = 1\text{kHz}$ $F = 20\text{Hz} \text{ to } 20\text{kHz}$ Channel Separation, $R_L = 16\Omega$ $F = 1\text{kHz}$ $F = 20\text{Hz} \text{ to } 20\text{kHz}$		100 80 100 80		dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwidth Product ($R_L = 32\Omega$)	1.2	2		MHz
SR	Slew Rate, Unity Gain Inverting ($R_L = 16\Omega$)	0.45	0.7		V/ μ s

1. Fig. 68 to 79 show dispersion of these parameters.

1. All electrical values are guaranteed with correlation measurements at 2V and 5V.

Table 5. Electrical characteristics when $V_{CC} = +2.5V$, GND = 0V, $T_{amb} = 25^\circ C$ (unless otherwise specified)⁽²⁾

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.1	7.2	mA
V_{IO}	Input Offset Voltage ($V_{ICM} = V_{CC}/2$)		1	5	mV
I_{IB}	Input Bias Current ($V_{ICM} = V_{CC}/2$)		200	500	nA
P_O	Output Power $THD+N = 0.1\% \text{ Max}, F = 1\text{kHz}, R_L = 32\Omega$ $THD+N = 1\% \text{ Max}, F = 1\text{kHz}, R_L = 32\Omega$ $THD+N = 0.1\% \text{ Max}, F = 1\text{kHz}, R_L = 16\Omega$ $THD+N = 1\% \text{ Max}, F = 1\text{kHz}, R_L = 16\Omega$	12.5 17.5	13.5 14.5 20.5 22		mW
THD + N	Total Harmonic Distortion + Noise ($A_v=-1$) ⁽¹⁾ $R_L = 32\Omega, P_{out} = 10\text{mW}, 20\text{Hz} \leq F \leq 20\text{kHz}$ $R_L = 16\Omega, P_{out} = 16\text{mW}, 20\text{Hz} \leq F \leq 20\text{kHz}$		0.03 0.03		%
PSRR	Power Supply Rejection Ratio ($A_v=1$), inputs floating $F = 100\text{Hz}, V_{ripple} = 100\text{mVpp}$		75		dB
I_O	Max Output Current $THD + N < 1\%, R_L = 16\Omega$ connected between out and $V_{CC}/2$	45	56		mA
V_O	Output Swing $V_{OL}: R_L = 32\Omega$ $V_{OH}: R_L = 32\Omega$ $V_{OL}: R_L = 16\Omega$ $V_{OH}: R_L = 16\Omega$	2.14 1.97	0.25 2.25 0.35 2.15	0.325 0.45	V
SNR	Signal-to-Noise Ratio (Filter Type A, $A_v=-1$) $R_L = 32\Omega, THD + N < 0.2\%, 20\text{Hz} \leq F \leq 20\text{kHz}$	89	102		dB
Crosstalk	Channel Separation, $R_L = 32\Omega$ $F = 1\text{kHz}$ $F = 20\text{Hz} \text{ to } 20\text{kHz}$ Channel Separation, $R_L = 16\Omega$ $F = 1\text{kHz}$ $F = 20\text{Hz} \text{ to } 20\text{kHz}$		100 80 100 80		dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwidth Product ($R_L = 32\Omega$)	1.2	2		MHz
SR	Slew Rate, Unity Gain Inverting ($R_L = 16\Omega$)	0.45	0.7		V/ μ s

1. Fig. 68 to 79 show dispersion of these parameters.

2. All electrical values are guaranteed with correlation measurements at 2V and 5V.

Table 6. Electrical characteristics when $V_{CC} = +2V$, GND = 0V, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5	7.2	mA
V_{IO}	Input Offset Voltage ($V_{ICM} = V_{CC}/2$)		1	5	mV
I_{IB}	Input Bias Current ($V_{ICM} = V_{CC}/2$)		200	500	nA
P_O	Output Power $THD+N = 0.1\% \text{ Max}, F = 1\text{kHz}, R_L = 32\Omega$ $THD+N = 1\% \text{ Max}, F = 1\text{kHz}, R_L = 32\Omega$ $THD+N = 0.1\% \text{ Max}, F = 1\text{kHz}, R_L = 16\Omega$ $THD+N = 1\% \text{ Max}, F = 1\text{kHz}, R_L = 16\Omega$	7 9.5	8 9 11.5 13		mW
THD + N	Total Harmonic Distortion + Noise ($A_v=-1$) $R_L = 32\Omega, P_{out} = 6.5\text{mW}, 20\text{Hz} \leq F \leq 20\text{kHz}$ $R_L = 16\Omega, P_{out} = 8\text{mW}, 20\text{Hz} \leq F \leq 20\text{kHz}$		0.02 0.025		%
PSRR	Power Supply Rejection Ratio ($A_v=1$), inputs floating $F = 100\text{Hz}, V_{ripple} = 100\text{mVpp}$		75		dB
I_O	Max Output Current $THD + N < 1\%, R_L = 16\Omega$ connected between out and $V_{CC}/2$	33	41.5		mA
V_O	Output Swing $V_{OL}: R_L = 32\Omega$ $V_{OH}: R_L = 32\Omega$ $V_{OL}: R_L = 16\Omega$ $V_{OH}: R_L = 16\Omega$		1.67 1.53	0.24 1.73 0.33 0.41	V
SNR	Signal-to-Noise Ratio (Filter Type A, $A_v=-1$) $R_L = 32\Omega, THD + N < 0.2\%, 20\text{Hz} \leq F \leq 20\text{kHz}$	88	101		dB
Crosstalk	Channel Separation, $R_L = 32\Omega$ $F = 1\text{kHz}$ $F = 20\text{Hz} \text{ to } 20\text{kHz}$ Channel Separation, $R_L = 16\Omega$ $F = 1\text{kHz}$ $F = 20\text{Hz} \text{ to } 20\text{kHz}$			100 80 100 80	dB
C_I	Input Capacitance		1		pF
GBP	Gain Bandwidth Product ($R_L = 32\Omega$)	1.2	2		MHz
SR	Slew Rate, Unity Gain Inverting ($R_L = 16\Omega$)	0.42	0.65		V/ μ s

1. Fig. 68 to 79 show dispersion of these parameters.

Table 7. Components description

Components	Functional Description
Rin	Inverting input resistor which sets the closed loop gain in conjunction with Rfeed. This resistor also forms a high pass filter with Cin ($f_c = 1 / (2 \times \pi \times R_{in} \times C_{in})$)
Cin	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
Rfeed	Feed back resistor which sets the closed loop gain in conjunction with Rin
Cs	Supply Bypass capacitor which provides power supply filtering
Cb	Bypass capacitor which provides half supply filtering
Cout	Output coupling capacitor which blocks the DC voltage at the load input terminal This capacitor also forms a high pass filter with RL ($f_c = 1 / (2 \times \pi \times R_{load} \times C_{out})$)
Rpol	These 2 resistors form a voltage divider which provide a DC biasing voltage (Vcc/2) for the 2 amplifiers.
Av	Closed loop gain = -Rfeed / Rin

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Figure 1. Open loop gain and phase vs. frequency response

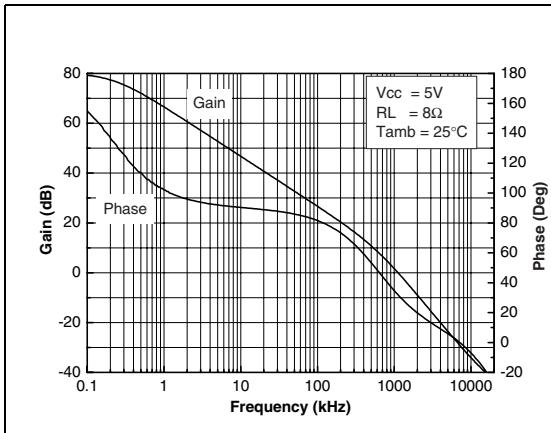


Figure 2. Open loop gain and phase vs. frequency response

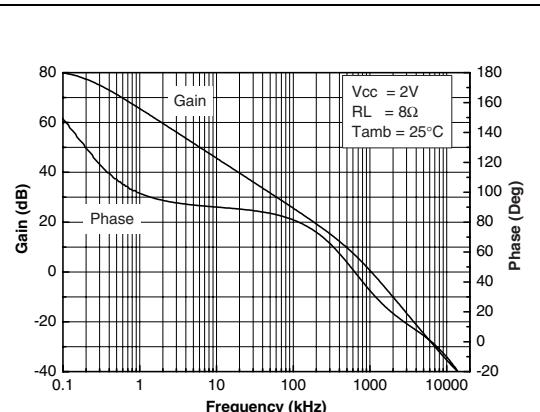


Figure 3. Open loop gain and phase vs. frequency response

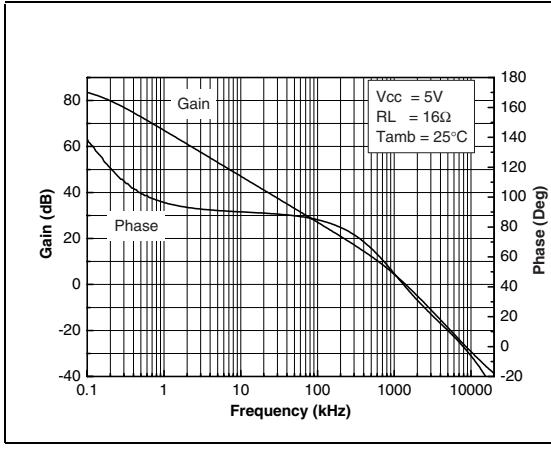


Figure 4. Open loop gain and phase vs. frequency response

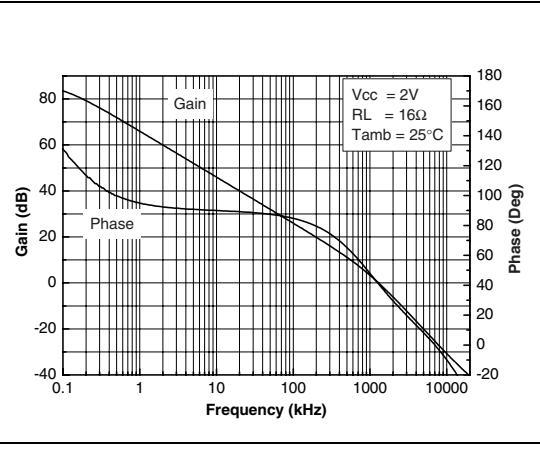


Figure 5. Open loop gain and phase vs. frequency response

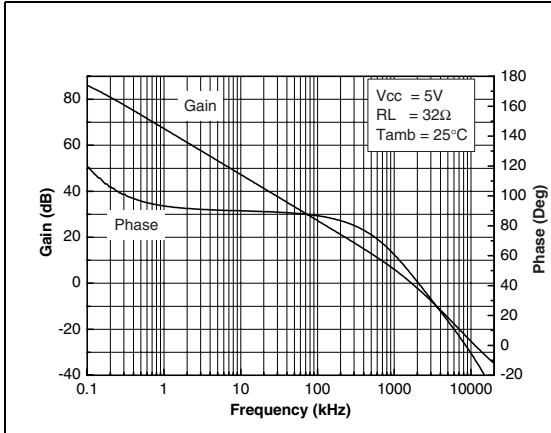


Figure 6. Open loop gain and phase vs. frequency response

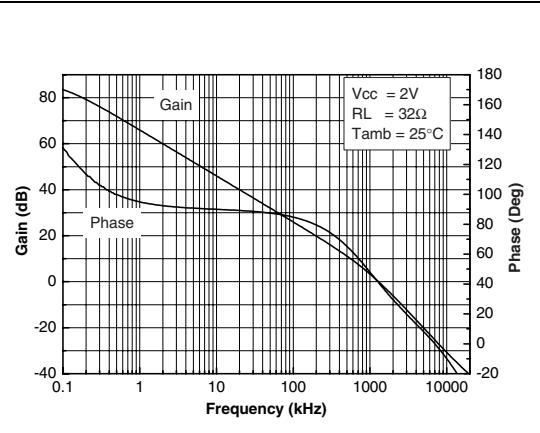


Figure 7. Open loop gain and phase vs. frequency response

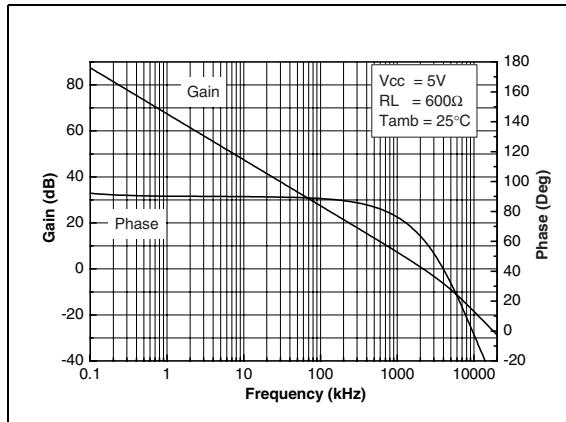


Figure 8. Open loop gain and phase vs. frequency response

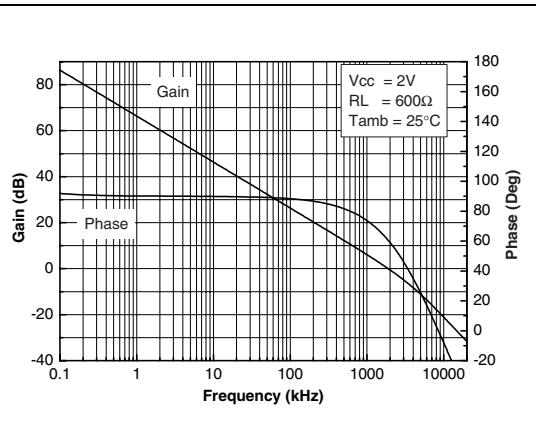


Figure 9. Open loop gain and phase vs. frequency response

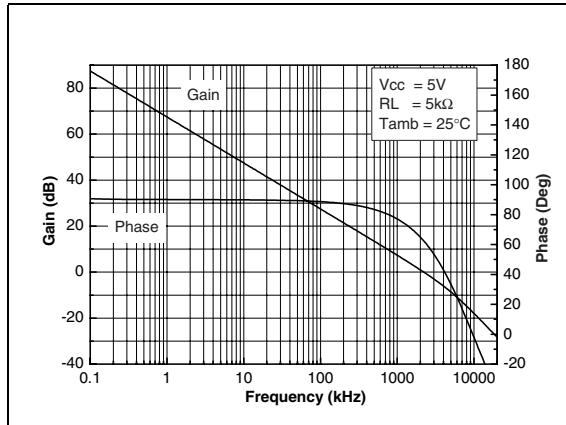


Figure 10. Open loop gain and phase vs. frequency response

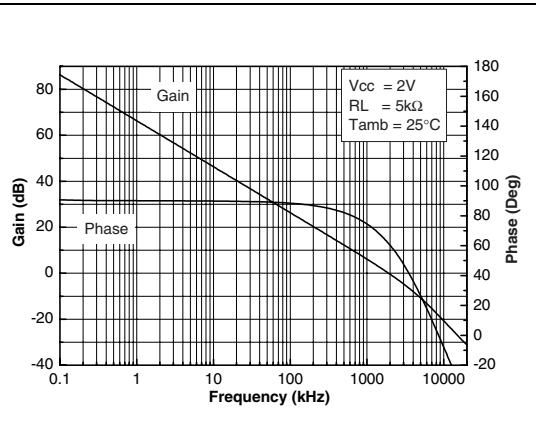


Figure 11. Phase margin vs. power supply voltage **Figure 12. Phase margin vs. power supply voltage**

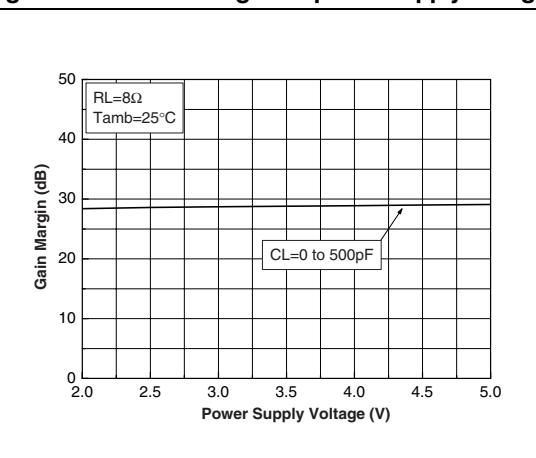
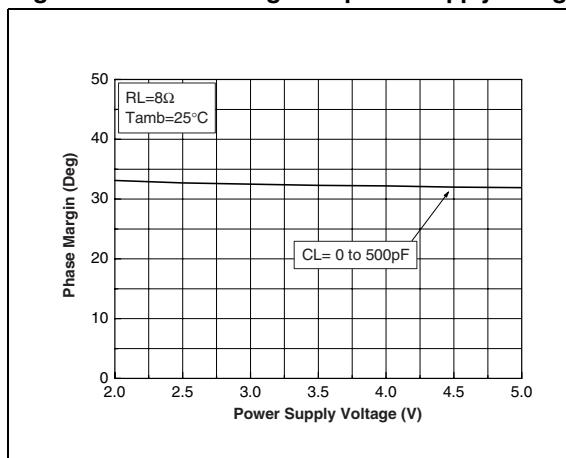


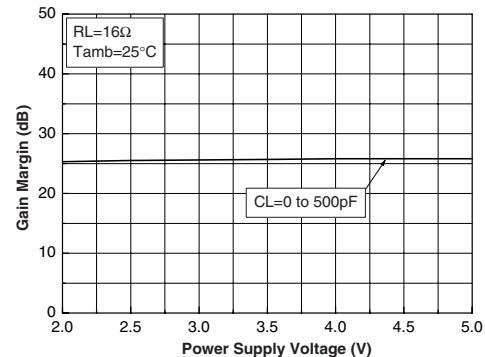
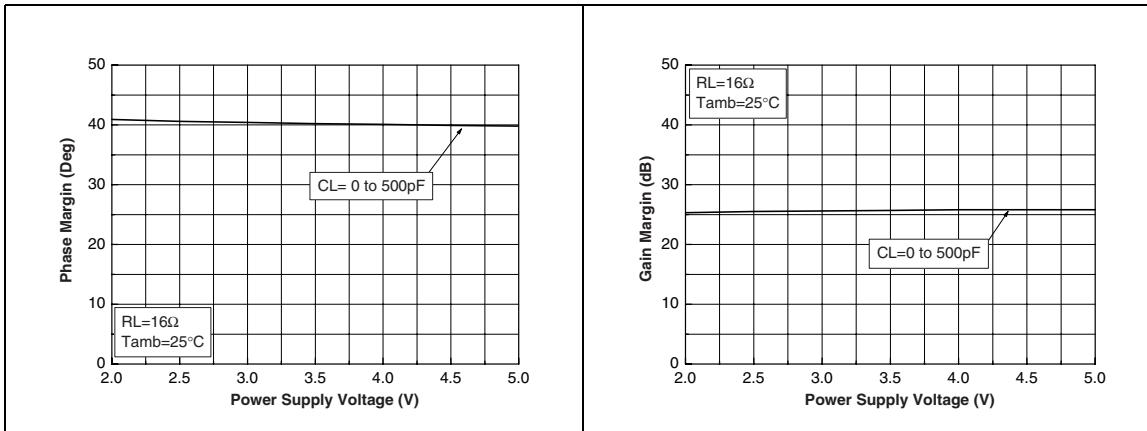
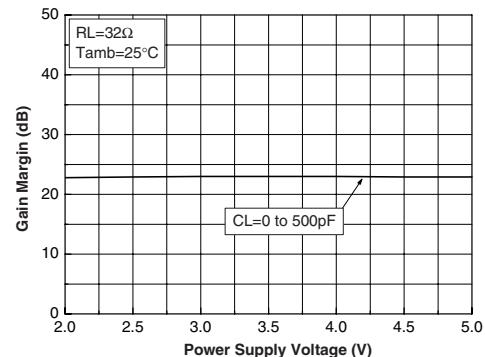
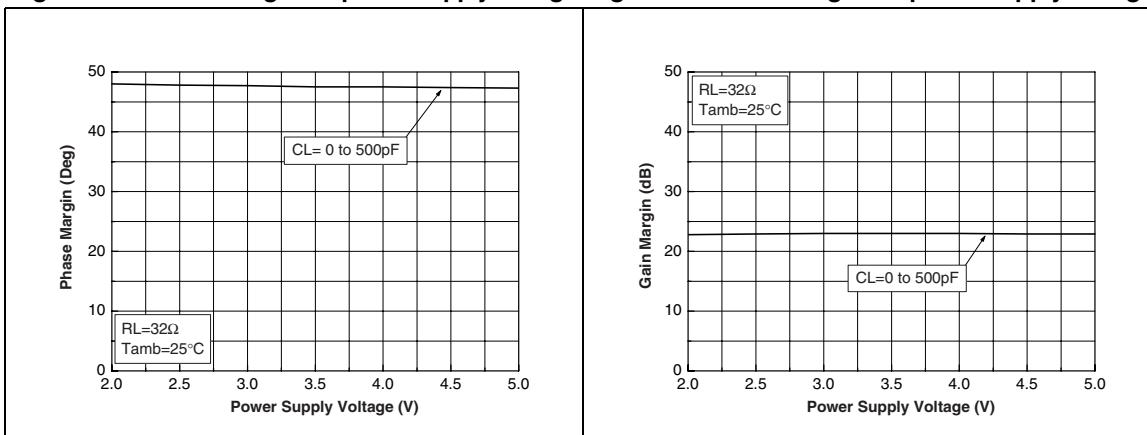
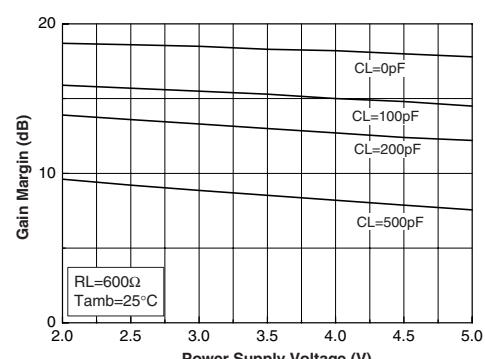
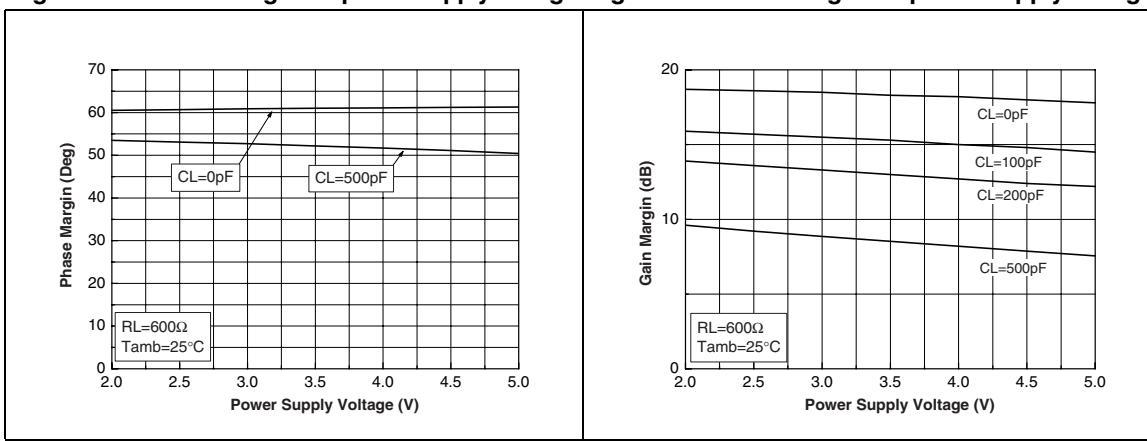
Figure 13. Phase margin vs. power supply voltage**Figure 15. Phase margin vs. power supply voltage****Figure 17. Phase margin vs. power supply voltage**

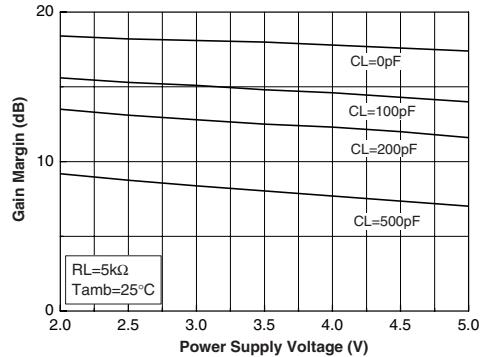
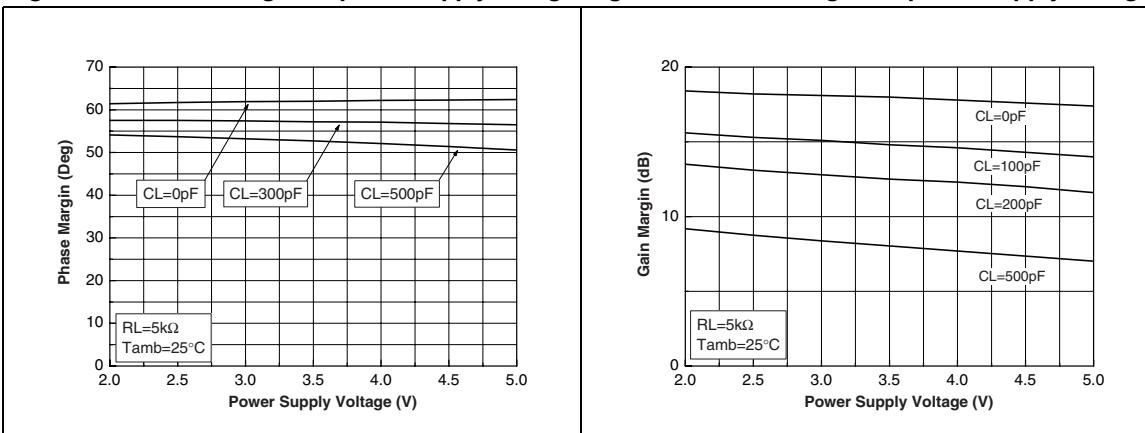
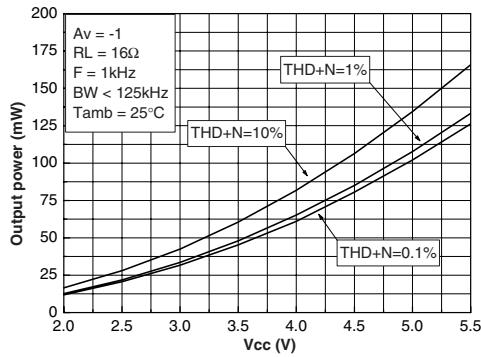
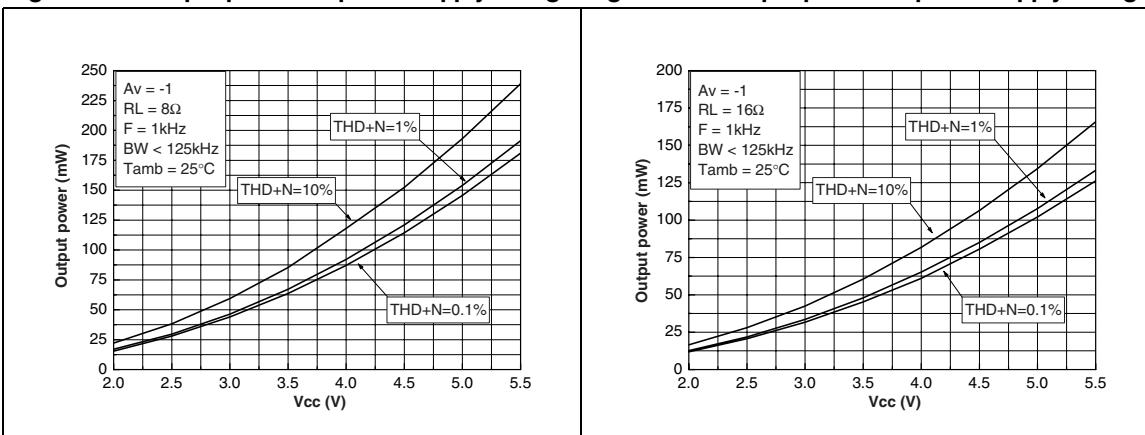
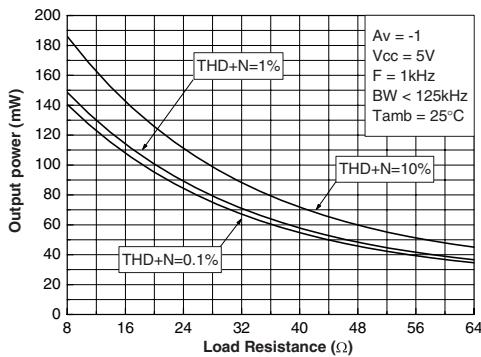
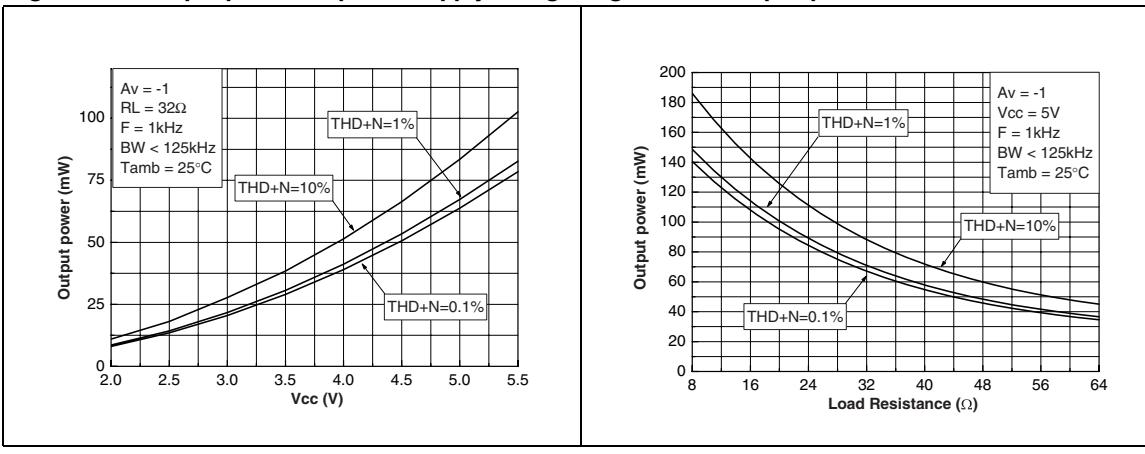
Figure 19. Phase margin vs. power supply voltage**Figure 21. Output power vs. power supply voltage****Figure 23. Output power vs. power supply voltage**

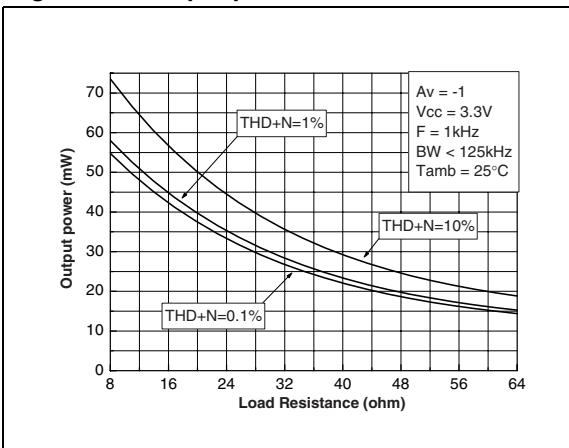
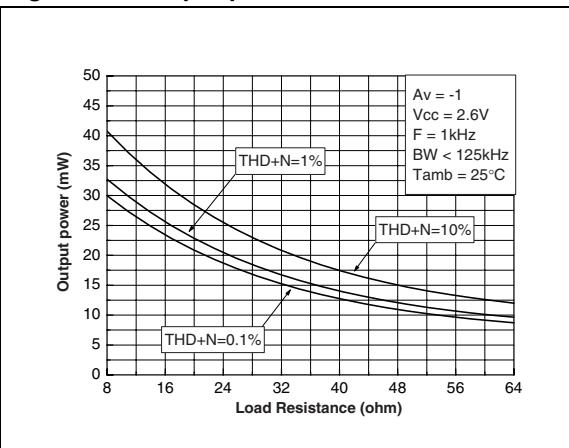
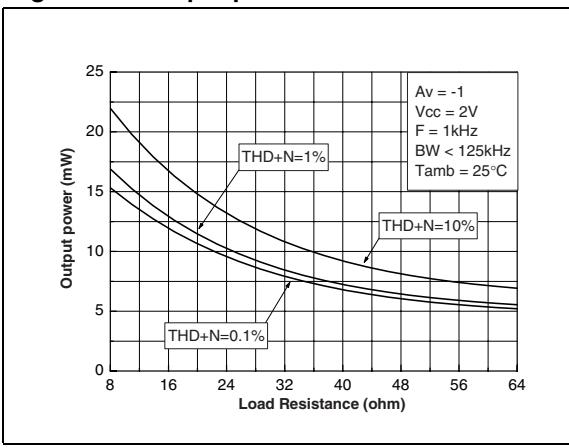
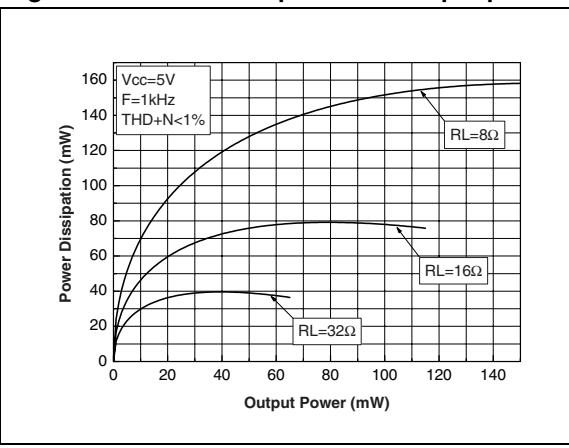
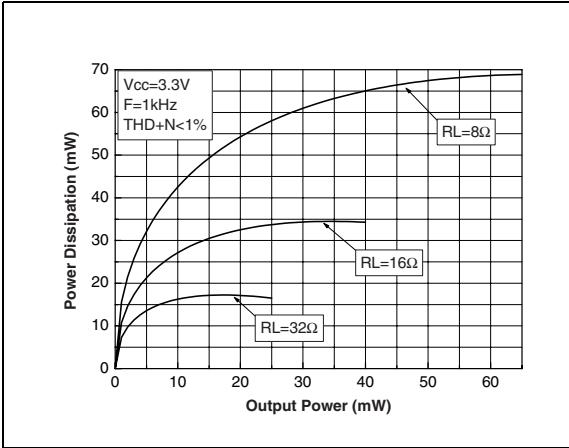
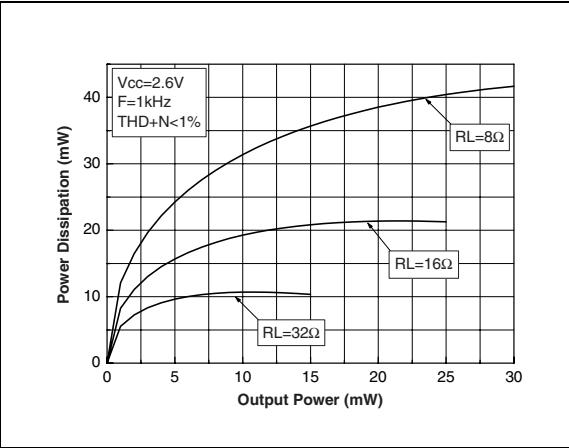
Figure 25. Output power vs. load resistance**Figure 26. Output power vs. load resistance****Figure 27. Output power vs. load resistance****Figure 28. Power dissipation vs. output power****Figure 29. Power dissipation vs. output power****Figure 30. Power dissipation vs. output power**

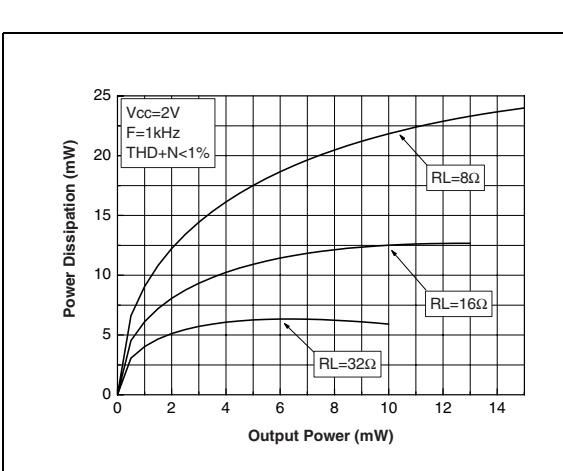
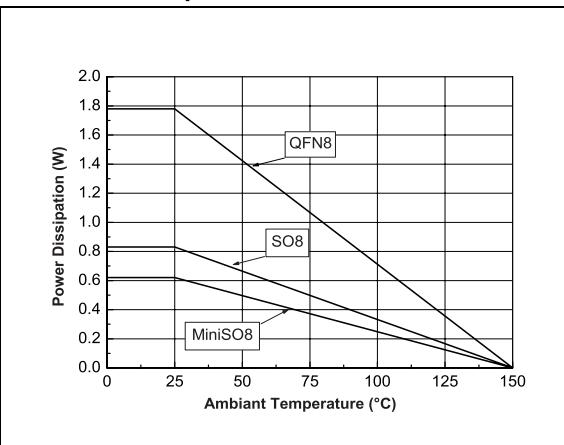
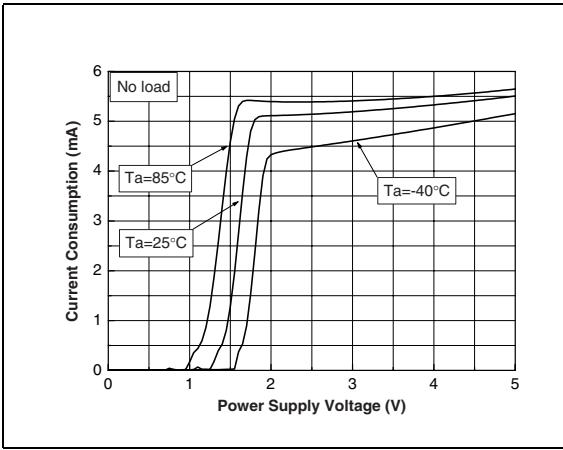
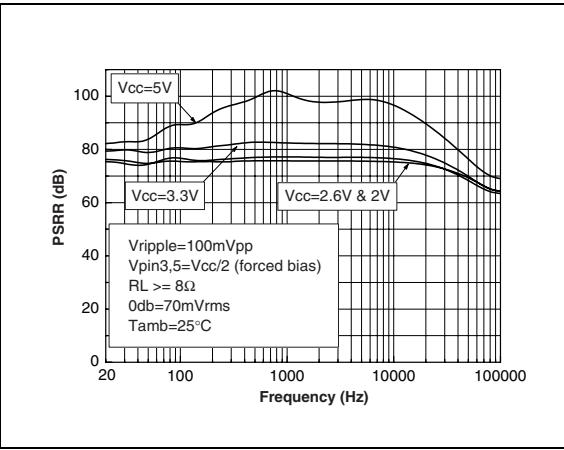
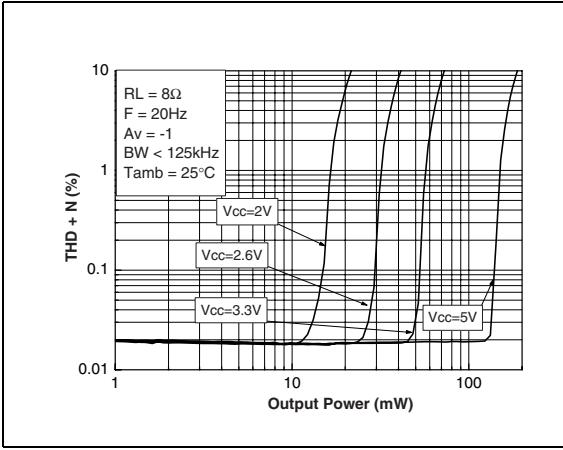
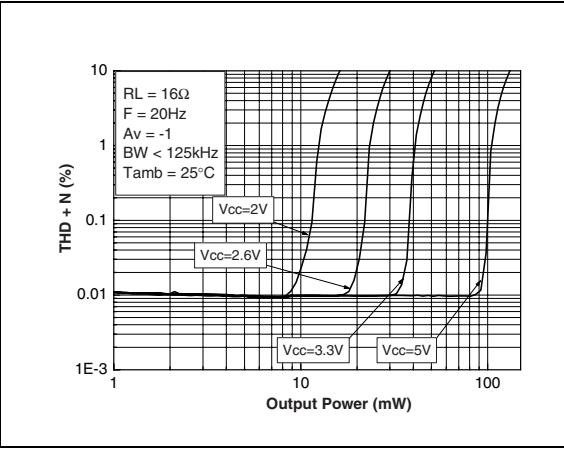
Figure 31. Power dissipation vs. output power**Figure 32. Power derating vs. ambient temperature****Figure 33. Current consumption vs. power supply voltage****Figure 34. Power supply rejection ratio vs. frequency****Figure 35. THD + N vs. output power****Figure 36. THD + N vs. output power**

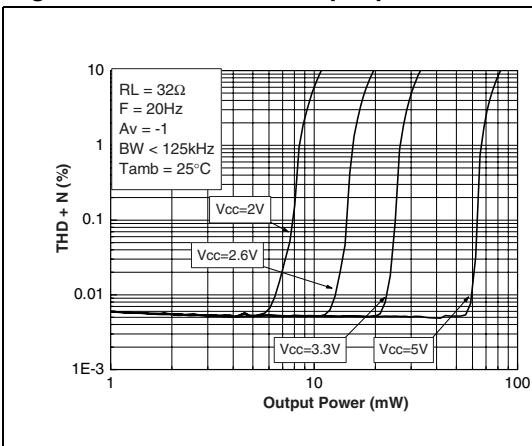
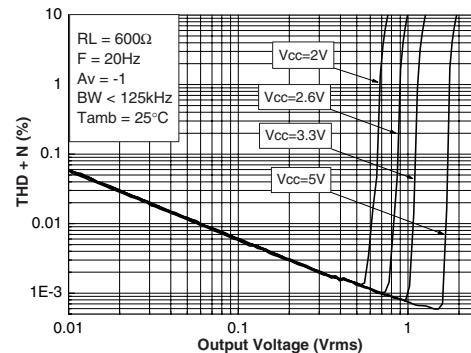
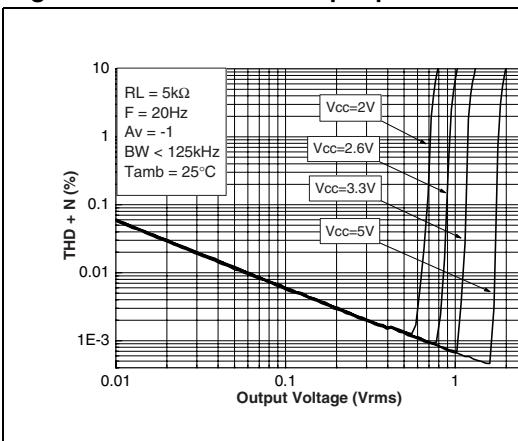
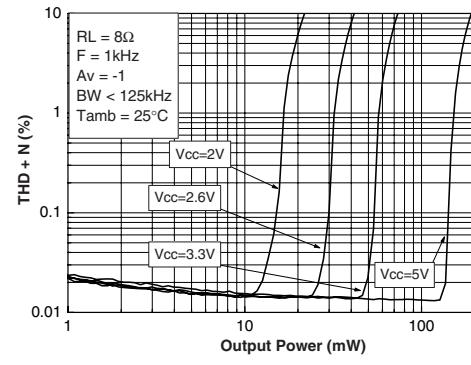
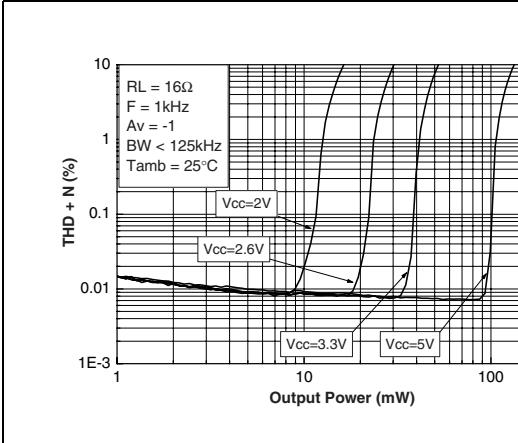
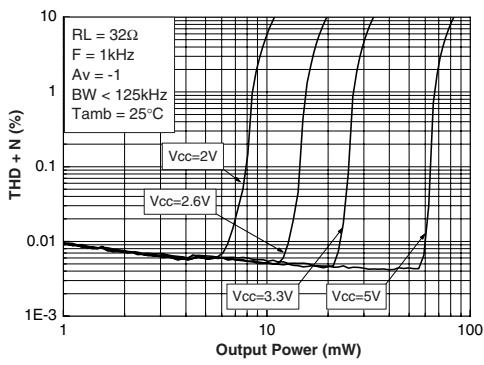
Figure 37. THD + N vs. output power**Figure 38. THD + N vs. output power****Figure 39. THD + N vs. output power****Figure 40. THD + N vs. output power****Figure 41. THD + N vs. output power****Figure 42. THD + N vs. output power**

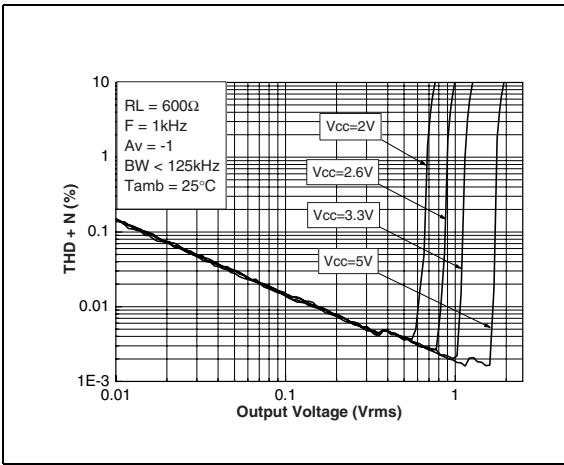
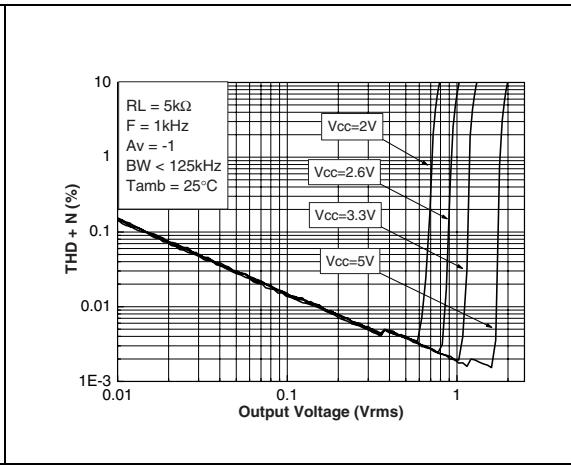
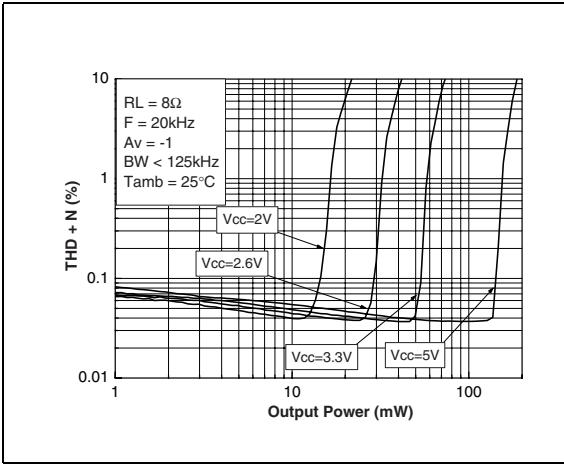
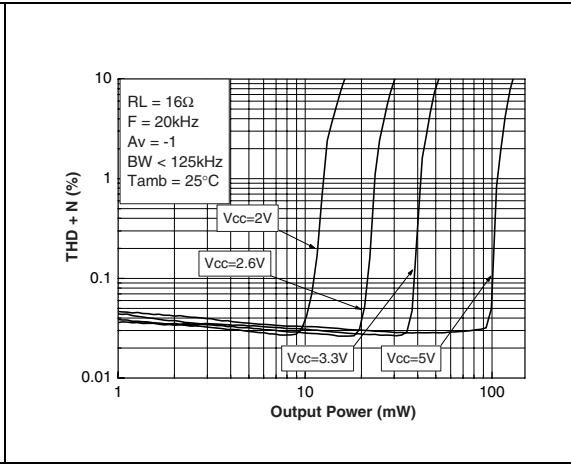
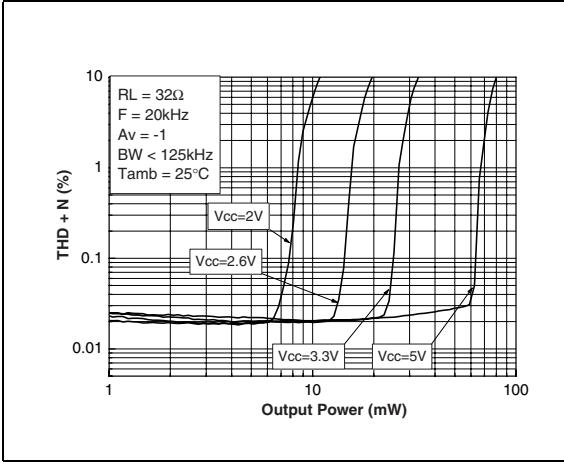
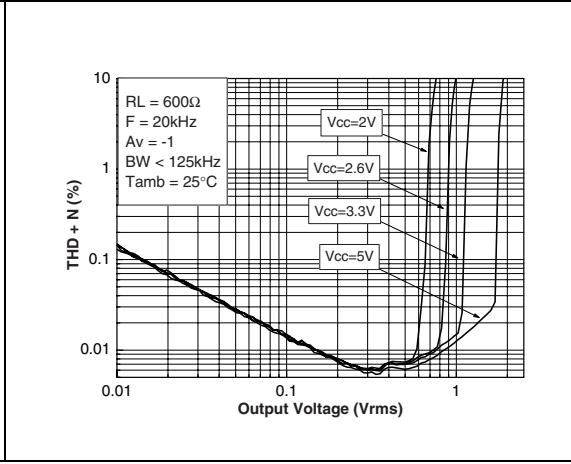
Figure 43. THD + N vs. output power**Figure 44. THD + N vs. output power****Figure 45. THD + N vs. output power****Figure 46. THD + N vs. output power****Figure 47. THD + N vs. output power****Figure 48. THD + N vs. output power**

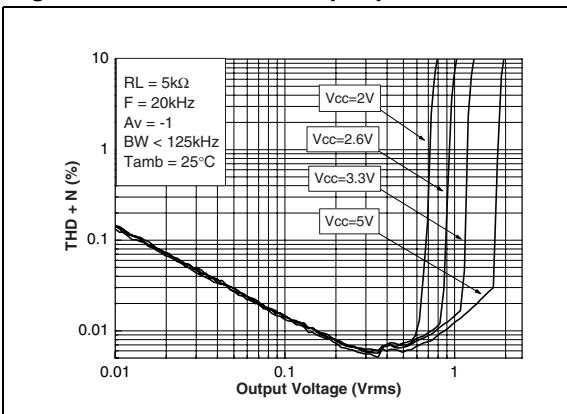
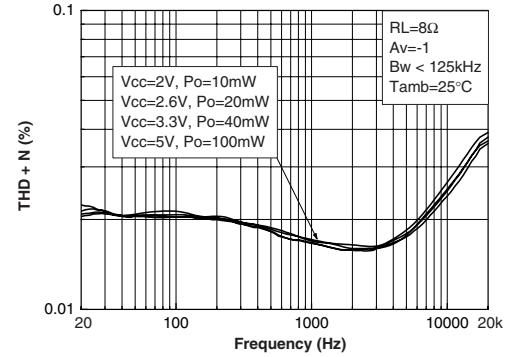
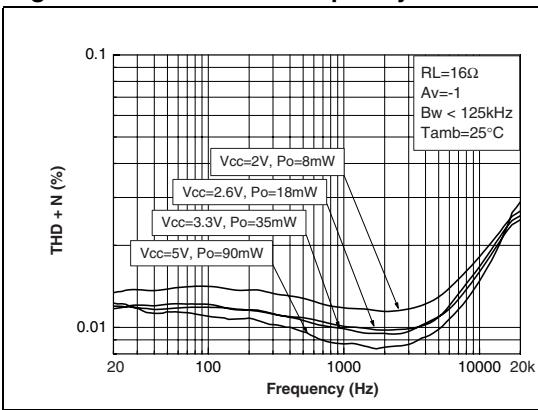
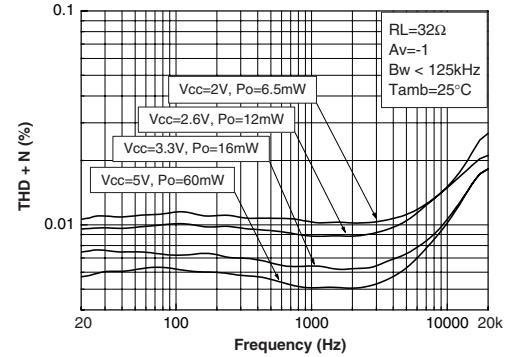
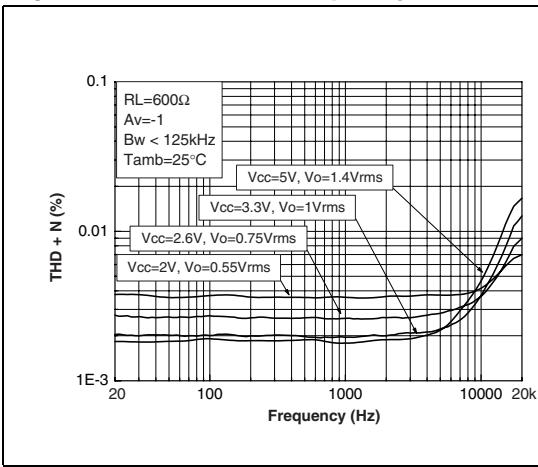
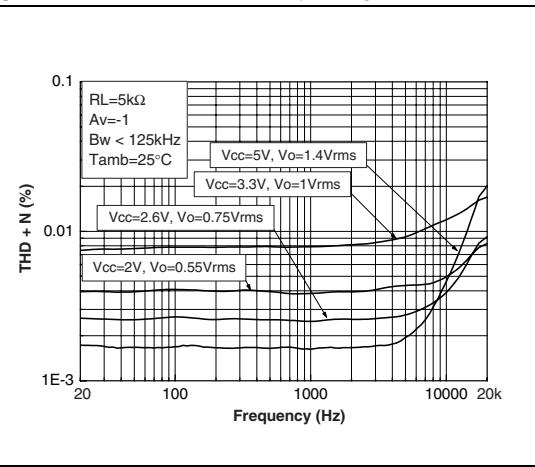
Figure 49. THD + N vs. output power**Figure 50. THD + N vs. frequency****Figure 51. THD + N vs. frequency****Figure 52. THD + N vs. frequency****Figure 53. THD + N vs. frequency****Figure 54. THD + N vs. frequency**

Figure 55. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

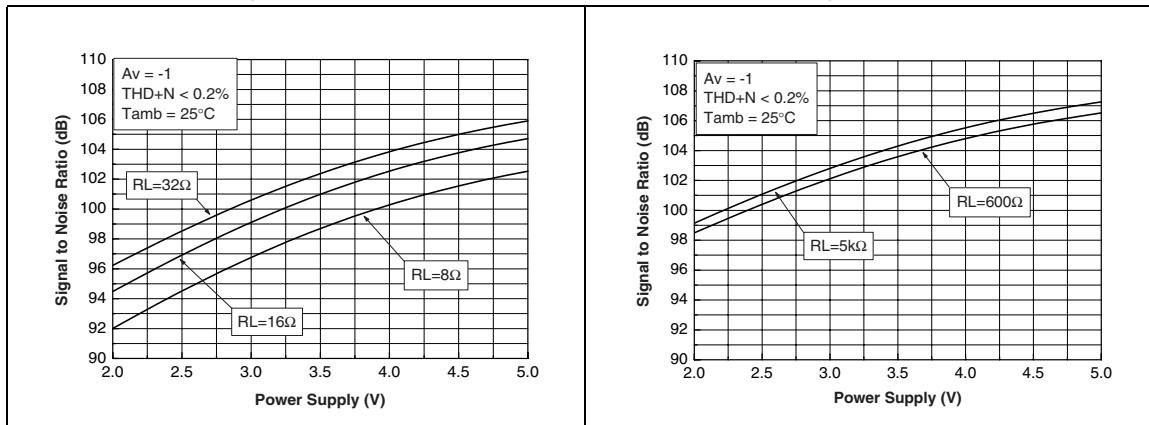


Figure 56. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

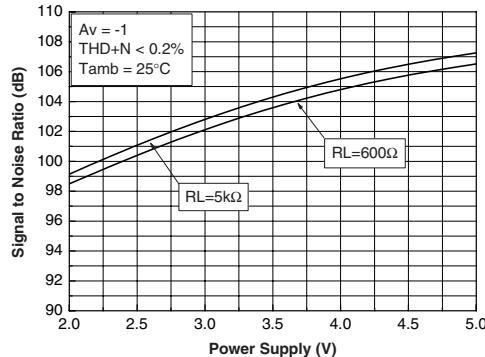


Figure 57. Signal to noise ratio vs. power supply with A weighted filter

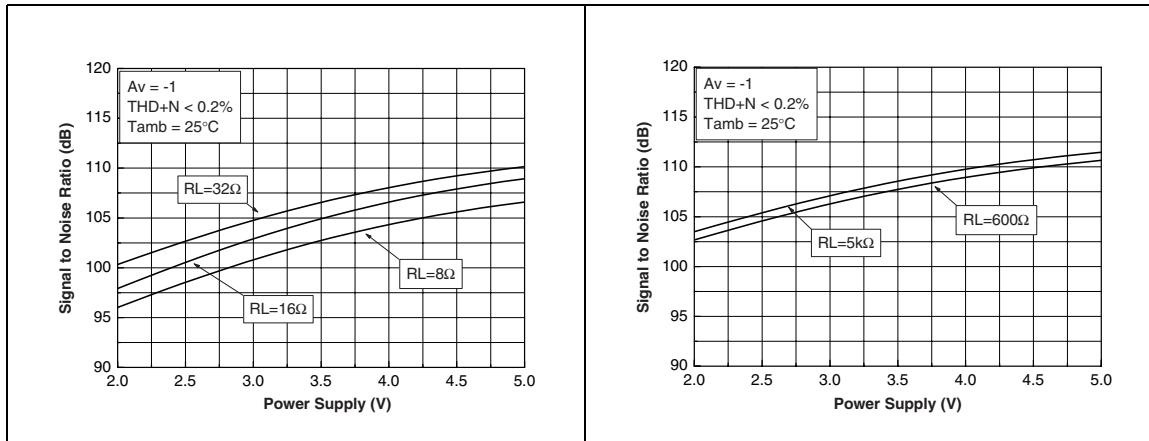


Figure 58. Signal to noise ratio vs. power supply with A weighted filter

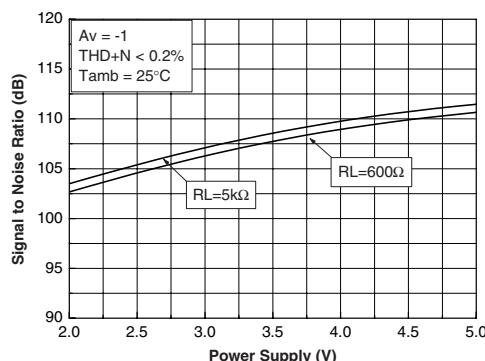


Figure 59. Equivalent input noise voltage vs. frequency

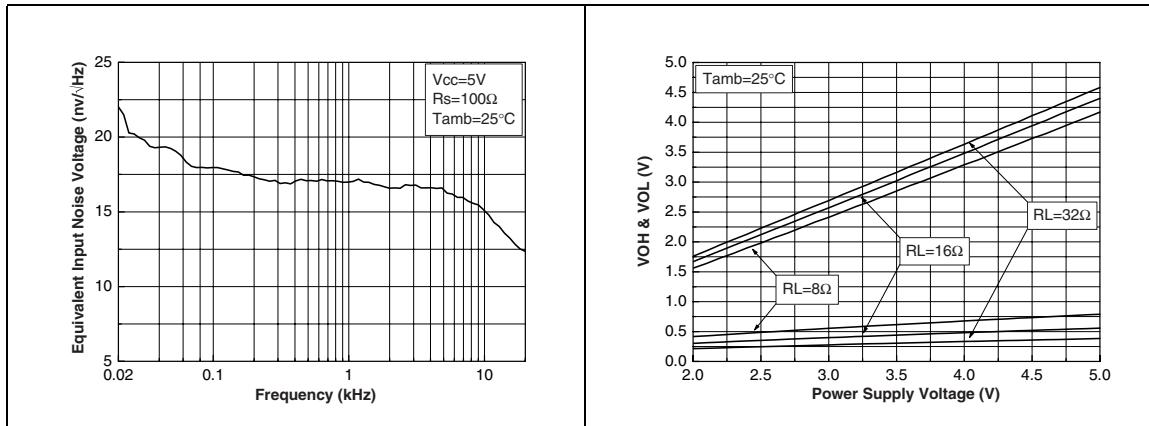


Figure 60. Output voltage swing vs. power supply

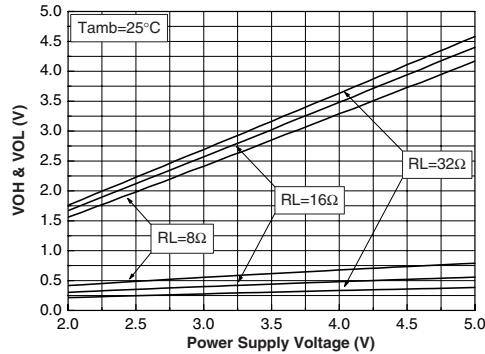


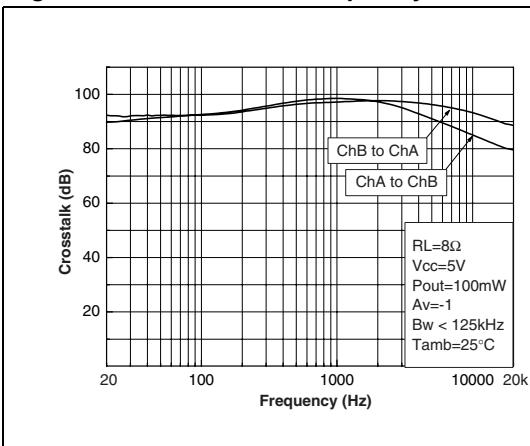
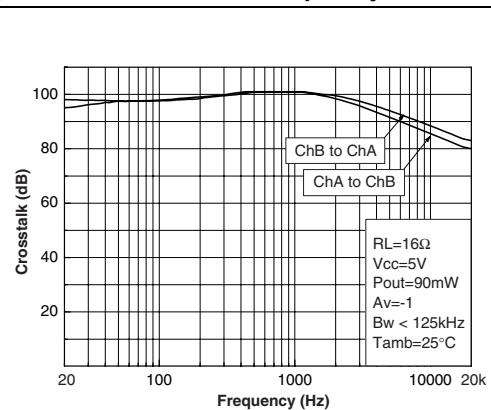
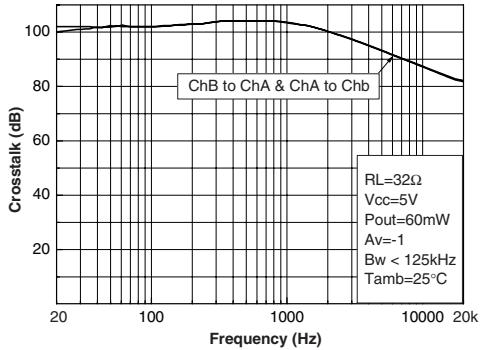
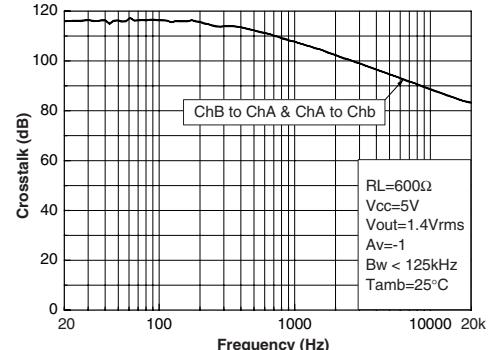
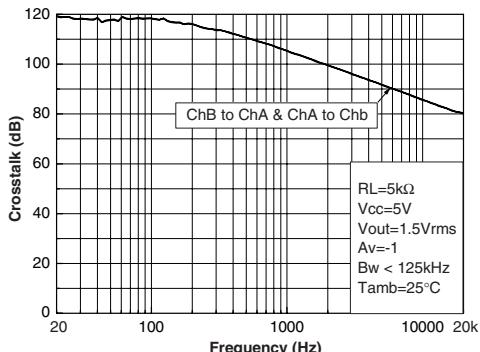
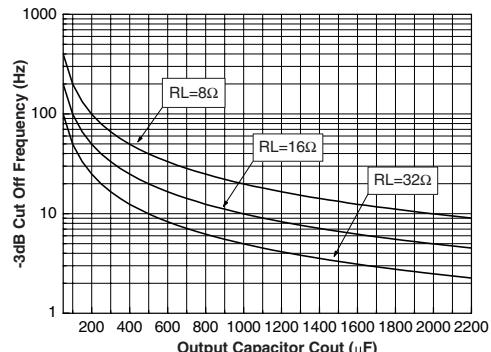
Figure 61. Crosstalk vs. frequency**Figure 62. Crosstalk vs. frequency****Figure 63. Crosstalk vs. frequency****Figure 64. Crosstalk vs. frequency****Figure 65. Crosstalk vs. frequency****Figure 66. Lower cut off frequency vs. output capacitor**

Figure 67. Lower cut off frequency vs. input capacitor

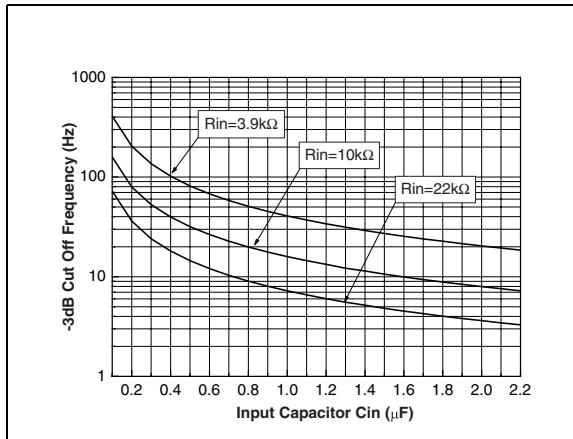


Figure 68. Typical distribution of TDH + N

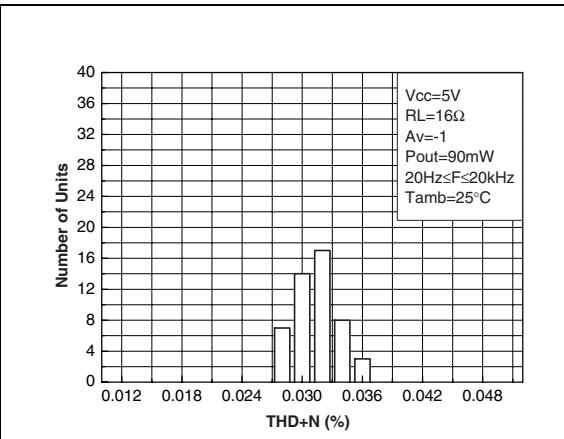


Figure 69. Best case distribution of THD + N

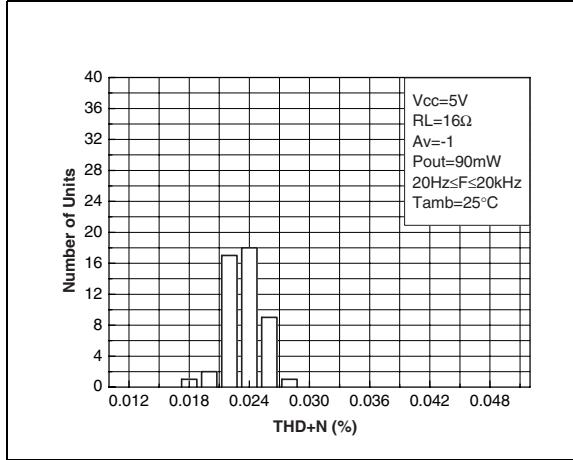


Figure 70. Worst case distribution of THD + N

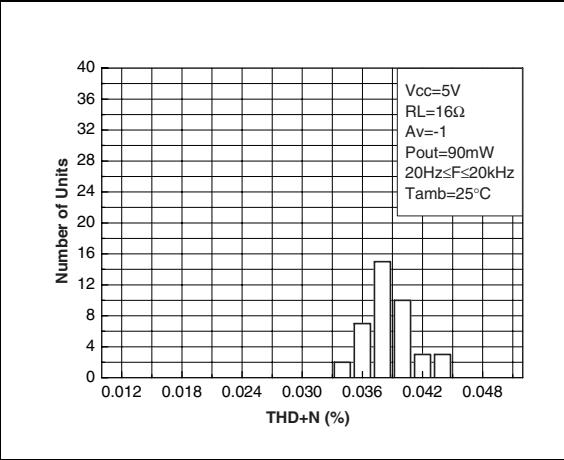


Figure 71. Typical distribution of TDH + N

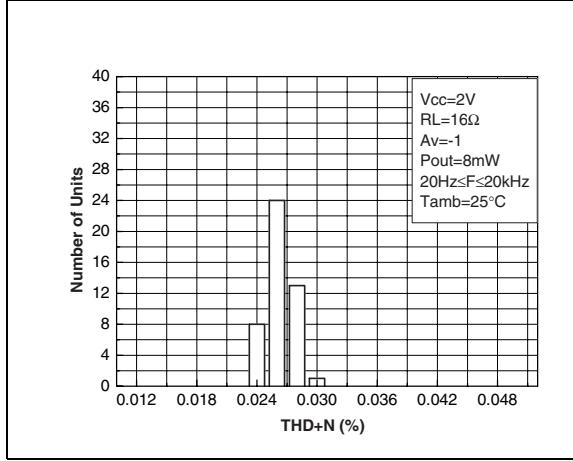


Figure 72. Best case distribution of THD + N

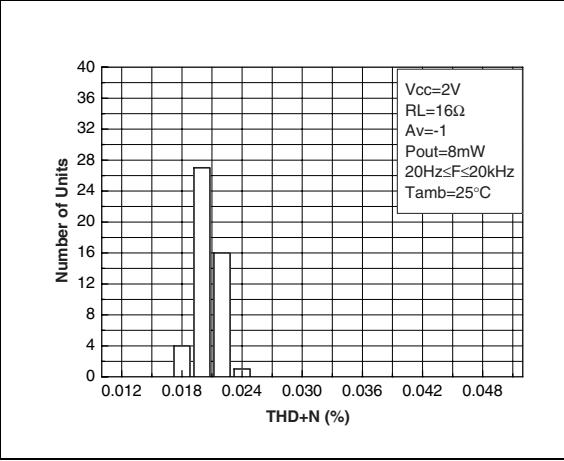


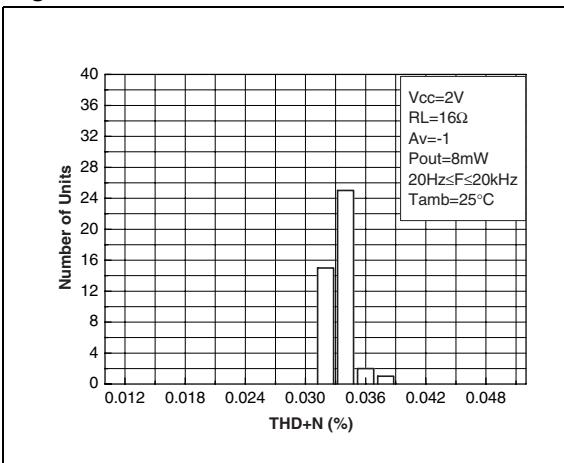
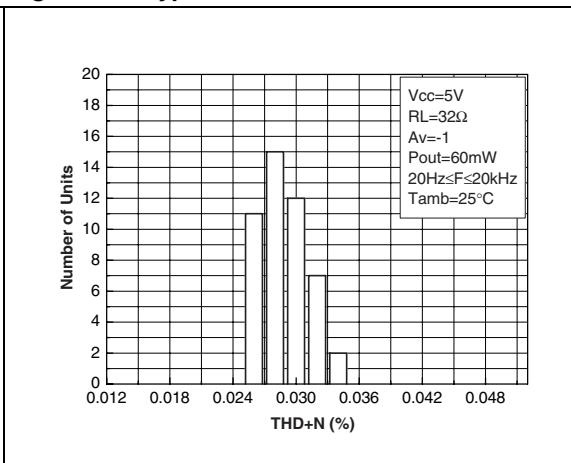
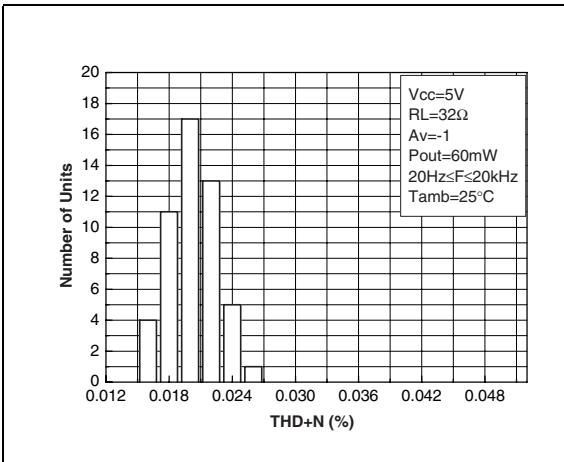
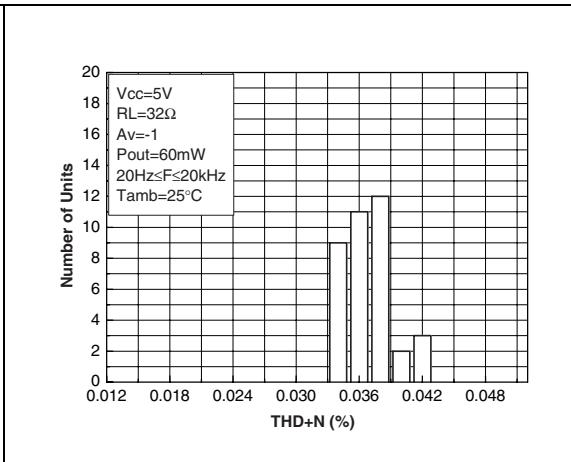
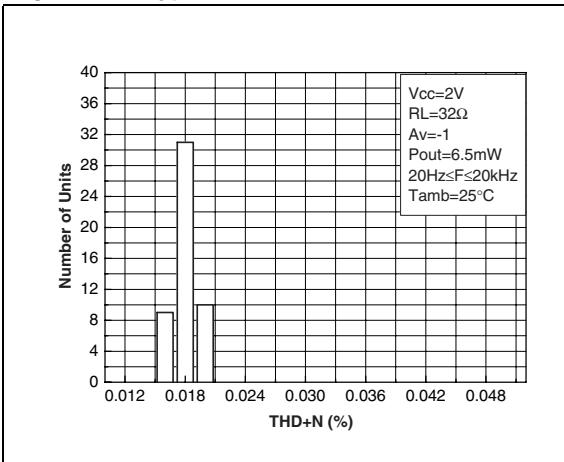
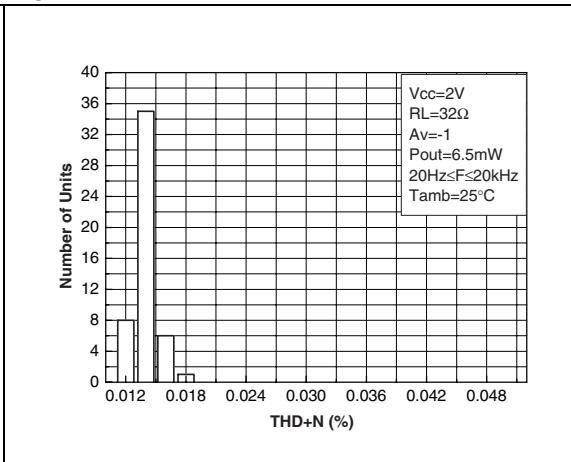
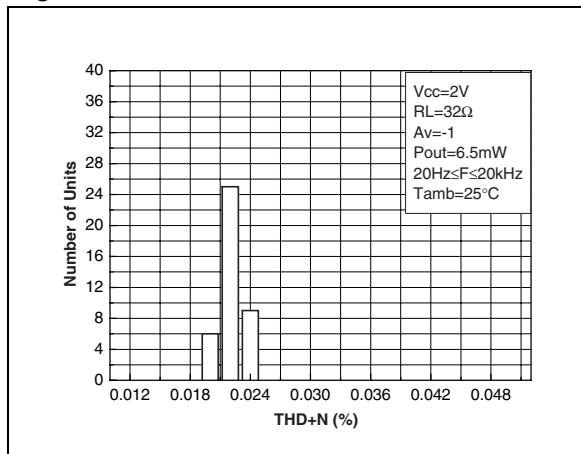
Figure 73. Worst case distribution of THD + N**Figure 74. Typical distribution of TDH + N****Figure 75. Best case distribution of THD + N****Figure 76. Worst case distribution of THD + N****Figure 77. Typical distribution of TDH + N****Figure 78. Best case distribution of THD + N**

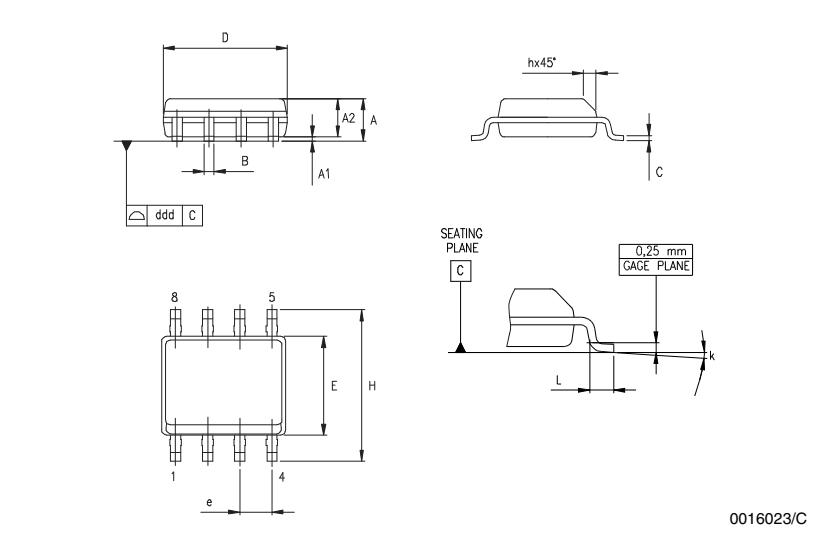
Figure 79. Worst case distribution of THD + N

3 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

3.1 SO-8 Package

SO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04

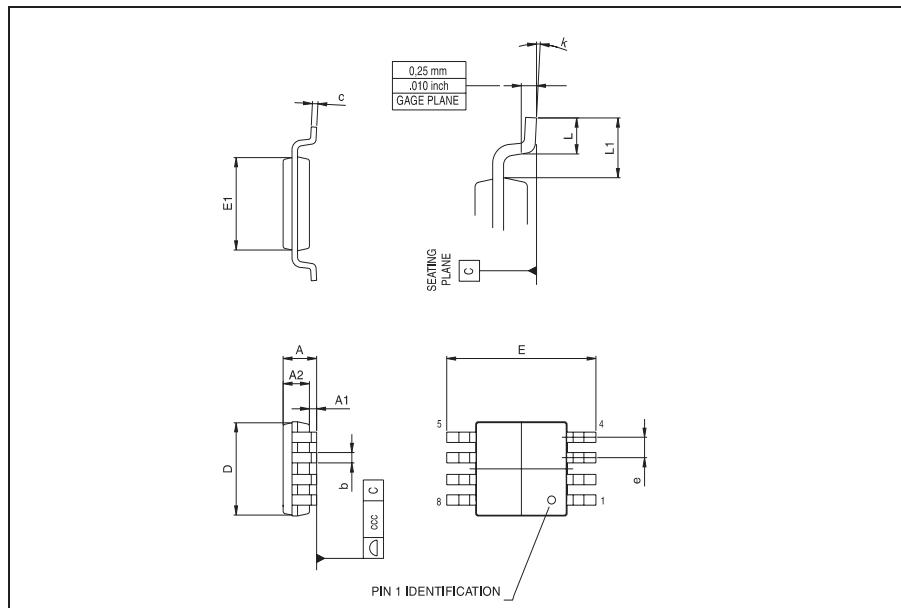


The technical drawings provide three views of the SO-8 package: a top view showing the footprint with pins numbered 1 through 8; a side cross-sectional view showing height dimensions H, h, and L, along with lead profile information (hx45°) and a seating plane indicator; and a bottom cross-sectional view showing the lead profile and a 0.25 mm GAGE PLANE dimension. Reference designators A, A1, A2, B, C, D, E, e, and k are also indicated.

0016023/C

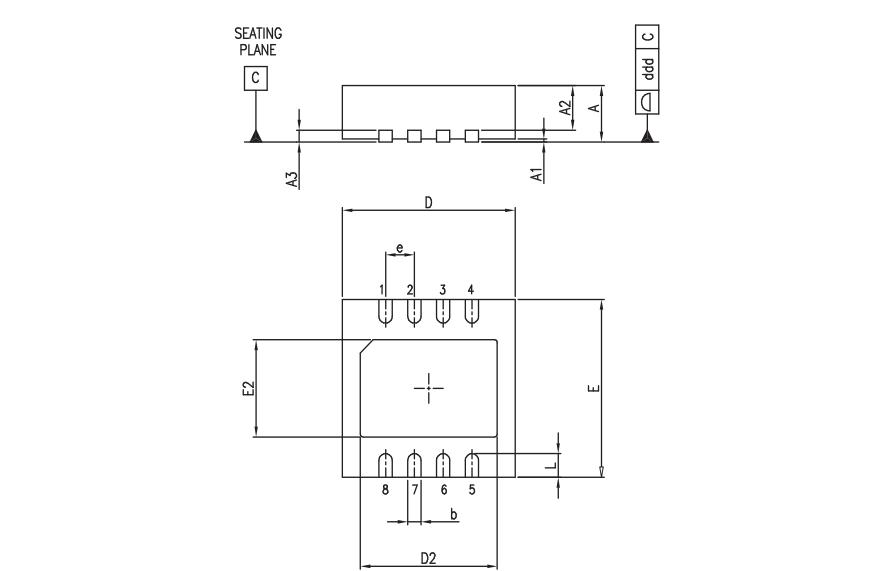
3.2 MiniSO-8 Package

miniSO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



3.3 DFN8 Package

DFN8 (3x3) MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			27.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D	2.875	3.00	3.125		118.1	
D2	2.23	2.38	2.48	87.8	93.7	97.7
E	2.875	3.00	3.125		118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.30	0.40	0.50	11.8	15.7	19.7



The diagram illustrates the top view of the DFN8 package. It shows a central rectangular body with four leads extending from the bottom. The package is mounted on a seating plane. Key dimensions are labeled: A (total height), A1 (lead thickness), A2 (lead pitch), A3 (lead height), b (lead width), D (body width), D2 (body length), E (body height), and e (lead pitch). The leads are numbered 1 through 8, arranged in two rows of four. Lead 1 is at the top left, 2 is to its right, 3 is below 2, 4 is to the right of 3, 5 is at the bottom left, 6 is to its right, 7 is below 6, and 8 is to the right of 7.

4 Revision history

Date	Revision	Changes
June 2003	1	Initial release.
Nov. 2005	2	The following changes were made in this revision: – Lead temperature for lead-free added see <i>Table 1: Key parameters and their absolute maximum ratings on page 2</i> . – Formatting changes throughout.

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