N a t i o n a l   S e m i c o n d u c t o r

N a t i o n a l   S e m i c o n d u c t o r

Preliminary
November 1997

PC87109VBE

PC87109VBE Advanced UART and Infrared Controller

N a t i o n a l   S e m i c o n d u c t o r

PC87109VBE Advanced UART and Infrared Controller

General Description

The PC87109 is a serial communication device with infrared capability. It supports 6 modes of operation and is backward compatible with the 16550 and 16450 (except for the MODEM control functions). The operational modes are: UART, Sharp-IR, IrDA 1.0 SIR, IrDA 1.1 MIR and FIR, and Consumer Electronics IR (also referred to as TV Remote or Consumer Remote Control).

In order to support existing legacy software based upon the 16550 UART, the PC87109 provides a special fallback mechanism that automatically switches the device to 16550 compatibility mode when the baud generator divisor is accessed through the legacy ports in bank 1.

The device architecture has been optimized to meet the requirements of a variety of UART and infrared based applications. DMA support for all operational modes has been incorporated into the architecture.
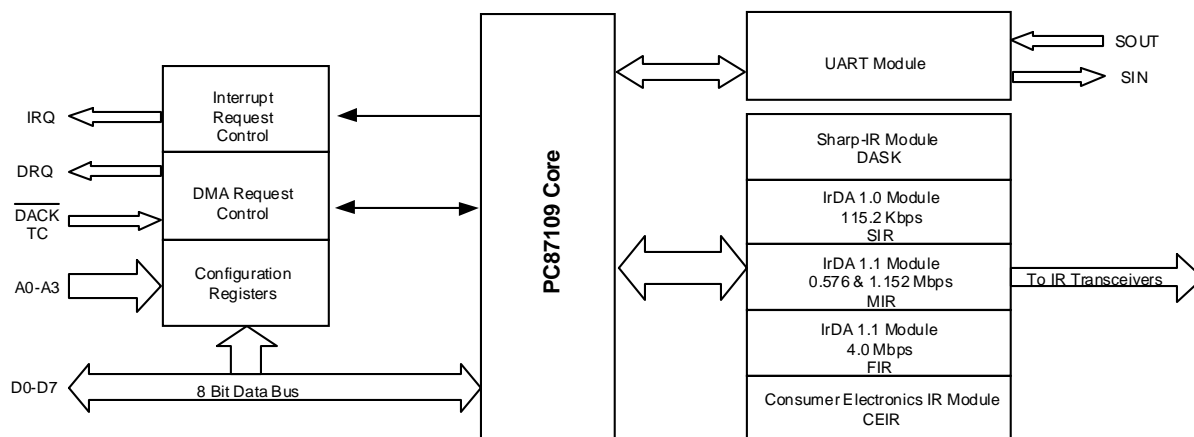
The device uses one DMA channel. One channel is required for infrared based applications since infrared communications work in half duplex fashion.

To further ease driver design and simplify the implementation of infrared protocols, a 12-bit timer with 125μs resolution has also been included.

Features

■ Compatible with 16550 and 16450 devices
■ Extended UART mode
■ Sharp-IR with selectable internal or external modulation
■ IrDA 1.0 SIR with up to 115.2 Kbaud data rate
■ IrDA 1.1 MIR and FIR with 0.576, 1.152 and 4.0 Mbps data rates
■ Consumer Electronics IR mode
■ UART mode data rates up to 1.5 Mbps
■ Back-to-Back infrared frame transmission and reception
■ Full duplex infrared frame transmission and reception
■ Transmit deferral
■ Automatic fallback to 16550 compatibility mode
■ Selectable 16 or 32 level FIFOs
■ 12-bit timer for infrared protocol support
■ Programmable IRQ and DMA signals polarity
■ Support for power management
■ 5V or 3.3V operation with back drive protection
■ 32-pin TQFP package

Block Diagram

IRQ ← Interrupt Request Control
DRQ ← DMA Request Control
DACK TC →
A0-A3 → Configuration Registers
D0-D7 ↔ 8 Bit Data Bus

PC87109 Core

UART Module — SOUT, SIN
Sharp-IR Module DASK
IrDA 1.0 Module 115.2 Kbps SIR
IrDA 1.1 Module 0.576 & 1.152 Mbps MIR — To IR Transceivers
IrDA 1.1 Module 4.0 Mbps FIR
Consumer Electronics IR Module CEIR

TRI-STATE® is a registered trademark of National Semiconductor Corp.
WATCHDOG™ is a trademark of National Semiconductor Corp.

Table Of Contents

List Of Figures

List Of Tables

1.0 Pin Descriptions

1.1 Connection Diagram
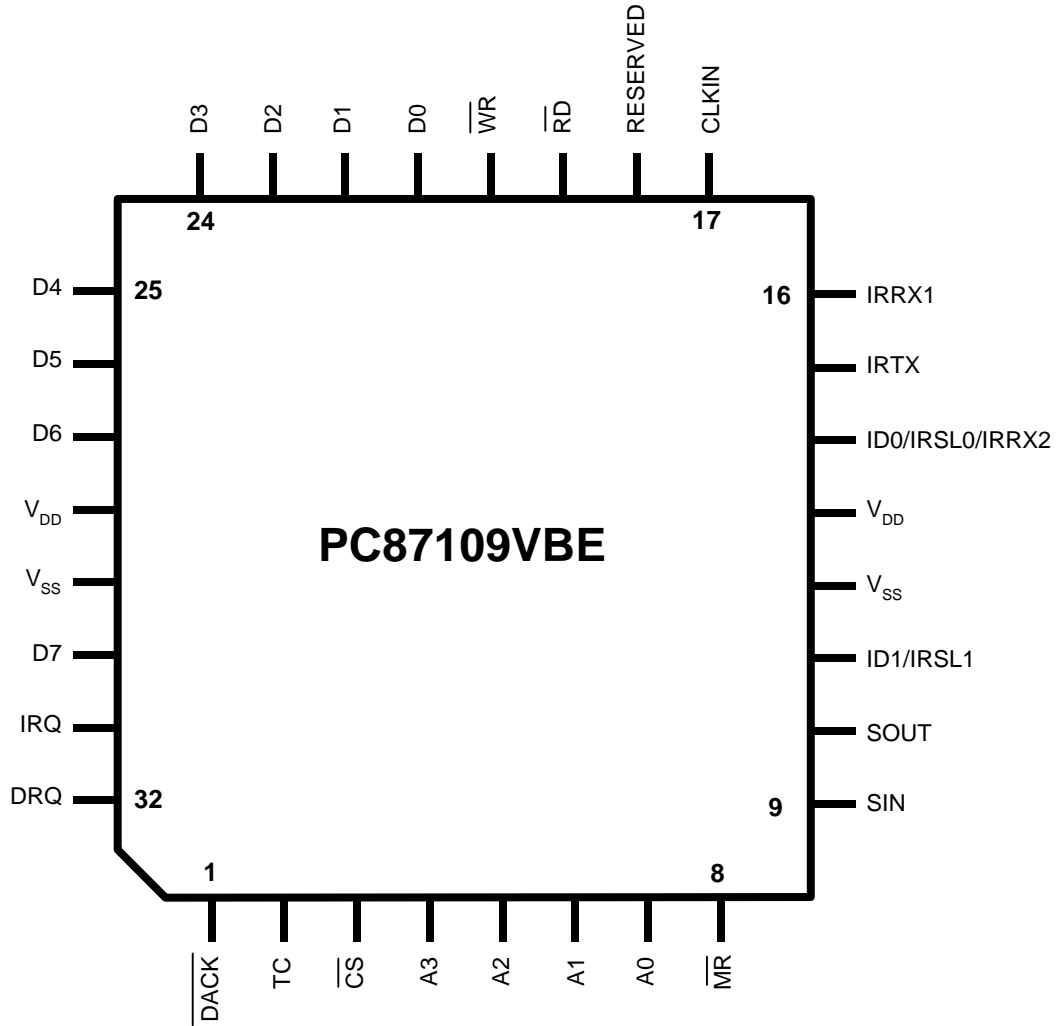
Top View

Figure 1-1. 32-Pin TQFP Package

Order number PC87109VBE
See NS package VBE32A

www.national.com

1.2 Pin Descriptions

Symbol	Pin(s)	Type	Description
SUPPLIES			
V$_{DD}$	13, 28		**5V or 3.3V Power Supply**
V$_{ss}$	12, 29		**Ground.**
BUS INTERFACE SIGNALS			
A0-A3	7-4	I	**Address**. Input signals used to determine which internal register is accessed (Section 4.2). A0-A3 are ignored during a DMA access.
$\overline{CS}$	3	I	**Chip Select**. Active low input used in conjunction with A0-A3 to select the internal registers.
D0-D7	21-27, 30	I/O	**Data Bus**. 8-bit bi-directional data lines used to transfer data between the PC87109 and the CPU or DMA controller. D0 is the LSB and D7 is the MSB.
$\overline{DACK}$	1	I	**DMA Acknowledge**. Used to acknowledge a DMA request and enable the $\overline{RD}$ or $\overline{WR}$ signals during a DMA access cycle. The polarity of this signal is programmable.
DRQ	32	O	**DMA Request**. Used to signal the DMA controller that a data transfer from the PC87109 is required. The polarity of this signal is programmable.
IRQ	31	O	**Interrupt Request**. This output is used to signal an interrupt condition to the CPU (Section 4.2.2). The IRQ signal can be configured to be either open-drain or totem pole. Its polarity is also programmable.
$\overline{MR}$	8	I	**Master Reset**. A low level on this input resets the PC87109. This signal asynchronously terminates any activity and places the device in the Disable state.
$\overline{RD}$	19	I	**Read**. Active low input asserted by the CPU or DMA controller to read data or status information from the PC87109.
TC	2	I	**Terminal Count**. This signal is asserted by the DMA controller to indicate the end of a DMA transfer. The signal is only effective during a DMA access cycle. Its polarity is programmable.
$\overline{WR}$	20	I	**Write**. Active low input asserted by the CPU or DMA controller to write data or control information to the PC87109.
UART INTERFACE SIGNALS			
SIN	9	I	**Serial Data In**. This input receives serial data from the communications link.
SOUT	10	O	**Serial Data Out**. This output sends serial data to the communications link. This signal is set to a Marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
INFRARED INTERFACE SIGNALS			
IRRX1	16	I	**Infrared Receive**. Primary input to receive serial data from the infrared transceiver module. If the infrared transceiver provides two receive data outputs, the low-speed output should be connected to this pin.
ID0/IRSL0/IRRX2	14	I/O	**Transceiver Identification, Control or Secondary Infrared Receive**. Multi function pin implementing the following functions: - ID0, to read identification data to support infrared adapters. - IRSL0, to select the transceiver operational mode. - IRRX2, used either as a high-speed receiver input (for MIR and FIR) to support transceiver modules with two receive data outputs, or as an auxiliary input to support two transceiver modules.
ID1/IRSL1	11	I/O	**Transceiver Identification or Control**. Used to read identification data to support infrared adapters, as well as to select the transceiver operational mode.
IRTX	15	O	**Infrared Transmit**. This output sends serial data to the transceiver module(s).
MISCELLANEOUS SIGNALS			
CLKIN	17	I	**Clock.** 48 MHz clock input.
RESERVED	18	NC	**Reserved**. No connection should be made on this pin.

8
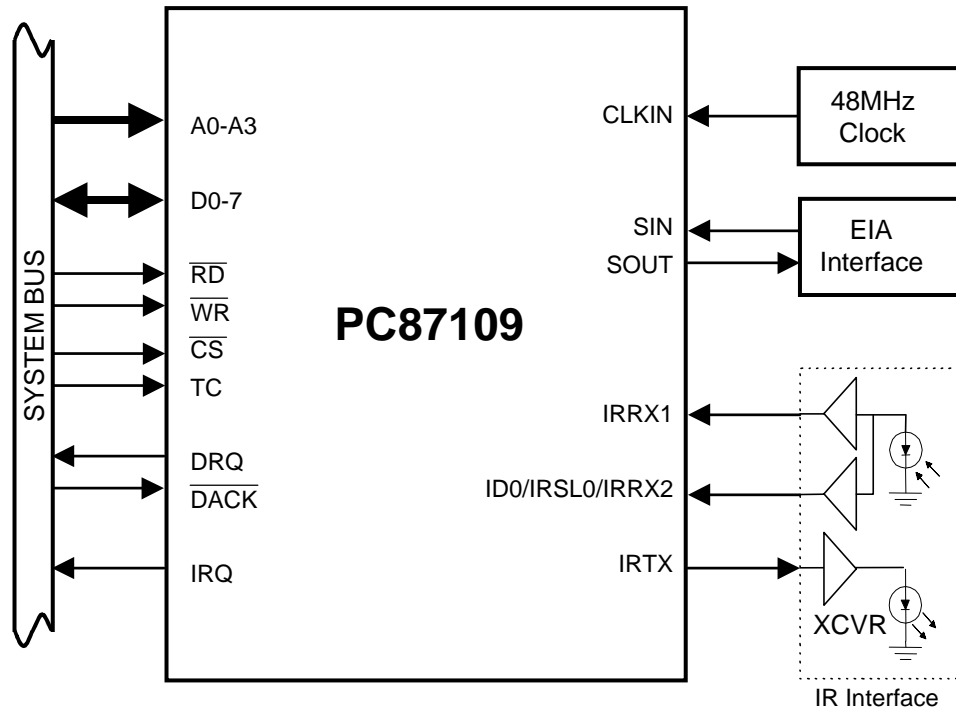
Figure 1-2. Basic Configuration

2.0 Functional Description

2.1 Device Overview

The PC87109 is a serial communications element that implements the most common infrared communications protocols.

In addition to the infrared modes, the device provides a UART mode of operation that is backward compatible to the 16550 to support existing communications software. The device includes two basic modules: the UIR (universal infrared) module and the configuration module. The UIR module implements all the communications functions while the configuration module controls the enabling of the device as well as the enabling the interrupt and DMA control signals. The UIR module uses a register-banking scheme similar to the one used by the 16550.

This minimizes the number of I/O addresses needed to access the internal registers. Most of the communications features are programmed via configuration registers placed in banks 0 through 7. The main control and status information has been consolidated into bank 0 to eliminate unnecessary bank switching. A description of the device operation is provided in the following sections.

2.2 UART Mode

This mode is designed to support serial data communications with a remote peripheral device or modem using a wired interface. The PC87109 provides transmit and receive channels that can operate concurrently to handle full-duplex operation.   They perform parallel-to-serial conversion on data characters received from the CPU or a DMA controller, and serial-to-parallel conversion on data characters received from the serial interface. The format of the serial data stream is shown in figure 1-3. A data character contains from 5 to 8 data bits. It is preceded by a start bit and is followed by an optional parity bit and a stop bit. Data is transferred in Little Indian order (least significant bit first).

The UART mode is the default mode of operation after power up or reset. In fact, after reset, the 16450-compatibility mode is selected. In addition to the 16450 and 16550 compatibility modes, an extended mode of operation is also available. When the extended mode is selected, the architecture changes slightly and a variety of additional features will be made available. The interrupt sources are no longer prioritized, and an auxiliary status and control register replaces the scratch pad register. The additional features include transmitter FIFO thresholding, DMA capability, and interrupts on transmitter empty and DMA event.

The clock for both transmit and receive channels is provided by an internal baud generator that divides its input clock by any divisor value from 1 to 2^{16} - 1. The output clock frequency of the baud generator must be programmed to be sixteen times the baud rate value. The baud generator input clock is derived from a 24 MHz clock through a programmable prescaler. The PRESL bits in the EXCR2 register determine the prescaler value. Its default value is 13. This allows all the standard baud rates, up to 115.2 Kbaud to be obtained. Smaller prescaler values will allow baud rates up to 921.6 Kbaud (standard) and 1.5 Mbaud (non-Standard).

Before operation can begin, both the communications format and the software must program baud rate. The communications format is programmed by loading a control byte into the LCR register, while the baud rate is selected by loading an appropriate value into the baud generator divisor register. The software can read the status of the device at any time during operation. The status information includes FULL/EMPTY state for both transmit and receive channels, and any other condition detected on the received data stream, like a parity error, framing error, data overrun, or break event.
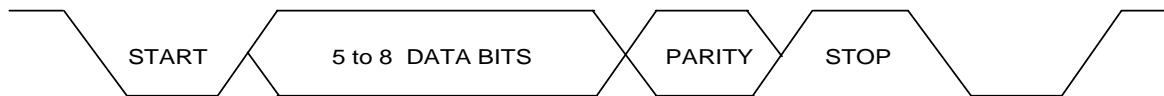
Figure 2-1. Serial Data Stream Format

2.3 Sharp-IR Mode

This mode supports bi-directional data communication with a remote device using infrared radiation as the transmission medium. Sharp-IR uses Digital Amplitude Shift Keying (DASK) and allows serial communication at baud rates up to 38.4 Kbaud. The format of the serial data is similar to the UART data format. Each data word is sent serially beginning with a zero value start bit, an optional parity bit, and ending with at least one stop bit with a binary value of one. Sending a 500 kHz continuous pulse train of infrared radiation signals a zero. A one is signaled by the absence of any infrared signal. The PC87109 can perform the modulation and demodulation operations internally, or it can rely on the external optical module to perform them.

The device operation, in Sharp-IR, is similar to the operation in UART mode. The main difference being that data transfer operation is normally performed in half-duplex fashion. The MDSL bits in the MCR register control selection of the Sharp-IR mode when the device is in extended mode or by the IR_SL bits in the IRCR1 register when the device is in non-extended mode. This prevents legacy software, running in non-extended mode, from spuriously switching the device to UART mode, when the software writes to the MCR register.

2.4 IrDA 1.0 SIR Mode

This is the first operational mode that has been defined by the IrDA committee and, similarly to Sharp-IR, it also supports bi-directional data communication with a remote device using infrared radiation as the transmission medium. IrDA 1.0 SIR allows serial communication at baud rates up to 115.2 Kbaud. The format of the serial data is similar to the UART data format. Each data word is sent serially beginning with a zero value start bit, followed by 8 data bits, and ending with at least one stop bit with a binary value of one. Sending a single infrared pulse signals a zero. A one is signaled by not sending any pulse. The width of each pulse can be either 1.6 µs or 3/16ths of a single bit time. (1.6 µs equals 3/16ths of a bit time at 115.2 Kbaud). This way, each word begins with a pulse for the start bit.
The device operation, in IrDA 1.0 SIR, is similar to the operation in UART mode. The main differences being those data transfer operations are normally performed in half-duplex fashion. Selection of the IrDA 1.0 SIR mode is controlled by the MDSL bits in the MCR register when the device is in extended mode or by the IR_SL bits in the IRCR1 register when the device is in non-extended mode. This prevents legacy software, running in non-extended mode, from spuriously switching the device to UART mode, when the software writes to the MCR register.

2.5 IrDA 1.1 MIR and FIR Modes

The PC87109 supports both IrDA 1.1 MIR and FIR modes, with data rates of 576 Kbps, 1.152 Mbps and 4.0 Mbps. Details on the frame format, encoding schemes, CRC sequences, etc. are provided in the appropriate IrDA documents. The MIR transmitter front-end section performs bit stuffing on the outbound data stream and places the Start and Stop flags at the beginning and end of MIR frames. The MIR receiver front-end section removes flags and "de-stuffs" the inbound bit stream, and checks for abort conditions.
The FIR transmitter front-end section adds the Preamble as well as Start and Stop flags to each frame and encodes the transmit data into a 4PPM (Four Pulse Position Modulation) data stream. The FIR receiver front-end section strips the Preamble and flags from the inbound data stream and decodes the 4PPM data while also checking for coding violations.
Both MIR and FIR front-ends also automatically append CRC sequences to transmitted frames and check for CRC errors on received frames.

2.5.1 High Speed Infrared Transmit

When the transmitter is empty, if either the CPU or the DMA controller writes data into the TX_FIFO, transmission of a frame will begin. Frame transmission can be normally completed by using one of the following methods:

1. S_EOT bit (Set End of Transmission)
This method is used when data transfers are performed in PIO mode. When the CPU sets the S_EOT bit before writing the last byte into the TX_FIFO, the byte will be tagged with an EOF indication. When this byte reaches the TX_FIFO bottom, and is read by the transmitter front-

end, a CRC is appended to the transmitted DATA and the frame is normally terminated.

2. DMA TC Signal (DMA Terminal Count)
This method is used when data transfers are performed in DMA mode. It works similarly to the previous method except that the tagging of the last byte of a frame occurs when the DMA controller asserts the TC signal during the write of the last byte to the TX_FIFO.

3. Frame Length Counter
This method can be used when data transfers are performed in either PIO or DMA mode. The value of the FEND_MD bit in the IRCR2 register determines whether the Frame Length Counter is effective in the PIO or DMA mode. The counter is loaded from the Frame Length Register (TFRL) at the beginning of each frame, and it is decrements as each byte is transmitted. An EOF is generated when the counter reaches zero. This method allows a large data block to be automatically split into equal-size back-to-back frames, plus a shorter frame that is terminated by the DMA TC signal when an 8237 type DMA controller is used.
An option is also provided to stop transmission at the end of each frame. This happens when the transmitter frame-end stop mode is selected (TX_MS bit in IRCR2 register set to 1).
By using this option, the software can send frames of different sizes without re-initializing the DMA controller for each frame. After transmission of each frame, the transmitter stops and generates an interrupt. The software loads the length of the next frame into the TFRL register and restarts the transmitter by clearing the TXHFE bit in the ASCR register.

While a frame is being transmitted, data must be written to the TX_FIFO at a rate dictated by the transmission speed. If the CPU or DMA controller fails to meet this requirement, a transmitter under-run will occur, an inverted CRC is appended to the frame being transmitted, and the frame is terminated with a Stop flag. Data transmission will then stop. Transmission of the inverted CRC will guarantee that the remote receiving device will receive the frame with a CRC error and will discard it.
Following an under-run condition, data transmission always stops at the next frame boundary. The frame bytes from the point where the under-run occurred to the end of the frame will not be sent out to the external infrared interface. Nonetheless, they will be removed from the TX_FIFO by the transmitter and discarded. The under-run indication will be reported only when the transmitter detects the end of frame via one of the methods described above. The software can do various things to recover form an under-run condition. For example, it can simply clear the under-run condition by writing a 1 into bit 6 of ASCR and re-transmit the under-run frame later, or it can re-transmit it immediately, before transmitting other frames.
If it chooses to re-transmit the frame immediately, it needs to perform the following steps:

1. Disable DMA controller, if DMA mode was selected.
2. Read the TXFLV register to determine the number of bytes in the TX_FIFO. (This is needed to determine

the exact point where the under-run occurred, and whether or not the first byte of a new frame is in the TX_FIFO).

3. Reset TX_FIFO.

4. Backup DMA controller registers.
5. Clear Transmitter under-run bit.
6. Re-enable DMA controller.

Note: the setting of the DMA_EN bit in the extended-mode MCR register only controls PIO or DMA mode. The device treats CPU and DMA access cycles the same except that DMA cycles always access the TX_ FIFO or RX_FIFO, regardless of the selected bank. When DMA_EN is set to 1, the CPU can still access the TX_FIFO and RX_FIFO. The CPU accesses will, however, be treated as DMA accesses as far as the function of the FEND_MD bit is concerned.

2.5.2 High Speed Infrared Receive

When the receiver front-end detects an incoming frame, it will start de-serializing the infrared bit stream and load the resulting data bytes into the RX_FIFO. When the EOF is detected, two or four CRC bytes are appended to the received data, and an EOF flag is written into the tag section of the RX_FIFO along with the last byte. In the present implementation, the CRC bytes are always transferred to the RX_FIFO following the data. Additional status information, related to the received frame, is also written into the RX_FIFO tag section at this time. The status information will be loaded into the LSR register when the last frame byte reaches the RX_FIFO bottom.

The receiver keeps track of the number of received bytes from the beginning of the current frame. It will only transfer to the RX_FIFO a number of bytes not exceeding the maximum frame length value, which is programmed via the RFRML register in bank 4. Any additional frame bytes will be discarded. When the maximum frame length value is exceeded, the MAX_LEN error flag will be set.

Although data transfers from the RX_FIFO to memory can be performed either in PIO or DMA mode, DMA mode should be used due to the high data rates.

In order to handle back-to-back incoming frames, when DMA mode is selected and an 8237 type DMA controller is used, an 8-level ST_FIFO (Status FIFO) is provided. When an EOF is detected, in 8237 DMA mode, the status and byte count information for the frame is written into the ST_FIFO. An interrupt is generated when the ST_FIFO level reaches a programmed threshold or an ST_FIFO time-out occurs.

The CPU uses this information to locate the frame boundaries in the memory buffer where the 8237 type DMA controller has transferred the data.

During reception of multiple frames, if the RX_FIFO and/or the ST_FIFO fills up, due to the DMA controller or CPU not serving them in time, one or more frames can be crushed and lost. This means that no bytes belonging to these frames were written to the RX_FIFO. In fact, a frame will be lost in 8237 mode when the ST_FIFO is full for the entire time during which the frame is being received, even though there were empty locations in the RX_FIFO. This is because no data bytes can be loaded into the RX_FIFO and then transferred to memory by the DMA controller, unless there is at least one available entry in the ST_FIFO to store the number of received bytes. This information, as mentioned before, is needed by the software to locate the frame boundaries in the DMA memory buffer.

In the event that a number of frames are lost, for any of the reasons mentioned above, one or more lost-frame indications including the number of lost frames, are loaded into the ST_FIFO.

Frames can also be lost in PIO mode, but only when the RX_FIFO is full. The reason being that, in these cases, the ST_FIFO is only used to store lost-frame indications. It will not store frame status and byte count.

2.6 Consumer Electronics IR (CEIR) Mode

The Consumer Electronics IR circuitry is designed to optimally support all the major protocols presently used in remote-controlled home entertainment equipment. The main protocols currently in use are RC-5, RC-6, RECS 80, NEC and RCA. The PC87109, in conjunction with an external optical module, provides the physical layer functions necessary to support these protocols. These functions include modulation, demodulation, serialization, de-serialization, data buffering, status reporting, interrupt generation, etc. The software is responsible for the generation of the infrared code to be transmitted, and for the interpretation of the received code.

2.6.1 Consumer Electronics IR Transmit

The code to be transmitted consists of a sequence of bytes that represent either a bit string or a set of run-length codes. The number of bits or run-length codes usually needed to represent each infrared code bit depends on the infrared protocol used. The RC-5 protocol, for example, needs two bits or between one and two run-length codes to represent each infrared code bit.

CEIR transmission starts when the transmitter is empty and either the CPU or the DMA controller writes code bytes into the TX_FIFO. The transmission is normally completed when the CPU sets the S_EOT bit in the ASCR register before writing the last byte, or when the DMA controller activates the TC signal. Transmission is also completed if the CPU simply stops transferring data and the transmitter becomes empty. In this case however, a transmitter under-run condition will be generated. The under-run must be cleared before the next transmission can occur. The code bytes written into the TX_FIFO are either de-serialized or run-length decoded, and the resulting bit string is modulated by a sub-carrier signal and sent to the transmitter LED. The bit rate of this bit string, like in the UART mode, is determined by the value programmed in the baud generator divisor register. Unlike a UART

transmission, start, stop and parity bits are not included in the transmitted data stream. Logic 1 in the bit string will keep the LED off, so no infrared signal is transmitted. A logic 0 will generate a sequence of modulating pulses which will turn on the transmitter LED. Frequency and pulse width of the modulating pulses are programmed by the MCFR and MCPW bits in the IRTXMC register as well as the TXHSC bit in the RCCFG register.

The RC_MMD bits select the transmitter modulation mode. If C_PLS mode is selected, modulation pulses are generated continuously for the entire time in which one or more logic 0 bits are being transmitted. If 6_PLS or 8_PLS modes are selected, 6 or 8 pulses are generated each time one or more logic 0 bits are transmitted following logic 1 bit. C_PLS modulation mode is used for RC-5, RC-6, NEC and RCA protocols. 8_PLS or 6_PLS modulation mode is used for the RECS 80 protocol. The 8_PLS or 6_PLS mode allows minimization of the number of bits needed to represent the RECS 80 infrared code sequence. The current transmitter implementation supports only the modulated modes of the RECS 80 protocol. The flash mode is not supported since it is not popular and is becoming less frequently used.

Note: The total transmission time for the logic 0 bits must be equal or greater than 6 or 8 times the period of the modulation sub-carrier, otherwise fewer pulses will be transmitted.

2.6.2 Consumer Electronics IR Receive

The CEIR receiver is significantly different from a UART receiver for two basic reasons. First, the incoming infrared signals are DASK modulated. Therefore, a demodulation operation may be necessary. Second, there are no start bits in the incoming data stream.

Whenever an infrared signal is detected, the operations performed by the receiver are slightly different depending on whether or not receiver demodulation is enabled. If the demodulator is not enabled, the receiver will immediately switch to the active state. If the demodulator is enabled, the receiver checks the sub-carrier frequency of the incoming signal, and it switches to the active state only if the frequency falls within the programmed range. If this is not the case, the signal is ignored and no other action is taken. When the receiver active state is entered, the RXACT bit in the ASCR register is set to 1. Once in the active state, the receiver keeps sampling the infrared input signal and generates a bit streams where logic 1 indicates an idle condition and logic 0 indicates the presence of infrared energy. The infrared input is sampled regardless of the presence of infrared pulses at a rate determined by the value loaded into the baud generator divisor register.   The received bit string is both de-serialized and assembled into 8-bit characters, or it is converted to run-length encoding values. The resulting data bytes are then transferred to the RX_FIFO.

The receiver also sets the RXWDG bit in the ASCR register each time an infrared pulse signal is detected. This bit is automatically cleared when the ASCR register is read, and it is intended to assist the software in determining when the infrared link has been idle for a certain time. The software can then stop the data reception by writing a 1 into the RXACT bit to clear it and return the receiver to the inactive state.

The frequency bandwidth for the incoming modulated infrared signal is selected by DFR and DBW bits in the IRRXDC register. There are two CEIR receiver data modes: "Over-sampled" and "Programmed-T-Period" mode. For either mode the sampling rate is determined by the setting of the baud generator divisor register.

The "Over-sampled" mode can be used with the receiver demodulator either enabled or disabled. It should be used with the demodulator disabled when a detailed snapshot of the incoming signal is needed, for example to determine the period of the sub-carrier signal. If the demodulator is enabled, the stream of samples can be used to reconstruct the incoming bit string. To obtain a good resolution, a fairly high sampling rate should be selected.

The "Programmed-T-Period" mode should be used with the receiver demodulator enabled. The T Period represents one half bit time, for protocols using bi-phase encoding, or the basic unit of pulse distance, for protocols using pulse distance encoding. The baud rate is usually programmed to match the T Period. For long periods of logic low or high, the receiver samples the demodulated signal at the programmed sampling rate.

Whenever a new infrared energy pulse is detected, the receiver will re-synchronize the sampling process to the incoming signal timing. This reduces timing related errors and eliminates the possibility of missing short infrared pulse sequences, especially when dealing with the RECS 80 protocol. In addition, the "Programmed-T-Period" sampling minimizes the amount of data used to represent the incoming infrared signal, therefore reducing the processing overhead in the host CPU.

2.7 FIFO Time-outs

In order to prevent received data from sitting in the RX _FIFO and/or the ST_FIFO indefinitely, if the programmed interrupt or DMA thresholds are not reached, time-out mechanisms are provided.

An RX_FIFO time-out generates a receiver High-Data-Level interrupt and/or a Receiver DMA request if bit 0 of IER and/or bit 2 of MCR (in extended mode) are set to 1 respectively. An RX_FIFO time-out also sets bit 0 of ASCR to 1 if the RX_FIFO is below the threshold. This bit is tested by the software, when a receiver High-Data-Level interrupt occurs, to decide whether a number of bytes, as indicated by the RX_FIFO threshold, can be read without checking bit 0 of the LSR register. An ST_FIFO time-out is enabled only in MIR and FIR modes, and generates an interrupt if bit 6 of IER is set to 1.

The conditions that must exist for a time-out to occur in the various modes of operation are described below. When a time-out has occurred, it can only be reset when the CPU or DMA controller reads the FIFO that caused the time-out.

MIR or FIR Modes
  RX_FIFO Time-out Conditions:
    1.   At least one byte is in the RX_FIFO, and
    2.   More than 64 μs have elapsed since the last byte was loaded into the RX_FIFO from the receiver logic, and

3. More than 64 µs have elapsed since the last byte was read from the RX_FIFO by the CPU or DMA controller.

ST_FIFO Time-out Conditions:
1. At least one entry is in the ST_FIFO, and
2. More than 1 ms has elapsed since the last byte was loaded into the RX_FIFO from the receiver logic, and
3. More than 1 ms has elapsed since the CPU read the last entry from the ST_FIFO.

UART, Sharp-IR, SIR Modes
RX_FIFO Time-out Conditions:
1. At least one byte is in the RX_FIFO, and
2. More than four character times have elapsed since the last byte was loaded into the RX_FIFO from the receiver   logic, and
3. More than four character times have elapsed since the last byte was read from the RX_FIFO by the CPU or DMA controller.

CEIR Mode
RX_FIFO Time-out Conditions:
The RX_FIFO Time-out, in CEIR mode, is disabled while the receiver is active. The conditions for this time-out to occur are as follows:
1. At least one byte has been in the RX_FIFO for 64 µs or more, and
2. The receiver has been inactive (RXACT=0) for 64 µs or more, and
3. More than 64 µs have elapsed since the last byte was read from the RX_FIFO by the CPU or DMA controller.

2.8 Transmit Deferral

This feature allows the software to send short high-speed data frames in PIO mode without the risk of a transmitter under-run being generated. Even though this feature is available and works the same way in all modes, it will most likely be used in MIR and FIR modes to support high-speed negotiations. This is because in other modes, either the transmit data rate is relatively low and thus the CPU can keep up with it without letting an under-run occur, as in the case CEIR Mode, or transmit under-runs are allowed and are not considered to be error conditions.

Transmit deferral is available only in extended mode and when the TX_FIFO is enabled. When transmit deferral is enabled (TX_DFR bit of MCR set to 1) and the transmitter becomes empty, an internal flag will be set that locks the transmitter. If the CPU now writes data into the TX_FIFO, the transmitter will not start sending the data until the TX_FIFO level reaches either 14 for a 16-level TX_FIFO, or 30 for a 32-level TX_FIFO, at which time the internal flag is cleared. The internal flag is also cleared and the transmitter starts transmitting when a time-out condition is reached. This prevents some bytes from being in the TX_FIFO indefinitely if the threshold is not reached. A timer that is enabled when the internal flag is set and there is at least one byte in the TX_FIFO implements the time-out mechanism. Whenever a byte is loaded into the TX_FIFO the timer gets reloaded with the initial value. If no

bytes are loaded for a 64 µs time, the timer times out and the internal flag gets cleared, thus enabling the transmitter.

2.9 Automatic Fallback to 16550 Compatibility Mode

This feature is designed to support existing legacy software packages using the 16550 UART.

For proper operation, many of these software packages require that the device look identical to a plain 16550 since they access the UART registers directly.

Due to the fact that several extended features as well as new operational modes are provided, the user must make sure that the device is in the proper state before a legacy program can be executed.

The fallback mechanism is designed for this purpose. It eliminates the need for user intervention to change the state of the device, when a legacy program must be executed following completion of a program that used any of the device's extended features.

This mechanism automatically switches the device to 16550 compatibility mode and turns off any extended features whenever the baud generator divisor register is accessed through the LBGDL or LBGDH ports in register bank 1.

In order to avoid spurious fallbacks, baud generator divisor ports are provided in bank 2. Accesses of the baud generator divisor through these ports will change the baud rate setting but will not cause a fall back.

New programs, designed to take advantage of the device extended features, should not use LBGDL and LBGDH to change the baud rate. They should use the BGDL or BGDH instead.

A fallback can occur from either extended or non-extended modes. If extended mode is selected, fallback is always enabled. In this case, when a fallback occurs, the following happens:

1. Transmitter and receiver FIFOs will switch to 16 levels.
2. A value of 13 will be selected for the baud generator prescaler.
3. The ETDLBK and BTEST bits in the EXCR1 Register will be cleared.
4. UART mode will be selected.
5. A switch to non-extended mode will occur.

When a fallback occurs from non-extended mode, only the first three of the above actions will take place. No switching to UART mode occurs if either Sharp-IR or SIR infrared modes were selected. This prevents spurious switching to UART mode when a legacy program, running in infrared mode, accesses the baud generator divisor register from bank 1.

Setting the LOCK bit in the EXCR2 register can disable fallback from non-extended mode. When Lock is set to 1 and the device is in non-extended mode, two scratch-pad registers overlaid with LBGDL and LBGDH are enabled. Any attempted CPU access of the baud generator divisor register through LBGDL and LBGDH will access the scratch-pad registers, and the baud rate setting will not be affected. This feature allows existing legacy programs to run faster than 115.2 Kbaud without their being aware of it.

2.10 Optical Transceiver Interface

The PC87109 implements a very flexible interface for the external infrared transceiver. Several signals are provided for this purpose. A transceiver module with one or two receive signals can be directly interfaced without any additional logic.

Since various operational modes are supported, the transmitter power as well as the receiver filter in the transceiver module must be configured according to the selected mode.

Two special interface pins (ID/IRSL[1-0]) are used to control the operational mode of the infrared transceiver.

The logic levels of the ID/IRSL[1-0] pins are directly controlled by the software (through the setting of bits 1-0 in the IRCFG1 register).

The ID/IRSL[1-0] pins will power up as inputs and can be driven by an external source. When in input mode, they can be used to read the identification data of Plug-n-Play infrared adapters.

The ID0/IRSL0/IRRX2 pin can also function as an input to support an additional infrared receive signal. In this case, however, only one configuration pin will be available. The IRSL0_DS and IRSL1_DS bits in the IRCFG4 register determine the direction of the ID/IRSL[1-0] pins.

www.national.com

3.0   Architectural Description

Eight register banks are provided to control the operation of the UIR module. These banks are mapped into the same address range, and only the selected bank is directly accessible by the software. The address range spans 8 byte locations. The BSR register is used to select the bank and is common to all banks. Therefore, each bank defines seven new registers. The register banks can be divided into two sets. Banks 0-3 are used to control both UART and infrared modes of operation; banks 4-7 are used to control and configure the infrared modes only. The register bank main functions are listed in Table 3-1. Descriptions of the various registers are given in the following sections.
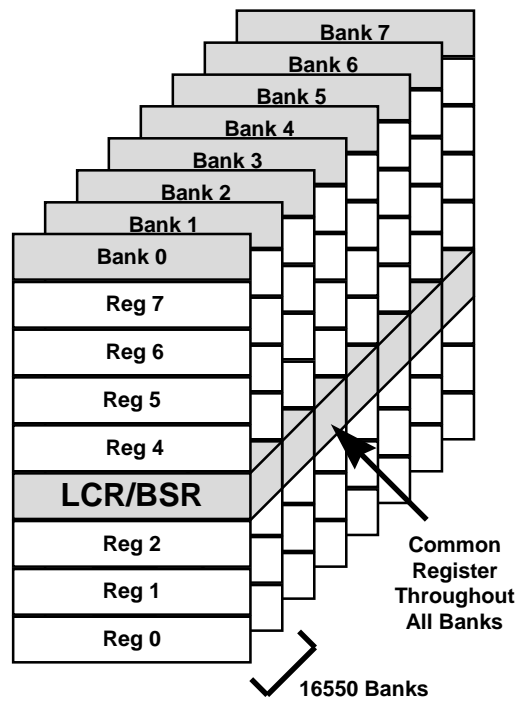
Figure 3-1. Register Bank Architecture

Bank	UART Mode	IR Mode	Description
0	✓	✓	Global Control and Status Registers
1	✓	✓	Legacy Bank
2	✓	✓	Baud Generator Divisor and Extended Control
3	✓	✓	Identification and Shadow Registers
4		✓	Timer and Counters
5		✓	Infrared Control and Status FIFO
6		✓	Infrared Physical Layer Configuration
7		✓	CEIR and Optical Transceiver Configuration

Table 3-1. Register Banks Summary

3.1 Bank 0

Address Offset	Register Name	Description
0	**TXD/RXD**	Transmit/Receive Data Ports
1	**IER**	Interrupt Enable Register
2	**EIR/FCR**	Event Identification/FIFO Control Registers
3	**LCR/BSR**	Link Control/Bank Select Registers.
4	**MCR**	Mode Control Register
5	**LSR**	Link Status Register
6	**Reserved**	Reserved (return 0x30 upon read).
7	**SPR/ASCR**	Scratch-pad /Auxiliary Status and control Register

Table 3-2. Bank 0 Register Set

3.1.1 TXD/RXD - Transmit/Receive Data Ports

These ports share the same address.

TXD is accessed during CPU write cycles.   It provides the write data path to the transmitter holding register when the FIFOs are disabled, or to the TX_FIFO top location when the FIFOs are enabled.

RXD is accessed during CPU read cycles. It provides the read data path from the receiver holding register when the FIFOs are disabled, or from the RX_FIFO bottom location when the FIFOs are enabled.

DMA cycles always access the transmitter and receiver holding registers or FIFOs, regardless of the selected bank.

3.1.2 IER - Interrupt Enable Register

This register controls the enabling of the various interrupts. Some interrupts are common to all operating modes, while others are only available with specific modes. Bits 4 to 7 can be set in extended mode only. They are cleared in non-extended mode. When a bit is set to 1, an interrupt is generated when the corresponding event occurs. In the non-extended mode most events can be identified by reading the LSR and MSR registers. Reading the EIR register after the corresponding interrupt has been generated can only identify the receiver high-data-level event. In the extended mode event flags in the EIR register identify events. Upon reset, all bits are set to 0.

Note1: If the interrupt signal drives an edge-sensitive interrupt controller input, it is advisable to disable all interrupts by clearing all the IER bits upon entering the interrupt routine, and re-enable them just before exiting it. This will guarantee proper interrupt triggering in the interrupt controller in case one or more interrupt events occur during execution of the interrupt routine.

Note 2: If an interrupt source must be disabled, the CPU can do so by clearing the corresponding bit in the IER register. However, if an interrupt event occurs just before the corresponding enable bit in the IER register is cleared, a spurious interrupt may be generated. To avoid this problem, the clearing of any IER bit should be done during execution of the interrupt service routine.   If the interrupt controller is programmed for level-sensitive interrupts, the clearing of IER bits can also be performed outside the interrupt service routine, but with the CPU interrupt disabled.

Note 3: If the LSR, MSR or EIR registers are to be polled, the interrupt sources which are identified via self-clearing bits should have their corresponding IER bits set to 0. This will prevent spurious pulses on the interrupt output pin.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	TMR_IE	SFIF_IE	TXEMP_IE	DMA_IE	res	LS_IE/ TXHLT_IE	TXLDL_IE	RXHDL_IE
Reset State	0	0	0	0	0	0	0	0

Figure 3-2. Interrupt Enable Register

B0　　**RXHDL_IE** - **Receiver High-Data-Level Interrupt Enable.**

B1　　**TXLDL_IE** - **Transmitter Low-Data-Level Interrupt Enable.**

B2   *UART, Sharp-IR, SIR Modes*
      LS_IE - Link Status Interrupt Enable.

     MIR, FIR, CEIR Modes
      LS_IE/TXHLT_IE - Link Status/Transmitter Halted Interrupt Enable.

B3   **Reserved**
     Read/Write as 0.

B4   **DMA_IE - DMA Interrupt Enable.**

B5   **TXEMP_IE - Transmitter Empty Interrupt Enable.**

B6   *MIR, FIR Modes*
     SFIF_IE - ST_FIFO Interrupt Enable.

B7   **TMR_IE - Timer Interrupt Enable.**

3.1.3 EIR/FCR - Event Identification/FIFO Control Registers

These registers share the same address.
EIR is accessed during CPU read cycles while FCR is accessed during CPU write cycles.

EIR - Event Identification Register, Read Only.
The function of this register changes depending upon whether the device is in extended or non-extended mode.

Non-Extended Mode

The function of EIR is the same as in the 16550. It returns an encoded value representing the highest priority pending interrupt. While a CPU access is occurring, the device records new interrupts, but it does not change the currently encoded value until the access is complete. Table 3-3 shows the interrupt priorities and the EIR encoded values.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	FEN1	FEN0	0	0	RXFT	IPR1	IPR0	IPF
Reset State	0	0	0	0	0	0	0	1

Figure 3-3. Event Identification Register, Non-Extended Mode

B0   **IPF - Interrupt Pending Flag.**
     When this bit is 0, an interrupt is pending.
     When it is 1, no interrupt is pending.

B2-1   **IPR [1-0] - Interrupt Priority**.
     When bit 0 is 0, these bits identify the highest priority pending interrupt.

B3   **RXFT - RX_FIFO Time-out.**
     In the 16450 mode this bit is always 0.
     In the 16550 mode (FIFOs enabled), this bit is set when an RX_FIFO time-out occurred and the associated interrupt is currently the highest priority pending interrupt.

B5-4   **These bits always return 0.**

B7-6   **FEN [1-0]- FIFOs Enabled**.
     These bits are set to 1 when the FIFOs are enabled
     (Bit 0 of FCR set to 1).

www.national.com

EIR bits 3210	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0001	N/A	None	None	N/A
0110	Highest	Line Status	Parity error, or Framing error, or Data overrun, or Break event	Reading the LSR Register
0100	Second	Receiver High-Data-Level Event	Receiver holding register full, or RX_FIFO level equal to or above threshold	Reading the RXD port, or RX_FIFO level drops below threshold
1100	Second	RX_FIFO Time-out	At least 1 character in RX_FIFO, and no character input to or read from the RX_FIFO for 4 character times	Reading the RXD port
0010	Third	Transmitter Low-Data-Level Event	Transmitter holding register or TX_FIFO empty	Reading the EIR register if this interrupt is currently the highest priority pending interrupt, or writing into the TXD port

Table 3-3. Non-Extended Mode Interrupt Priorities

Extended Mode

The EIR register does not return an encoded value like in the non-extended mode. Each bit represents an event flag and is set to 1 when the corresponding event occurred or is pending, regardless of the setting of the corresponding bit in the IER register. Bits 7 (timer interrupt) is cleared when this register is read. Bit 4 is cleared when this register is read if an 8237 type DMA controller is used. All other bits are cleared when the corresponding interrupts are acknowledged.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	TMR_EV	SFIF_EV	TXEMP_EV	DMA_EV	res	LS_EV/ TXHLT_EV	TXLDL_EV	RXHDL_EV
Reset State	0	0	1	0	0	0	1	0

Figure 3-4. Event Identification Register, Extended Mode

B0 **RXHDL_EV - Receiver High-Data-Level Event.**

FIFOs Disabled:
  Set to 1 when one character is in the receiver holding register.

FIFOs Enabled:
  Set to 1 when the RX_FIFO level is equal to or above the threshold level, or an RX_FIFO time-out has occurred.

B1 **TXLDL_EV** - **Transmitter Low-Data-Level Event**.

FIFOs Disabled:
  Set to 1 when the transmitter holding register is empty.

FIFOs Enabled:
  Set to 1 when the TX_FIFO level is below the threshold level.

B2 *UART, Sharp-IR, SIR Modes*
  LS_EV - **Link Status Event**.
  Set to 1 when a receiver error or break condition is reported.
  Note that, when the FIFOs are enabled, the PE, FE and BRK conditions are only reported when the associated character reaches the bottom of the RX_FIFO. An overrun error (OE) is reported as soon as it occurs.

MIR, FIR Modes
  LS_EV/TXHLT_EV - Link Status/Transmitter Halted Event.
  Set to 1 when any of the following conditions occurs:
   1. EOF character reaches the bottom of the RX_FIFO
   2. Receiver overrun
   3. Transmitter under-run
   4. Transmitter halted on frame end

CEIR Mode
  LS_EV/TXHLT_EV - Link Status/Transmitter Halted.
  Set to 1 when a receiver overrun or a transmitter under-run condition occurs.

Note: A high speed CPU can service the interrupt generated by the last frame byte reaching the RX_FIFO bottom before that byte is transferred to memory by the DMA controller. This can happen when the CPU interrupts latency is shorter than the RX_FIFO Time-out (Refer to the 'FIFO Time-outs' section). A DMA request is generated only when the RX_FIFO level reaches the DMA threshold or when a FIFO Time-out occurs, in order to minimize the performance degradation due to DMA signal handshake sequences. If the DMA controller must be set up before receiving each frame, the software in the interrupt routine should make sure that the last byte of the frame just received has been transferred to memory before re-initializing the DMA controller, otherwise that byte could appear as the first byte of the next received frame.

B3   **Reserved.**
Read as 0.

B4   **DMA_EV - DMA Event**.
When an 8237 type DMA controller is used, this bit is set to 1 when a DMA terminal count (TC) is signaled.
It is cleared upon read.

B5   **TXEMP_EV - Transmitter Empty.**
This bit is the same as bit 6 of the LSR register. It is set to 1 when the transmitter is empty.

B6   *MIR, FIR Modes*
SFIF_EV - ST_FIFO Event.
Set to 1 when the ST_FIFO level is equal to or above the threshold, or an ST_FIFO time-out occurs.
This bit is cleared when the CPU reads the
ST_FIFO and its level drops below the threshold.

B7   **TMR_EV - Timer Event.**
Set to 1 when the timer reaches 0.
Cleared by writing 1 into bit 7 of the ASCR register.

FCR - FIFO Control Register Write Only

Used to enable the FIFOs, clear the FIFOs and set the interrupt threshold levels.
Upon reset, all bits are set to 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RXFTH1	RXFTH0	TXFTH1	TXFTH0	res	TXSR	RXSR	FIFO_EN
Reset State	0	0	0	0	0	0	0	0

Figure 3-5. FIFO Control Register

B0   **FIFO_EN - Enable FIFOs.**
When set to 1, both TX_FIFO and RX_FIFO are enabled.
In MIR, FIR and CEIR modes, the FIFOs are always enabled, and the setting of this bit is ignored.

B1   **RXSR - Receiver Soft Reset.**
Writing a 1 to this bit position generates a receiver soft reset, whereby the receiver logic as well as the RX_FIFO
are both cleared.
This bit is automatically cleared by the hardware.

B2   **TXSR - Transmitter Soft Reset.**
Writing a 1 to this bit position generates a transmitter soft reset, whereby the transmitter logic as well as the
TX_FIFO are both cleared.
This bit is automatically cleared by the hardware.

B3   **Reserved.**
Write 0.

B5-4   **TXFTH [1-0] - TX-FIFO Interrupt Threshold**.
In non-extended mode, these bits have no effect, regardless of the values written into them.
In extended mode, these bits select the TX_FIFO interrupt threshold level.
An interrupt is generated when the TX_FIFO level drops below the threshold.

Bits 5-4	TX_FIFO Thresh. (16 Levels)	TX_FIFO Thresh. (32 Levels)
00	1	1
01	3	7
10	9	17
11	13	25

B7-6   RXFTH [1-0] - RX_FIFO Interrupt Threshold.
These bits select the RX_FIFO interrupt threshold level.
An interrupt is generated when the RX_FIFO level is equal to or above the threshold.

Bits 7-6	RX_FIFO Thresh. (16 Levels)	RX_FIFO Thresh. (32 Levels)
00	1	1
01	4	8
10	8	16
11	14	26

3.1.4 LCR/BSR - Link Control/Bank Select Register

These registers share the same address.
The Link Control Register (LCR) is used to select the communications format for data transfers in UART, Sharp-IR and SIR modes.
The Bank select register (BSR) is used to select the register bank to be accessed next.
When the CPU performs a read cycle from this address location, the BSR content is returned. The content of LCR is returned when the CPU reads the SH_LCR register in bank 3.
During CPU write cycles, the setting of bit 7 (BKSE, bank select enable) determines the register to be accessed.
If bit 7 is 0, both LCR and BSR are written into. If bit 7 is 1, only BSR is written into, and LCR is not affected. This prevents the communications format from being spuriously affected when a bank other than bank 0 is accessed. Upon reset, all bits are set to 0.

LCR - Link Control Register

The Format of LCR is shown in figure 3-6.
Bits 0 to 6 are only effective in UART, Sharp-IR and SIR modes.
They are ignored in MIR, FIR and CEIR modes.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1	WLS0
Reset State	0	0	0	0	0	0	0	0

Figure 3-6. Link Control Register

B1-0   WLS [1-0] - Character Length.
These bits specify the length of each transmitted or received serial character.

Bits 10	Character Length
00	5 Bits
01	6 Bits
10	7 Bits
11	8 Bits

B2   STB - Stop Bits.
Number of stop bits in each transmitted serial character. If this bit is 0, 1 stop bit is generated in the transmitted data. If it is 1 and a 5-bit character length is selected via bits 0 and 1, 1.5 stop bits are generated. If it is 1 and a 6, 7 or 8-bit character length is selected, 2 stop bits are generated. The receiver checks 1 stop bit only, regardless of the number of stop bits selected.

B3   PEN - Parity Enable.
When set to 1, parity bits are generated and checked by the transmitter and receiver channels respectively.

B4   EPS - Even Parity.
Used in conjunction with the STKP bit to determine the parity bit.   See encoding below.

B5   STKP - Stick Parity.
The encoding of this and the previous two bits, for control of the parity bit, are as follows:

PEN	EPS	STKP	Selected Parity
0	x	x	none
1	0	0	odd
1	1	0	even
1	0	1	logic 1
1	1	1	logic 0

B6   **SBRK - Set Break**.

When set to 1, the following occurs:

− If UART mode is selected, the SOUT pin is forced to logic 0 state.
− If SIR mode is selected, pulses are issued continuously on the IRTX pin.
− If Sharp-IR mode is selected and internal modulation is enabled, pulses are issued continuously on the IRTX pin.
− If Sharp-IR mode is selected and internal modulation is disabled, the IRTX pin is forced to a logic 1 state.

Setting this bit to 0 disables the break. This bit acts only on the transmitter front-end and has no effect on the rest of the transmitter logic.
The following sequence should be followed to avoid transmission of erroneous characters because of the break.

1. Wait for the transmitter to be empty (TXEMP = 1).
2. Set SBRK to 1
3. Wait for the transmitter to be empty and clear SBRK when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

B7   **BKSE - Bank Select Enable**.
In the LCR register this bit is always 0.

BSR - Bank Select Register

When bit 7 is 1, bits 0-6 of BSR are used to select the bank. The encoding are shown in Table 3-4.

BSR Bits								Selected
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Bank**
0	x	x	x	x	x	x	x	0
1	0	x	x	x	x	x	x	1
1	1	x	x	x	x	1	x	1
1	1	x	x	x	x	x	1	1
1	1	1	0	0	0	0	0	2
1	1	1	0	0	1	0	0	3
1	1	1	0	1	0	0	0	4
1	1	1	0	1	1	0	0	5
1	1	1	1	0	0	0	0	6
1	1	1	1	0	1	0	0	7
1	1	1	1	1	x	0	0	**Reserved**
1	1	0	x	x	x	0	0	**Reserved**

Table 3-4. Bank Selection Encoding

3.1.5 MCR - Mode Control Register

Used to control the device operational mode. The function of this register changes depending upon whether the device is in extended or non-extended mode. In extended mode the interrupt output signal is always enabled. Loop-back can be selected by setting bit 4 of the EXCR1 register. Upon reset, all bits are set to 0.

Non-Extended Mode

The format of the non-extended mode MCR is shown in figure 3-7.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	-	-	-	LOOP	ISEN	res	res	res
Reset State	0	0	0	0	0	0	0	0

Figure 3-7. Mode Control Register, Non-Extended Mode

B0-2   **Reserved.**
Read/Write as 0.

B3   **ISEN - Interrupt Signal Enable**
In normal operation this bit controls the interrupt signal, and it must be set to 1 in order to enable it.
Note: New programs should always keep this bit set to 1 during normal operation. The interrupt signal should be controlled through the device configuration logic.

B4   **LOOP – Loop-back Enable**.
When set to 1, loop-back mode is selected.
This bit accesses the same internal register as bit 4 of the EXCR1 register.
Refer to the section describing the EXCR1 register for more information on the loop-back mode.

B7-5   **Reserved.**
Forced to 0.

Extended Mode

The format of the extended mode MCR is shown in figure 3-8.

Note: Bits 2 to 7 should always be initialized when the operational mode is changed from non-extended to extended.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	MDSL2	MDSL1	MDSL0	IR_PLS	TX_DFR	DMA_EN	res	res
Reset State	0	0	0	0	0	0	0	0

Figure 3-8. Mode Control Register, Extended Mode

B0-1   **Reserved.**
Read/Write as 0.

B2   **DMA_EN - DMA Mode Enable.**
When set to 1, DMA mode of operation is enabled.
When data transfers are performed by a DMA controller transmit and/or receive data interrupts should be disabled to avoid spurious interrupts.
Note that DMA cycles always access the data holding registers or FIFOs, regardless of the selected bank.

B3   **TX_DFR - Transmit Deferral**.
When set to 1, transmit deferral is enabled.
Effective only when the TX_FIFO is enabled.

B4   **IR_PLS - Send Interaction Pulse**.
This bit is effective only in MIR and FIR Modes.
It is set to 1 by writing 1 into it.
Writing 0 into it has no effect.
When set to 1, a 2 µs infrared interaction pulse is transmitted at the end of the frame and the bit is automatically cleared by the hardware.
This bit is also cleared when the transmitter is soft reset.

B7-5   **MDSL [2-0] - Mode Select**.
These bits are used to select the operational mode as shown in Table 3-5.
When the mode is changed, the transmitter and receiver are soft reset.

Bits 7 6 5	Operational Mode
000	**UART**
001	**Reserved**
010	**Sharp-IR**
011	**SIR**
100	**MIR**
101	**FIR**
110	**CEIR**
111	**Reserved**

Table 3-5. UIR Module Operational Modes

3.1.6 LSR - Link Status Register

This register provides status information to the CPU concerning the data transfer.
Bits 1 through 4, and 5 (when in MIR or FIR mode) indicate link status events.
These bits are sticky, and accumulate any conditions occurred since the last time the register was read.
These bits are cleared when any of the following events occurs:

1. Hardware reset.
2. The receiver is soft reset.
3. The LSR register is read.

23

Note: This register is intended for read operations only. Writing to this register is not recommended as it may cause indeterminate results.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function.	ER_INF/ FR_END	TXEMP	TXRDY	BRK/ MAX_LEN	FE/ PHY_ERR	PE/ BAD_CRC	OE	RXDA
Reset State	0	1	1	0	0	0	0	0

Figure 3-9. Link Status Register

B0   **RXDA - Receiver Data Available**.
   Set to 1 when the Receiver Holding Register is full.
   If the FIFOs are enabled, this bit is set when at least one character is in the RX_FIFO.
   Cleared when the CPU reads all the data in the Holding Register or in the RX_FIFO.

B1   *UART, Sharp-IR, SIR, CEIR Modes*
   OE - Overrun Error.
   This bit is set to 1 as soon as the receiver detects an overrun condition.
   Cleared upon read.

   FIFOs Disabled:
     An overrun occurs when a new character is completely received into the receiver front-end section and the CPU has not yet read the previous character in the receiver holding register. The new character is discarded, and the receiver holding register is not affected.

   FIFOs Enabled:
     An overrun occurs when a new character is completely received into the receiver front-end section and the RX_FIFO is full.
     The new character is discarded, and the RX_FIFO is not affected.

   MIR, FIR Modes
   OE - Overrun Error.
   An overrun occurs when a new character is completely received into the receiver front-end section and the RX_FIFO or the ST_FIFO is full.
   The new character is discarded, and the RX_FIFO is not affected.
   Cleared upon read.

B2   *UART, Sharp-IR, SIR Modes*
   PE - Parity Error.
   This bit is set to 1 if the received character did not have the correct parity, as selected by the parity control bits in the LCR register.
   If the FIFOs are enabled, the Parity Error condition will be associated with the particular character in the RX_FIFO it applies to.
   In which case, the PE bit is set when the character reaches the bottom of the RX_FIFO.
   Cleared upon read.

   MIR, FIR Modes
   BAD_CRC - CRC Error.
   Set to 1 when a mismatch between the received CRC and the receiver-generated CRC is detected, and the last byte of the received frame has reached the bottom of the RX_FIFO.
   Cleared upon read.

B3   *UART, Sharp-IR, SIR Modes*
   FE - Framing Error.
   This bit indicates that the received character did not have a valid stop bit.
   It is set to 1 when the stop bit is detected as logic 0.
   If the FIFOs are enabled, the Framing Error condition will be associated with the particular character in the RX_FIFO it applies to.
   In which case, the FE bit is set when the character reaches the bottom of the RX_FIFO.
   After a Framing Error is detected, the receiver will try to re-synchronize.
   If the bit following the stop bit position is 0, the receiver assumes it to be a valid start bit and the next character is shifted in.
   If that bit is 1, the receiver will enter the idle state looking for the next start bit.
   Cleared upon read.

24

MIR Mode

PHY_ERR - Physical Layer Error.
Set to 1 when an abort condition is detected during the reception of a frame, and the last byte of the frame has reached the bottom of the RX_FIFO.
Cleared upon read.

FIR Mode

PHY_ERR - Physical Layer Error.
Set to 1 when an encoding error or the sequence BOF-data-BOF is detected (missing EOF) during the reception of a frame and the last byte of the frame has reached the bottom of the RX_FIFO.
Cleared upon read.

B4 *UART, Sharp-IR, SIR Modes*

BRK - Break Event Detected.
Set to 1 when a sequence of logic 0 bits, equal or longer than a full character transmission, is received.
If the FIFOs are enabled, the Break condition will be associated with the particular character in the RX_FIFO it applies to.
In which case, the BRK bit is set when the character reaches the bottom of the RX_FIFO. When a Break occurs only one zero character is transferred to the receiver holding register or to the RX_FIFO.
The next character transfer takes place after at least one bit (logic 1) is received followed by a valid start bit.
Cleared upon read.

MIR, FIR Modes

MAX_LEN - Maximum Length.
Set to 1 when a frame exceeding the maximum length has been received, and the last byte of the frame has reached the bottom of the RX_FIFO.
Cleared upon read.

B5 **TXRDY - Transmitter Ready**.
This bit is set to 1 when the Transmitter Holding Register or the TX_FIFO is empty.
It is cleared when a data character is written to the TXD port.

B6 **TXEMP - Transmitter Empty**.
Set to 1 when the Transmitter is empty.
The transmitter empty condition occurs when the Holding Register or the TX_FIFO is empty, and the transmitter front-end is idle.

B7 *UART, Sharp-IR, SIR Modes*

ER_INF - Error in RX_FIFO.
Set to 1 when at least one character with a PE, FE or BRK condition is in the RX_FIFO.
This bit is always 0 in 16450 mode.

MIR, FIR Modes

FR_END - Frame End. Set to 1 when the last byte (Frame End byte) of a received frame reaches the bottom of the RX_FIFO.
Cleared upon read.

3.1.7 SPR/ASCR - Scratchpad/Auxiliary Status and Control Register

These registers share the same address.

SPR - Scratchpad Register**.**
This register is accessed when the device is in non-extended mode.
It is to be used by the programmer to hold data temporarily and it has no control the device in any way.

ASCR - Auxiliary Status and Control Register.

This register is accessed when the extended mode of operation is selected.

All the ASCR bits are cleared when hardware reset occurs.

Bits 2 and 6 are cleared when the transmitter is soft reset.

Bits 0, 1, 4 and 5 are cleared when the receiver is soft reset.

The format of ASCR is shown in figure 3-11.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CTE	TXUR	RXBSY/ RXACT	LOST_FR/ RXWDG	TXHFE	S_EOT	EOF_INF	RXF_TOUT
Reset State	0	0	0	0	0	0	0	0

Figure 3-10. Auxiliary Status and Control Register

B0   **RXF_TOUT - RX_FIFO Time-out.**
This bit is read-only, and is set to 1 when an RX_FIFO Time-out occurs.
In MIR or FIR modes this bit can be used in conjunction with bit 1 to determine whether a number of bytes as determined by the RX_FIFO threshold, can be read without checking the RXDA bit in the LSR register for each byte. Cleared when a character is read from the RX_FIFO.

B1   *MIR, FIR Modes*
EOF_INF - EOF Bytes in RX_FIFO.
This bit is read-only, and is set to 1 when one or more EOF bytes are in the RX_FIFO.
Cleared when no EOF byte is in the RX_FIFO.

B2   *MIR, FIR Modes*
S_EOT - Set End of Transmission.
When a 1 is written into this bit position before writing the last character into the TX_FIFO, frame transmission is completed and a CRC + EOF is sent. This bit can be used as an alternative to the Transmitter Frame Length register. If this method is to be used, the FEND_MD bit in the IRCR2 register should be set to 1, or the Transmitter Frame Length register should be set to maximum count.
This bit is automatically cleared by the hardware when a character is written into the TX_FIFO.

CEIR Mode
S_EOT - Set End of Transmission.
When a 1 is written into this bit position before writing the last character into the TX_FIFO, data transmission is gracefully completed. If the CPU simply stops writing data into the TX_FIFO at the end of the data stream, a transmitter under-run is generated and the transmitter stops. In this case, this is not an error, however the software needs to clear the under-run before the next transmission can occur.
 This bit is automatically cleared by the hardware when a character is written into the TX_FIFO.

B3   *MIR, FIR Modes*
TXHFE - Transmitter Halted on Frame End.
This bit is used only when the transmitter frame-end stop mode is selected (TX_MS bit in IRCR2 set to 1).
It is set to 1 by the hardware when transmission of a frame is complete and the TFRCC counter reaching 0 generated the end-of –frame condition.
This bit must be cleared, by writing 1 into it, to re-enable transmission.

B4   *MIR, FIR Modes*
LOST_FR - Lost Frame Flag.
This bit is read-only, and reflects the setting of the lost-frame indicator flag at the bottom of the ST_FIFO.

CEIR Mode
RXWDG - Receiver WATCHDOG.
Set to 1 each time an infrared pulse or the receiver detects pulse-train.
Can be used by the software to detect a receiver idle condition.
Cleared upon read.

B5   *MIR, FIR Modes*
RXBSY - Receiver Busy.
This bit is read-only, and returns a 1 when reception of a frame is in progress.

CEIR Mode
RXACT - Receiver Active.
Set to 1 when an infrared pulse or pulse-train is received. If a 1 is written into this bit position, the bit is cleared and the receiver is deactivated. When this bit is set, the receiver samples the infrared input continuously at the programmed baud rate and transfers the data to the RX_FIFO.

www.national.com

B6   *MIR, FIR, CEIR Modes*

   TXUR - Transmitter Under-run.
   This bit is set to 1 when a transmitter under-run occurs.
   It is always cleared when a mode other than MIR, FIR or CEIR is selected.
   This bit must be cleared, by writing 1 into it, to re-enable transmission.

B7   *MIR, FIR, SIR Modes*
   CTE - Clear Timer Event.

   Writing 1 into this bit position clears the TMR_EV bit in the EIR register. Writing 0 into it has no effect.

3.2 Bank 1

Address Offset	Register Name	Description
0	**LBGDL**	Legacy Baud Generator Divisor Port Low Byte
1	**LBGDH**	Legacy Baud Generator Divisor Port High-Byte
2	**Reserved**	
3	**LCR/BSR**	Link Control/Bank Select Registers
4-7	**Reserved**	

Table 3-6. Bank 1 Register Set

3.2.1 LBGD - Legacy Baud Generator Divisor Port

This port provides an alternate data path to the baud generator divisor register. It is implemented for compatibility with the 16550 and to support existing legacy software packages. New software should use the BGD port in bank 2 to access the baud generator devisor register.   Like the BGD port, LBGD is 16 bits wide and is split into two 8-bit parts, LBGDL and LBGDH, occupying consecutive address locations. A CPU read or write access of the divisor register, through either LBGDL or LBGDH, will affect the device operational mode as follows.

If the device is in extended mode, the device is switched back to 16550-compatibility mode.
In addition to the EXT_SL bit, the following bits are also cleared.

1. Bits 2 to 7 of extended-mode MCR.
2. Bit 5 and 7 of EXCR1.
3. Bits 0 to 5 of EXCR2.
4. Bits 2 and 3 of IRCR1.

 If the device is in non-extended mode and the LOCK bit is 0, the following bits will be cleared.

1. Bits 5 and 7 of EXCR1.
2. Bits 0 to 5 of EXCR2.

If the device is in non-extended mode and the LOCK bit is 1, the content of the divisor register will not be affected and no other action is taken.

3.2.2 LCR/BSR - Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.3 Bank 2

Address Offset	Register Name	Description
0	**BGDL**	Baud Generator Divisor Port Low-Byte
1	**BGDH**	Baud Generator Divisor Port High-Byte
2	**EXCR1**	Extended Control Register 1
3	**LCR/BSR**	Link Control / Bank Select Registers
4	**EXCR2**	Extended Control Register 2
5	**Reserved**	
6	**TXFLV**	TX_FIFO Level
7	**RXFLV**	RX_FIFO Level

Table 3-7. Bank 2 Register Set

3.3.1 BGD - Baud Generator Divisor Port

This port provides the data path to the baud generator divisor register that holds the reload value for the baud generator counter. Divisor values from 1 to 2^{16} - 1 can be used. See Table 3-8. The zero value is reserved and must not be used. The programmed value must be such that the baud generator output clock frequency is sixteen times the desired baud rate value. The baud generator divisor register is 16 bits wide and is split into two independently accessible 8-bit parts. Correspondingly, the BGD port is also 16 bits wide and is split into two 8-bit parts, occupying consecutive address locations. BGDL is located at the lower address and accesses the least significant part of the baud generator divisor register, whereas BGDH is located at the higher address and accesses the most significant part. The baud generator divisor register must be loaded during initialization to ensure proper operation of the baud generator. Upon loading either part of it, the baud generator counter is immediately loaded.

After reset, the content of the baud generator divisor register is indeterminate.

Prescaler Value	13		1.625		1	
Baud Rate	Divisor	%Error	Divisor	%Error	Divisor	%Error
50	2304	0.16%	18461	0.00%	30000	0.00%
75	1536	0.16%	12307	0.01%	20000	0.00%
110	1047	0.19%	8391	0.01%	13636	0.00%
134.5	857	0.10%	6863	0.00%	11150	0.02%
150	768	0.16%	6153	0.01%	10000	0.00%
300	384	0.16%	3076	0.03%	5000	0.00%
600	192	0.16%	1538	0.03%	2500	0.00%
1200	96	0.16%	769	0.03%	1250	0.00%
1800	64	0.16%	512	0.16%	833	0.04%
2000	58	0.53%	461	0.12%	750	0.00%
2400	48	0.16%	384	0.16%	625	0.00%
3600	32	0.16%	256	0.16%	416	0.16%
4800	24	0.16%	192	0.16%	312	0.16%
7200	16	0.16%	128	0.16%	208	0.16%
9600	12	0.16%	96	0.16%	156	0.16%
14400	8	0.16%	64	0.16%	104	0.16%
19200	6	0.16%	48	0.16%	78	0.16%
28800	4	0.16%	32	0.16%	52	0.16%
38400	3	0.16%	24	0.16%	39	0.16%
57600	2	0.16%	16	0.16%	26	0.16%
115200	1	0.16%	8	0.16%	13	0.16%
230400	---	---	4	0.16%	---	---
460800	---	---	2	0.16%	---	---
750000	---	---	---	---	2	0.00%
921600	---	---	1	0.16%	---	---
1500000	---	---	---	---	1	0.00%

Table 3-8. Baud Generator Divisor Settings

3.3.2 EXCR1 - Extended Control Register 1

Used to control the extended mode of operation.
Upon reset all bits are set to 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	BTEST	res	ETDLBK	LOOP	DMASWP	DMATH	DMANF	EXT_SL
Reset State	0	0	0	0	0	0	0	0

Figure 3-11. Extended Control Register 1

B0 **EXT_SL - Extended Mode Select.**
0 => Legacy mode is selected

1 => Extended mode is selected.

When the extended mode is selected, the device architecture changes slightly and a variety of additional features are made available. The interrupt sources are no longer prioritized, and an auxiliary status and control register replaces the scratch pad register. The additional features include transmitter FIFO thresholding, DMA capability, and interrupts on transmitter empty and DMA event.

B1 **DMANF - DMA Fairness Control.**
This bit controls the maximum duration of DMA burst transfers.
0 => DMA requests are forced inactive after approximately 10.5 μs of continuous transmitter and/or receiver DMA operation.
1 => A TX_DMA request is deactivated when the TX_FIFO is full.
An RX_DMA request is deactivated when the RX_FIFO is empty.

B2 **DMATH - DMA Threshold Levels Select.**
This bit selects the TX_FIFO and RX_FIFO threshold levels used by the DMA request logic to support demand transfer mode.
A TX_DMA request is generated when the TX_FIFO level is below the threshold.
An RX_DMA request is generated when the RX_FIFO level reaches the threshold or when an RX_FIFO time-out occurs.

Bit Value	RX_FIFO DMA Thresh.	TX_FIFO DMA Thresh. (16-Levels)	TX_FIFO DMA Thresh. (32- Levels)
0	4	13	29
1	10	7	23

B3 **DMASWP - DMA Swap.**
This bit selects the routing of the DMA control signals between the internal DMA logic and the configuration module. When this bit is 0, the external DMA handshake signals are routed to the internal receiver DMA channel. When it is 1, they are routed to the internal DMA transmitter channel. A block diagram illustrating the control signals routing is given in figure 3-13.

B4 **LOOP – Loop-back Enable**.
When set to 1, loop-back mode is selected.
This bit accesses the same internal register as bit 4 in the MCR register, when the device is in non-extended mode.

Loop-back mode behaves similarly in both non-extended and extended modes.
During loop-back the following occur:

1. The DMA control signals are fully operational.
2. UART input (SIN) and infrared receiver (IRRX1, 2) input pins are disconnected. The internal receiver inputs are connected to the corresponding internal transmitter outputs.
3. The UART transmitter serial output (SOUT) is forced high and the infrared transmitter serial output (IRTX) is forced low, unless the ETDLBK bit is set to 1, In which case they will function normally.

B5 **ETDLBK - Enable Transmitter Output During Loop-back.**
When set to 1, the transmitter serial output is enabled and functions normally when loop-back is selected.

B6 **Reserved**.
Write 1.

B7 **BTEST - Baud Generator Test.**
When set to 1, the output of the baud generator is routed to the ID1/IRSL1 pin.

www.national.com
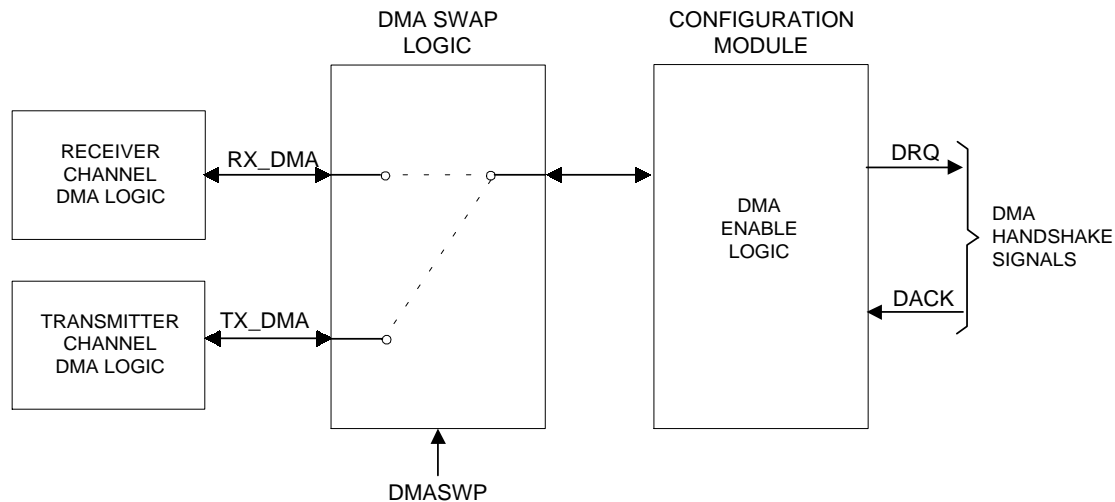
Figure 3-12. DMA Control Signals Routing

3.3.3 LCR/BSR - Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.3.4 EXCR2 - Extended Control Register 2

This register is used to configure the transmitter and receiver FIFOs, and the baud generator prescaler.
Upon reset all bits are set to 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	LOCK	res	PRESL1	PRESL0	RF_SIZ1	RF_SIZ0	TF_SIZ1	TF_SIZ0
Reset State	0	0	0	0	0	0	0	0

Figure 3-13. Extended Control Register 2

B1-0 **TF_SIZ [1-0] - TX_FIFO Levels Select.**
These bits select the number of levels for the TX_FIFO.
They are effective only when the FIFOs are enabled.

Bits 1-0	TX_FIFO Levels
00	16
01	32
1x	Reserved

B3-2 **RF_SIZ [1-0] - RX_FIFO Levels Select.**
These bits select the number of levels for the RX_FIFO.
They are effective only when the FIFOs are enabled.

Bits 3-2	RX_FIFO Levels
00	16
01	32
1x	Reserved

B5-4 **PRESL [1-0] - Prescaler Select**.
The prescaler divides the 24 MHz input clock frequency to provide the clock for the baud generator.

Bits 5-4	Prescaler Value
00	13.0
01	1.625
10	Reserved
11	1.0

B6 **Reserved.**
Read/write 0.

B7   **LOCK - Lock Bit.**

When set to 1, accesses to the baud generator divisor register through LBGDL and LBGDH as well as fallback are disabled from non-extended mode.

In this case two scratchpad registers overlaid with LBGDL and LBGDH are enabled, and any attempted CPU access of the baud generator divisor register through LBGDL and LBGDH will access the scratchpad registers instead. This bit must be set to 0 when extended mode is selected.

3.3.5 TXFLV - TX_FIFO Level, Read Only

This register returns the number of bytes in the TX_FIFO. It can be used for software debugging or during recovery from a transmitter under-run condition in one of the high-speed infrared modes.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	TFL5	TFL4	TFL3	TFL2	TFL1	TFL0
Default	0	0	0	0	0	0	0	0

Figure 3-14. Transmit FIFO Level

B5-0   **TFL [5-0] -** Number of bytes in TX_FIFO.

B7-6   **Reserved.**
Return 0's.

3.3.6 RXFLV - RX_FIFO Level, Read Only

This register returns the number of bytes in the RX_FIFO. It can be used for software debugging.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	RFL5	RFL4	RFL3	RFL2	RFL1	RFL0
Reset State	0	0	0	0	0	0	0	0

Figure 3-15. Receive FIFO Level

B5-0   **RFL [5-0] -** Number of bytes in RX_FIFO.

B7-6   **Reserved.**
Return 0's.

3.4 Bank 3

Address Offset	Register Name	Description
0	**MRID**	Module Identification Register
1	**SH_LCR**	Link Control Register Shadow
2	**SH_FCR**	FIFO Control Register Shadow
3	**LCR/BSR**	Link Control/Bank Select Registers
4 - 7	**Reserved**	

Table 3-9. Bank 3 Register Set

3.4.1 MRID - Module Revision Identification Register, Read Only

When read, it returns the UART and Infrared (UIR) module identification and revision.
The returned value is 3Xh.

3.4.2 SH_LCR - Link Control Register Shadow, Read Only

This register returns the value of the LCR register.
The LCR register is written into when a byte value with bit 7 set to 0 is written to the LCR/BSR registers location (at offset 3) from any bank.

3.4.3 SH_FCR - FIFO Control Register Shadow, Read Only

This register returns the value written into the FCR register in bank 0.

3.4.4 LCR/BSR - Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.5 Bank 4

Address Offset	Register Name	Description
0	**TMRL**	Timer Register Low-Byte
1	**TMRH**	Timer Register High-Byte
2	**IRCR1**	Infrared Control Register 1
3	**LCR/BSR**	Link control/Bank Select registers
4	**TFRLL/ TFRCCL**	Transmitter Frame Length/ Current Count Low Byte
5	**TFRLH/ TFRCCH**	Transmitter Frame Length/ Current Count High Byte
6	**RFRMLL/ RFRCCL**	Receive Frame Maximum Length/ Current Count (Low Byte)
7	**RFRMLH/ RFRCCH**	Receive Frame Maximum Length/ Current Count High Byte

Table 3-10. Bank 4 Register Set

3.5.1 TMR - Timer Register

This register is used to program the reload value for the internal down counter as well as to read the current counter value. TMR is 12 bits wide and is split into two independently accessible parts occupying consecutive address locations. TMRL is located at the lower address and accesses the least significant 8 bits, whereas TMRH is located at the higher address and accesses the most significant 4 bits. Values from 1 to 2^{12} - 1 can be used. The zero value is reserved and must not be used. The upper 4 bits of TMRH are reserved and must be written with 0's. The timer resolution is 125 µs, providing a maximum time-out interval of approximately 0.5 seconds. To properly program the timer, the CPU must always write the lower value into TMRL first and then the upper value into TMRH. Writing into TMRH causes the counter to be loaded. A read of TMR returns the current counter value if the CTEST bit is 0, or the programmed reload value if CTEST is 1. In order for a read access to return an accurate value, the CPU should always read TMRL first, and then TMRH. This is because a read of TMRH returns the content of an internal latch that is loaded with the 4 most significant bits of the current counter value when TMRL is read. After reset, the content of this register is indeterminate.

3.5.2 IRCR1- Infrared Control Register 1

Used to control the timer and counters as well as enable the Sharp-IR or SIR infrared mode in the non-extended mode of operation. Upon reset, all bits are set to 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	res	res	IR_SL1	IR_SL0	CTEST	TMR_EN
Reset State	0	0	0	0	0	0	0	0

Figure 3-16. Infrared Control Register 1

B0   **TMR_EN - Timer Enable, Extended Mode Only**.
           When this bit is 1, the timer is enabled.
           When it is 0, the timer is frozen.

B1   **CTEST - Counters Test.**
           When this bit is set to 1, the TMR register reload value, as well as the TFRL and RFRML register contents are
           returned during CPU reads.

B3-2   IR_SL [1-0] - **SIR or Sharp-IR Select, Non-Extended Mode Only.**
These bits are used to select the appropriate infrared mode when the device is in non-extended mode.
They are ignored when extended mode is selected.

Bits 3-2	Selected Mode
00	UART
01	Reserved
10	Sharp-IR
11	SIR

B7-4   Reserved.
Write as 0's.

3.5.3 LCR/BSR - Link Control/Bank Select Registers

These Registers are the same as in bank 0.

3.5.4 TFRL/TFRCC - Transmitter Frame-Length/Current-Count

These registers share the same addresses. TFRL is always accessed during write cycles and is used to program the frame length, in bytes, for the frames to be transmitted. The frame length value does not include any appended CRC bytes. TFRL is accessed during read cycles if the CTEST bit is set to 1, and returns the previously programmed value. Values from 1 to 2^{13} - 1 can be used. The zero value is reserved and must not be used. TFRCC is loaded with the content of TFRL when transmission of a frame begins, and decrement after each byte is transmitted. It is read-only and is accessed during CPU read cycles when the CTEST bit is 0. It returns the number of currently remaining bytes of the frame being transmitted. These registers are 13 bits wide and are split into two independently accessible parts occupying consecutive address locations. TFRLL and TFRCCL are located at the lower address and access the least significant 8 bits, whereas TFRLH and TFRCCH are located at the higher address and access the most significant 5 bits. To properly program TFRL, the CPU must always write the lower value into TFRLL first and then the upper value into TFRLH. The upper 3 bits of TFRLH are reserved and must be written with 0's. In order for a read access of TFRCC to return an accurate value, the CPU should always read TFRCCL first, and then TFRCCH. After reset, the content of the TFRL register is 800h.

3.5.5 RFRML/RFRCC - Receiver Frame Maximum-Length/Current-Count

These registers share the same addresses. RFRML is always accessed during write cycles and is used to program the maximum frame length, in bytes, for the frames to be received. The maximum frame length value includes the CRC bytes. RFRML is accessed during read cycles if the CTEST bit is set to 1, and returns the previously programmed value. Values from 4 to 2^{13} - 1 can be used. The values from 0 to 3 are reserved and must not be used. RFRCC holds the current byte count of the incoming frame, and an increment after each byte is received. It is read-only and is accessed during CPU read cycles when the CTEST bit is 0. These registers are 13 bits wide and are split into two independently accessible parts occupying consecutive address locations. RFRMLL and RFRCCL are located at the lower address and access the least significant 8 bits, whereas RFRMLH and RFRCCH are located at the higher address and access the most significant 5 bits. To properly program RFRML, the CPU must always write the lower value into RFRMLL first and then the upper value into RFRMLH. The upper 3 bits of RFRMLH are reserved and must be written with 0's. In order for a read access of RFRCC to return an accurate value, the CPU should always read RFRCCL first, and then RFRCCH.   After reset, the content of the RFRML register is 800h.

Note: TFRCC and RFRCC are intended for testing purposes only. Use of these registers for any other purpose is not
        recommended.

3.6 Bank 5

Address Offset	Register Name	Description
0-2	**Reserved**	
3	**LCR/BSR**	Link Control/Bank Select Registers
4	**IRCR2**	Infrared Control Register 2
5	**FRM_ST**	Frame Status
6	**RFRLL/ LSTFRC**	Received Frame Length Low-Byte / Lost Frame Count
7	**RFRLH**	Received Frame Length High Byte

Table 3-11. Bank 5 Register Set

3.6.1 LCR/BSR - Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.6.2 IRCR2 - Infrared Control Register 2

Upon reset, the content of this register is 02h.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	SFTSL	FEND_MD	AUX_IRRX	TX_MS	MDRS	res	IR_FDPLX
Reset State	0	0	0	0	0	0	1	0

Figure 3-17. Infrared Control Register 2

B0   **IR_FDPLX - Infrared Full Duplex Mode.**
          When set to 1, the infrared receiver is not masked during transmission.

B1   **Reserved.**
          Read/Write as 1.

B2   **MDRS - MIR Data Rate Select.**
          This bit determines the data rate in MIR mode.
          0 => 1.152 Mbps
          1 => 0.576 Mbps

B3   **TX_MS - Transmitter Mode Select**.
          This bit is used in MIR and FIR modes only.
          When it is set to 1, transmitter frame-end stop mode is selected.
          In this case the transmitter stops after transmission of a frame is complete, if the TFRCC counter reaching 0
          generated the end-of-frame condition.
          Clearing the TXHFE bit in the ASCR register can restart the transmitter.

B4   **AUX_IRRX – Auxiliary Infrared Input Select.**
          When set to 1, the infrared signal is received from the auxiliary input. See Table 3-17.

B5   **FEND_MD - Frame End Control**.
          This bit selects whether a terminal-count condition from the
          TFRCC register will generate an EOF in PIO mode or DMA mode.
          0 => TFRCC terminal count effective in PIO mode.
          1 => TFRCC terminal count effective in DMA mode.

B6   **SFTSL - ST_FIFO Threshold Select.**
          An interrupt request is generated when the ST_FIFO level reaches the threshold or when an ST_FIFO timeout
          occurs.

Bit Value	**Threshold Level**
0	2
1	4

B7   **Reserved.**
          Read/write 0.

3.6.3 ST_FIFO - Status FIFO

The ST_FIFO is used in MIR and FIR Modes.
It is an 8-level FIFO and is intended to support back-to-back incoming frames in DMA mode, when an 8237-type DMA controller
is used. Each ST_FIFO entry contains both status information and frame length for a single frame, or the number of lost frames.
The bottom entry spans three address locations, and is accessed via the FRM_ST, RFRLL/LSTFRC and RFRLH registers. The
ST_FIFO is flushed when a hardware reset occurs or when the receiver is soft reset.

Note: The status and length information of received frames is loaded into the ST_FIFO whenever the DMA_EN bit in the
          extended-mode MCR register is set to 1 and an 8237 type DMA controller is used. It is done regardless of whether the
          CPU or the DMA controller is transferring the data from the RX_FIFO to memory. This implies that, during testing, if
          full duplex is enabled and a DMA channel is servicing the transmitter while the CPU is servicing the receiver, the CPU
          must still read the ST_FIFO otherwise it fills up and incoming frames will be rejected.

3.6.3.1 FRM_ST - Frame Status Byte at ST_FIFO Bottom, Read Only

This register returns the status byte at the bottom of the ST_FIFO. If the LOST_FR bit is 0, bits 0 to 4 indicate if any error condition occurred during reception of the corresponding frame. Error conditions will also affect the error flags in the LSR register.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	VLD	LOST_FR	Res	MAX_LEN	PHY_ERR	BAD_CRC	OVR1	OVR2
Reset State	0	0	0	0	0	0	0	0

Figure 3-18. Frame Status Byte

B0 **OVR2 - Overrun Error 2.**
This bit is set to 1 when incoming characters or entire frames have been discarded due to the ST_FIFO being full.

B1 **OVR1 - Overrun Error 1.**
This bit is set to 1 when incoming characters or entire frames have been discarded due to the RX_FIFO being full.

B2 **BAD_CRC** - **CRC Error.**
Set to 1 when a mismatch between the received CRC and the receiver-generated CRC is detected.

B3 **PHY_ERR - Physical Layer Error.**
Set to 1 when an encoding error or the sequence BOF-data-BOF is detected in FIR mode or an abort condition is detected in MIR mode.

B4 **MAX_LEN - Maximum Frame Length Exceeded.**
Set to 1 when a frame exceeding the maximum length has been received.

B5 **Reserved**.
Returned data is indeterminate.

B6 **LOST_FR** - **Lost Frame Indicator Flag.**
Indicates the type of information provided by this ST_FIFO entry.

0 => Entry provides status information and length for a received frame.
1 => Entry provides overrun indications and number of lost frames.

B7 **VLD** - **ST_FIFO Entry Valid.**
When set to 1, the bottom ST_FIFO entry contains valid data.

3.6.3.2 RFRL(L)/LSTFRC - Received Frame Length /Lost-Frame-Count at ST_FIFO Bottom, Read Only

This register should be read only when the VLD bit in FRM_ST is 1. The information returned depends on the setting of the LOST_FR bit. Upon reset, all bits are set to 0.

LOST_FR = 0 => Least significant 8 bits of the received frame length.
LOST_FR = 1 => Number of lost frames

3.6.3.3 RFRL(H) - Received-Frame-Length at ST_FIFO Bottom, Read Only

This register should be read only when the VLD bit in FRM_ST is 1. The information returned depends on the setting of the LOST_FR bit. Upon reset, all bits are set to 0.

LOST_FR = 0 => Most significant 5 bits of the received frame length.
LOST_FR = 1 => All 0's

Reading this register removes the bottom ST_FIFO entry.

3.7 Bank 6

Address Offset	Register Name	Description
0	**IRCR3**	Infrared Control Register 3
1	**MIR_PW**	MIR Pulse Width Register
2	**SIR_PW**	SIR Pulse Width Register
3	**LCR/BSR**	Link Control/Bank Select Registers
4	**BFPL**	Beginning Flags/Preamble Length Register
5-7	**Reserved**	

Table 3-12. Bank 6 Register Set

3.7.1 IRCR3 - Infrared Control Register 3

Used to select the operating mode of the infrared interface.
Upon reset, the content of this register is 20h.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SHDM_DS	SHMD_DS	FIR_CRC	MIR_CRC	res	TXCRC_INV	TXCRC_DS	res
Reset State	0	0	1	0	0	0	0	0

Figure 3-19. Infrared Control Register 3

B0   **Reserved.**
Write 0.

B1   **TXCRC_DS** - **Disable Transmitter CRC.**
When set to 1, a CRC is not transmitted.

B2   **TXCRC_INV** - **Invert Transmitter CRC.**
When set to 1, an inverted CRC is transmitted.

B3   **Reserved.**
Write 0.

B4   **MIR_CRC** - **MIR Mode CRC Select.**
Determines the length of the CRC in MIR mode.
0 => 16 bit CRC
1 => 32 bit CRC

B5   **FIR_CRC - FIR Mode CRC Select.**
Determines the length of the CRC in FIR mode.
0 => 16-bit CRC
1 => 32-bit CRC

B6   **SHMD_DS** - **Sharp-IR Modulation Disable**.
When set to 1, internal 500 kHz transmitter modulation is disabled.

B7   **SHDM_DS - Sharp-IR Demodulation Disable.**
When set to 1, internal 500 kHz receiver demodulation is disabled.

3.7.2 MIR_PW - MIR Pulse Width Register

This register is used to program the width of the transmitted MIR infrared pulses in increments of either 20.833 ns or 41.666 ns depending on the setting of the MDSR bit in the IRCR2 register.
The programmed value has no effect on the MIR receiver. After reset, the content of this register is 0Ah.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	Res	res	MPW3	MPW2	MPW1	MPW0
Reset State	0	0	0	0	1	0	1	0

Figure 3-20. MIR Pulse Width Register

B3-0   MPW [3-0] - MIR Signal Pulse Width

Encoding	Pulse Width, MDRS = 0	Pulse Width, MDRS = 1
00XX	Reserved	Reserved
0100	83.3 ns	166.6 ns
0101	104.1 ns	208.3 ns
0110	125.0 ns	250.0 ns
0111	145.8 ns	291.6 ns
1000	166.6 ns	333.3 ns
1001	187.5 ns	374.9 ns
1010	208.3 ns	416.6 ns
1011	229.1 ns	458.3 ns
1100	250.0 ns	500.0 ns
1101	270.8 ns	541.6 ns
1110	291.6 ns	583.3 ns
1111	312.5 ns	625.0 ns

B7-4   Reserved.
Write 0's.

3.7.3 SIR_PW - SIR Pulse Width Register

This register determines the width of the transmitted SIR infrared pulses.
The programmed value has no effect on the SIR receiver. After reset, the content of this register is 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	Res	res	SPW3	SPW2	SPW1	SPW0
Reset State	0	0	0	0	0	0	0	0

Figure 3-21. SIR Pulse Width Register

B3-0   SPW [3-0] - SIR Signal Pulse Width.

Encoding	Pulse Width
0000	3/16 of bit time
1101	1.6 μs

Other encoding are reserved.

B7-4   Reserved.
Write 0's**.**

3.7.4 LCR/BSR - Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.7.5 BFPL - Beginning Flags/Preamble Length Register

Used to program the number of beginning flags and the preamble for MIR and FIR modes respectively.
After reset, the content of this register is 2Ah.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	MBF3	MBF2	MBF1	MBF0	FPL3	FPL2	FPL1	FPL0
Reset State	0	0	1	0	1	0	1	0

Figure 3-22. Beginning Flags/Preamble Length Register

B3-0   FPL [3-0] - FIR Preamble Length.
Selects the number of preamble symbols for FIR frames.

Encoding	Preamble Length
0000	Reserved
0001	1
0010	2
0011	3
0100	4

www.national.com

Encoding	Preamble Length
0101	5
0110	6
0111	8
1000	10
1001	12
1010	16
1011	20
1100	24
1101	28
1110	32
1111	Reserved

B7-4   MBF [3-0] - MIR Beginning Flags.
Selects the number of beginning flags for MIR frames.

Encoding	Beginning Flags
0000	Reserved
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	8
1000	10
1001	12
1010	16
1011	20
1100	24
1101	28
1110	32
1111	Reserved

3.8 Bank 7

Address Offset	Register Name	Description
0	**IRRXDC**	Infrared Receiver Demodulator Control
1	**IRTXMC**	Infrared Transmitter Modulator Control
2	**RCCFG**	CEIR Configuration
3	**LCR/BSR**	Link Control/Bank Select Registers
4	**IRCFG1**	Infrared Interface Configuration Register 1
5	**Reserved**	
6	**Reserved**	
7	**IRCFG4**	Infrared Interface Configuration Register 4

Table 3-13. Bank 7 Register Set

3.8.1 IRRXDC - Infrared Receiver Demodulator Control Register

After reset, the content of this register is 29h, selecting a frequency range from 34.61 to 38.26 kHz for the CEIR mode, and from 480.0 to 533.3 kHz for Sharp-IR mode. The value of this register is ignored if receiver demodulation for both Sharp-IR and CEIR mode is disabled. The available frequency ranges for CEIR and Sharp-IR modes are given in Tables 3-14 through 3-16.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	DBW2	DBW1	DBW0	DFR4	DFR3	DFR2	DFR1	DFR0
Reset State	0	0	1	0	1	0	0	1

Figure 3-23. Infrared Receiver Demodulator Control Register

B4-0 **DFR [4-0]** - **Demodulator Frequency**.
These bits determine the subcarrier' center frequency for the CEIR mode.

B7-5 **DBW [2-0]** - **Demodulator Bandwidth**.
These bits determine the demodulator bandwidth within which the subcarrier signal frequency has to fall in order for the signal to be accepted.
Used for both Sharp-IR and CEIR modes.

DBW [2-0] bits											
001		010		011		100		101		110	
DFR [4 - 0] min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	min.	max.
00011 28.6	31.6	27.3	33.3	26.1	35.3	25.0	37.5	24.0	40.0	23.1	42.9
00100 29.3	32.4	28.0	34.2	26.7	36.2	25.6	38.4	24.6	41.0	23.7	43.9
00101 30.1	33.2	28.7	35.1	27.4	37.1	26.3	39.4	25.2	42.1	24.3	45.1
00110 31.7	35.1	30.3	37.0	29.0	39.2	27.8	41.7	26.7	44.4	25.6	47.6
00111 32.6	36.0	31.1	38.1	29.8	40.3	28.5	42.8	27.4	45.7	26.3	48.9
01000 33.6	37.1	32.0	39.2	30.7	41.5	29.4	44.1	28.2	47.0	27.1	50.4
01001 34.6	38.3	33.0	40.4	31.6	42.8	30.3	45.4	29.1	48.5	28.0	51.9
01011 35.7	39.5	34.1	41.7	32.6	44.1	31.3	46.9	30.0	50.0	28.8	53.6
01100 36.9	40.7	35.2	43.0	33.7	45.5	32.3	48.4	31.0	51.6	29.8	55.3
01101 38.1	42.1	36.4	44.4	34.8	47.1	33.3	50.0	32.0	53.3	30.8	57.1
01111 39.4	43.6	37.6	45.9	36.0	48.6	34.5	51.7	33.1	55.1	31.8	59.1
10000 40.8	45.1	39.0	47.6	37.3	50.4	35.7	53.6	34.3	57.1	33.0	61.2
10010 42.3	46.8	40.4	49.4	38.6	52.3	37.0	55.6	35.6	59.3	34.2	63.5
10011 44.0	48.6	42.0	51.3	40.1	54.3	38.5	57.7	36.9	61.5	35.5	65.9
10101 45.7	50.5	43.6	53.3	41.7	56.5	40.0	60.0	38.4	64.0	36.9	68.6
10111 47.6	52.6	45.5	55.6	43.5	58.8	41.7	62.5	40.0	66.7	38.5	71.4
11010 49.7	54.9	47.4	57.9	45.3	61.4	43.5	65.2	41.7	69.5	40.1	74.5
11011 51.9	57.4	49.5	60.6	47.4	64.1	45.4	68.1	43.6	72.7	41.9	77.9
11101 54.4	60.1	51.9	63.4	49.7	67.2	47.6	71.4	45.7	76.1	43.9	81.6

Table 3-14. CEIR Low-Speed Demodulator Frequency Ranges in kHz (RXHSC = 0)

DBW [2-0] bits											
001		010		011		100		101		110	
DFR [4-0] min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	min.	max.
00011 381.0	421.1	363.6	444.4	347.8	470.6	333.3	500.0	320.0	533.3	307.7	571.4
01000 436.4	480.0	417.4	505.3	400.0	533.3	384.0	564.7	369.2	600.0	355.6	640.0
01011 457.7	505.3	436.4	533.3	417.4	564.7	400.0	600.0	384.0	640.0	369.9	685.6

Table 3-15. CEIR High-Speed Demodulator Frequency Ranges in kHz (RXHSC=1)

DBW [2-0] bits											
001		010		011		100		101		110	
DFR [4-0] min.	Max.	min.	max.	min.	max.	min.	max.	min.	max.	min.	max.
xxxxx 480.0	533.3	457.1	564.7	436.4	600.0	417.4	640.0	400.0	685.6	384.0	738.5

Table 3-16. Sharp-IR Demodulator Frequency Ranges in kHz

3.8.2 IRTXMC - Infrared Transmitter Modulator Control Register

Used to select the modulation sub-carrier parameters for CEIR and Sharp-IR modes. For Sharp-IR, only the sub-carrier pulse width is controlled by this register, the sub-carrier frequency is fixed at 500 kHz.
After reset, the content of this register is 69h, selecting a sub-carrier frequency of 36 kHz and a pulse width of 7 µs for CEIR, or a pulse width of 0.8 µs for Sharp-IR.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	MCPW2	MCPW1	MCFW0	MCFR4	MCFR3	MCFR2	MCFR1	MCFR0
Reset State	0	1	1	0	1	0	0	1

Figure 3-24. Infrared Transmitter Modulator Control Register

B4-0   MCFR [4-0] - Modulation Sub-carrier Frequency.
Selects the frequency for the CEIR modulation sub-carrier.

Encoding	Low Frequency, TXHSC = 0	High Frequency, TXHSC = 1
00000	Reserved	Reserved
00001	Reserved	Reserved
00010	Reserved	Reserved
00011	30 kHz	400 kHz
00100	31 kHz	Reserved
00101	32 kHz	Reserved
00110	33 kHz	Reserved
00111	34 kHz	Reserved
01000	35 kHz	450 kHz
01001	36 kHz	Reserved
01010	37 kHz	Reserved
01011	38 kHz	480 kHz
01100	39 kHz	Reserved
01101	40 kHz	Reserved
01110	41 kHz	Reserved
01111	42 kHz	Reserved
10000	43 kHz	Reserved
10001	44 kHz	Reserved
10010	45 kHz	Reserved
10011	46 kHz	Reserved
10100	47 kHz	Reserved
10101	48 kHz	Reserved
10110	49 kHz	Reserved
10111	50 kHz	Reserved
11000	51 kHz	Reserved
11001	52 kHz	Reserved
11010	53 kHz	Reserved
11011	54 kHz	Reserved
11100	55 kHz	Reserved
11101	56 kHz	Reserved
11110	56.9 kHz	Reserved
11111	Reserved	Reserved

B7-5   MCPW [2-0] - Modulation Sub-carrier Pulse Width.

Encoding	Low Frequency, TXHSC = 0 (CEIR only)	High Frequency, TXHSC = 1 (CEIR or Sharp-IR)
000	Reserved	Reserved
001	Reserved	Reserved
010	6 µs	0.7 µs
011	7 µs	0.8 µs
100	9 µs	0.9 µs
101	10.6 µs	1.0 µs
110	Reserved	Reserved
111	Reserved	Reserved

3.8.3 RCCFG - CEIR Configuration Register

This register controls the basic operation of the CEIR mode.
After reset, all bits are set to 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	R_LEN	T_OV	RXHSC	RCDM_DS	res	TXHSC	RC_MMD1	RC_MMD0
Reset State	0	0	0	0	0	0	0	0

Figure 3-25. CEIR Configuration Register

B1-0   RC_MMD [1-0] - Transmitter Modulation Mode.
Determines how infrared pulses are generated from the transmitted bit string.

   00 =>   C_PLS Modulation Mode.
               Pulses are generated continuously for the entire logic 0 bit time
   01 =>   8_PLS Modulation Mode.
               8 pulses are generated each time one or more logic 0 bits are transmitted following logic 1 bit.
   10 =>   6_PLS Modulation Mode.
               6 pulses are generated each time one or more logic 0 bits are transmitted following logic 1 bit.
   11 =>   Reserved.
               Result is indeterminate.

B2   TXHSC - Transmitter Sub-carrier Frequency Select.
Selects the frequency range for the modulation carrier.
   0   => 30 - 56.9 kHz
   1   => 400 - 480 kHz

B3   Reserved.
Write 0.

B4   RCDM_DS - **Receiver Demodulation Disable.**
When this bit is 1, the internal demodulator is disabled. The internal demodulator, when enabled, performs carrier frequency checking and envelope generation.
It must be disabled when demodulation is done externally, or when over-sampling mode is used to determine the carrier frequency.

B5   RXHSC - Receiver Carrier Frequency Select.
Selects the frequency range for the receiver demodulator.
   0   => 30 - 56.9 kHz
   1   => 400 - 480 kHz

B6   T_OV - Receiver Sampling Mode.
   0   => Programmed-T-period sampling.
   1   => Over-sampling Mode.

B7   R_LEN - **Run-Length Control.**
When set to 1, run-length encoding/decoding is enabled.
The format of a run-length code is YXXXXXXX, where:
 Y - Bit value
XXXXXXX - Number of bits minus 1.
            (Selects 1 to 128 bits).

3.8.4 LCR/BSR - Link Control/Bank Select Registers

These registers are the same as in bank 0.

3.8.5 IRCFG1, 4 - Infrared Interface Configuration Registers

Two registers are provided to configure the infrared interface. These registers are used to select the infrared receiver inputs as well as the transceiver operational mode. Selection of the transceiver mode is accomplished by up to two special output signals (ID/IRSL [1-0]). When these signals are programmed as outputs, they will be forced low when the UART mode is selected.

3.8.5.1 IRCFG1 - Infrared Interface Configuration Register 1

This register is used to directly control the transceiver operational mode. It is also used to read the identification data of a infrared adapter.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	STRV_MS	res	Res	res	res	res	IRIC1	IRIC0
Reset State	0	0	0	0	0	0	X	X

Figure 3-26. Infrared Configuration Register 1

B0   **IRIC0 - Transceiver Identification/Control.**
The function of this bit depends on whether the ID0/IRSL0/IRRX2 pin is programmed as input or as an output.

ID0/IRSL0/IRRX2 Pin Programmed as Input (IRSL0_DS = 0).
  Upon read, this bit returns the logic level of the pin.
  Data written into this bit position is ignored.

ID0/IRSL0/IRRX2 Pin Programmed as Output (IRSL0_DS = 1).
  This bit will drive the ID0/IRSL0/IRRX2 pin regardless of the selected mode.
  Upon read, this bit returns the value previously written.

B1   **IRIC1 - Transceiver Identification/Control**
The function of this bit depends on whether the ID1/IRS1 pin is programmed as input or as output.

ID1/IRSL1 Pin Programmed as Input (IRSL1_DS = 0).
  Upon read, this bit returns the logic level of the pin.
  Data written into this bit position is ignored.

ID1/IRSL1 Pin Programmed as Output (IRSL1_DS = 1).
  This bit will drive the ID1/IRSL1 pin regardless of the selected mode.
  Upon read, this bit returns the value previously written.

B2-6   **Reserved.**
Read/Write as 0.

B7   **STRV_MS** - **Special Transceiver Mode Select**.
This bit is used to select the operational mode in some optical transceiver modules. When this bit is set to 1, the IRTX output is forced high and a timer is started.
The timer times out after approximately 64 us, at which time the bit is reset and IRTX returns low. The timer is restarted every time a 1 is written into this bit position. Therefore, the time in which IRTX is forced high can be extended beyond 64 us.
This should be avoided, however, to prevent damage to the transmitter LED.
Writing 0 into this bit position has no effect.

3.8.5.2 IRCFG4 - Infrared Interface Configuration 4

This register is used to configure the receiver data path and enable the selection of the configuration pins.
After reset, the content of this register is 0.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	IRRX_MD	IRSL0_DS	RXINV	IRSL1_DS	res	res	res
Reset State	0	0	0	0	0	0	0	0

Figure 3-27. Infrared Configuration Register 4

B2-0   **Reserved.**
Read/write 0's.

B3   **IRSL1_DS - ID1/IRSL1 Pin's Direction Select.**
This bit determines the direction of the ID1/IRSL1 pin.

0 => Pin's direction is input.
1 => Pin's direction is output.

B4   **RXINV - IRRX Signal Invert**.
This bit is provided in order to support optical transceivers with receive signals of opposite polarity (active high instead of active low).
When set to 1, an inverter is placed on the receiver input signal path.

B5   **IRSL0_DS - ID0/IRSL0/IRRX2 Pin Direction Select.**
This bit determines the direction of the ID0/IRSL0/IRRX2 pin.

0 => Pin's direction is input.
1 => Pin's direction is output.

B6   **IRRX_MD** - **IRRX Mode Select**.
Determines whether a single input or two separate inputs are used for Low-Speed and High-Speed IrDA modes.

   0 => One input is used for both SIR and MIR/FIR.
   1 => Separate inputs are used for SIR and MIR/FIR.

Table 3-17 shows the IRRXn pins used in the PC87109 for the low-speed and high-speed infrared modes, and for the various combinations of IRSL0_DS, IRRX_MD and AUX_IRRX.

B7   **Reserved.**
Read/Write as 0.

IRSLO_DS	IRRX_MD	AUX_IRRX	HIS_IR	IRRXn
0	0	0	X	IRRX1
0	0	1	X	IRRX2
0	1	X	0	IRRX1
0	1	X	1	IRRX2
1	X	X	X	IRRX1

Table 3-17. Infrared Receiver Input Selection

(HIS_IR = 1 when selected mode is MIR or FIR)

43

4.0 Device Configuration

4.1 Overview

On power-up or after a hardware reset, the PC87109 will have all of its modules and functions disabled.

The ID/IRSL [1-0] pins are in input mode. The IRTX and the UART output pin are set to their inactive state. Before normal operation can be started, the device must be enabled and several items must be configured. These include the enabling and polarity selection of the interrupt and DMA control signals.

Additional items, related to the communications protocols and the infrared transceiver interface, are configured via appropriate registers in the UIR module register set.

4.2 Configuration Registers

Three registers are provided to control the basic configuration. One additional register is provided for device identification.

The PC87109 has a linear address space. The selected register bank occupies address locations at offsets 0 to 7. The configuration registers are accessible at offsets 08h to 0Dh. A total of 12 locations are used. The four locations at offsets 0Bh, 0Ch, 0Eh and 0Fh are reserved.

The configuration registers and their corresponding offset values are shown in Table 4.1. A description of these registers is provided in the following sections.

Offset	Register	Description
08h	**CSCFG**	Control Signals Configuration Register
09h	**CSEN**	Control Signals Enable Register
0Ah	**MCTL**	Mode Control Register
0Bh	**Reserved**	
0Ch	**Reserved**	
0Dh	**DID**	Device Identification Register
0Eh	**Reserved**	
0Fh	**Reserved**	

Table 4-1. Configuration Registers

4.2.1 CSCFG – Control Signals Configuration Register (offset = 08h)

This register controls the configuration of the IRQ and DMA handshake signals as well as the selection of the register banks.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	TCINV	DACKINV	DRQINV	IRQBC	IRQINV	EN_BNK	res	res
Reset State	0	0	0	0	0	0	0	0

Figure 4-1. Control Signals Configuration Register

B1-0 **Reserved**.
Read/write as 0.

B2 **EN_BNK -- Enable Register Banks**.
When set to 1, any bank from 0 to 7 can be selected.
When this bit is cleared, only banks 0 and 1 can be selected, and any attempt to select banks 2 to 7 is ignored.

B3 **IRQINV** – **IRQ Polarity Invert.**
When set to 1, the IRQ output signal polarity is inverted.

Value	IRQ Signal
0	Active High
1	Active Low

B4   **IRQBC -- IRQ Output Buffer Configuration**.
This bit determines whether the IRQ output buffer is configured as Open Drain or Totem Pole.

Value	Output Buffer Type
0	Open Drain
1	Totem Pole

B5   **DRQINV** – **DRQ Polarity Invert.**
When set to 1, the DRQ output signal polarity is inverted.

Value	DRQ Signal
0	Active High
1	Active Low

B6   **DACKINV** – **DACK Polarity Invert.**
When set to 1, the DACK input signal polarity is inverted.

Value	DRQ Signal
0	Active Low
1	Active High

B7   **TCINV** – **TC Polarity Invert.**
When set to 1, the TC input signal polarity is inverted.

Value	TC Signal
0	Active High
1	Active Low

4.2.2 CSEN - Control Signals Enable Register (offset = 09h)

This register is used to enable the Interrupt output signal, and the DMA control signals for the device's receiver and transmitter communication channels.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	res	res	DCH_EN	res	res	IRQ_EN
Reset State	0	0	0	0	0	0	0	0

Figure 4-2. Control Signals Enable Register

B0   **IRQ_EN -- IRQ Signal Enable.**
When this bit is set to 1, the interrupt output signal is enabled.
After reset, this bit is cleared, and the IRQ output pin is in TRI-STATE condition.

B1-2   **Reserved.**
Read/Write as 0.

B3   **DCH_EN -- DMA Control Signals Enable.**
When this bit is set to 1, the DMA control signals are enabled and are routed to either the internal receiver or the internal transmitter DMA channel depending on the setting of the DMASWP bit in the EXCR1 register.
After reset, this bit is cleared, and the DMA control signals are disabled; DRQ is floated, DACK and TC are blocked.

B4-7   **Reserved.**
Read/Write as 0.

4.2.3 MCTL - Mode Control Register (offset = 0Ah)

This register is used to enable the device and select the power mode.
It also returns the device's busy/Idle state.

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	res	res	Res	res	res	BUSY	NOM	DEV_EN
Reset State	0	0	0	0	0	0	0	0

Figure 4-3. Mode Control Register

www.national.com

B0　　**DEV_EN -- Device Enable.**
When set to 1, the device is enabled.
When this bit is 0, the device is disabled and the following occurs:

   1. All internal modules are powered down.
   2. Accesses to the UIR module registers are inhibited, and the bus is not driven during reads.
   3. UART interface output is set to its inactive state.
   4. UART interface input is blocked.
   5. ID/IRSL[1-0] pins programmed as outputs are not affected.
   6. ID/IRSL[1-0] pins programmed as inputs are blocked.
   7. IRTX is set to its inactive state.
   8. IRRXn inputs are blocked.
   9. IRQ and DMA control outputs are floated.
   10. DMA control inputs are blocked
   11. Bus interface signals are fully functional.
   12. All the register contents are maintained.

B1　　**NOM -- Normal Operating Mode.**
This bit must be set to 1 for normal operation. When this bit is 0, the device is in low power mode and the following occurs:

   1. All internal modules are powered down.
   2. Accesses to all the device's internal registers are handled normally.
   3. UART interface output is set to its inactive state.
   4. UART interface input is blocked.
   5. ID/IRSL[1-0] pins programmed as outputs are not affected.
   6. ID/IRSL[1-0] pins programmed as inputs are blocked.
   7. IRTX is set to its inactive state.
   8. IRRXn inputs are blocked.
   9. The IRQ output is fully functional.
   10. The DMA control output (if enabled) is set to its inactive state.
   11. DMA control inputs are blocked.
   12. Bus interface signals are fully functional.
   13. All the register contents are maintained.

B2　　**BUSY -- Busy Status.**
This bit is read-only. It is set to 1 whenever a data transfer/receive is in progress. The power management software can use this bit in order to determine when the device can be shut down.

B3-7　　**Reserved.**
Write as 0's.

4.2.4 DID - Device Identification Register (offset = 0Dh)

This is a read-only register. When read, it returns the PC87109 identification and revision.
The returned value is 2Xh.

5.0 Device Specifications

5.1 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	-0.5V to + 7.0V
Input Voltage (V_I)	-0.5 to V_{DD} + 0.5V
Output Voltage (V_o)	-0.5 to V_{DD} + 0.5V
Storage Temperature (T_{STG})	-65°C to + 165°C
Power Dissipation (P_D)	1W
Lead Temperature (T_L) (Soldering, 10 seconds)	+260°C
ESD Tolerance (Note 2)	1500V min.
C_{ZAP}	100 pF
R_{ZAP}	1.5 k•

Note 1: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits are not intended; operation should be limited to those conditions specified under electrical characteristics.

Note 2: Value based on test complying with NSC SOP5-028 human body model ESD testing using the ETS-910 tester.

Note 3: Unless otherwise specified all voltages are referenced to ground.

5.2 Capacitance

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$ or $3.3V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{IN}	Input Pin Capacitance			8	10	pF
C_{ICLK}	Clock Input Capacitance			8	10	pF
C_{IO}	I/O Pin Capacitance	f = 1 MHz		10	12	pF
C_O	Output Pin Capacitance	f = 1 MHz		6	8	pF

5.3 Electrical Characteristics

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$ or $3.3V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
I_{CC}	V_{DD} Average Supply Current	$V_{DD} = 5V$, $V_{IL} = 0.5V$, $V_{IH} = 2.4V$, No Load			15	25	mA
		$V_{DD} = 3.3V$, $V_{IL} = 0.5V$, $V_{IH} = 2.4V$, No Load			8	15	mA
I_{CCSB}	V_{DD} Quiescent Supply Current in Low Power Mode (Note 1)	$V_{DD} = 5V$, $V_{IL} = 0.5V$, $V_{IH} = 2.4V$, No Load CLKIN=0			20		μA
		$V_{DD} = 3.3V$, $V_{IL} = 0.5V$, $V_{IH} = 2.4V$, No Load			10		μA
V_{IH}	Input High Voltage			2.0		V_{DD}	V
V_{IL}	Input Low Voltage			-0.5		0.8	V
BUS INTERFACE SIGNALS							
V_{OH}	Output High Voltage	$V_{DD} = 5V$ $I_{OH} = -15$ mA	$V_{DD} = 3.3V$ $I_{OH} = -7.5$ mA	2.4			V
V_{OL}	Output Low Voltage	$V_{DD} = 5V$ $I_{OL} = 24$ mA	$V_{DD} = 3.3V$ $I_{OL} = 12$ mA			0.4	V
I_{IL}	Input Load Current	$V_{IN} = V_{SS}$				-10	μA
		$V_{IN} = V_{DD}$				10	μA

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
I_{OZ}	Output TRI-STATE	$V_{IN} = V_{SS}$				-10	μA
	Leakage Current	$V_{IN} = V_{DD}$				10	μA
UART INTERFACE SIGNALS							
V_{OH}	Output High Voltage	$V_{DD} = 5V$ $I_{OH} = -6$ mA	$V_{DD} = 3.3V$ $I_{OH} = -3$ mA	2.4			V
V_{OL}	Output Low Voltage	$V_{DD} = 5V$ $I_{OL} = 12$ mA	$V_{DD} = 3.3V$ $I_{OL} = 6$ mA			0.4	V
I_{IL}	Input Load Current	$V_{IN} = V_{SS}$				-10	μA
		$V_{IN} = V_{DD}$				10	μA
INFRARED INTERFACE SIGNALS							
V_{OH}	Output High Voltage	$V_{DD} = 5V$ $I_{OH} = -6$ mA	$V_{DD} = 3.3V$ $I_{OH} = -3$ mA	2.4			V
V_{OL}	Output Low Voltage	$V_{DD} = 5V$ $I_{OL} = 12$ mA	$V_{DD} = 3.3V$ $I_{OL} = 6$ mA			0.4	V
I_{IL}	Input Load Current	$V_{IN} = V_{SS}$				-10	μA
		$V_{IN} = V_{DD}$				10	μA
MISCELLANEOUS SIGNALS							
V_{OL}	Output Low Voltage	$I_{OL} = 2$ mA				0.4	V
I_{ICLK}	CLK Input Load Current	$V_{IN} = V_{SS}$				-10	μA
		$V_{IN} = V_{DD}$				-10	μA

Note1: To achieve minimum power consumption it is recommended to do the following:
    1. Place the device in disable state by writing '00' to NOM and DEV_EN bits of the MCTL register.
    2. Keep all inputs stable high (2.7V for 3.3V and 4.4V for 5V supply) or stable low (0.3V for 3.3/5V supply).
    3. The clock-input pin, CLKIN, may remain active during disable state since it is blocked internally.

5.4 Switching Characteristics

All the timing specifications given in this section refer to 0.8V and 2.0V on all the signals as illustrated in Figure 5-1, unless specifically stated otherwise.

TL/C/11930-22

Figure 5-1. Testing Specification Standard

5.4.1 Timing Table

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$ or $3.3V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Min	Max	Unit
CLOCK TIMING				
t_{CH}	Clock High Pulse Width	8		ns
t_{CI}	Clock Low Pulse Width	8		ns
C_{FREQ}	Clock Frequency	48 - 100 ppm	48 + 100 ppm	MHz
CPU ACCESS TIMING				
t_{AR}	Address Valid to Read Active	15		ns
t_{AW}	Address Valid to Write Active	15		ns
t_{CSS}	$\overline{CS}$ Signal Setup	5		ns
t_{CSH}	$\overline{CS}$ Signal Hold	1		ns
t_{DH}	Data Hold	2		ns
t_{DS}	Data Setup	18		ns

48

Symbol	Parameter		Min	Max	Unit
t_{HZ}	Data Bus Floating From Read Inactive			25	ns
t_{RA}	Address Hold from Read Inactive		1		ns
t_{RRV}	Read Cycle Recovery		45		ns
t_{RD}	Read Strobe Width		60	1000	ns
t_{RDH}	Read Data Hold		10		ns
t_{RDV}	Data Valid From Read Active			55	ns
t_{WA}	Address Hold from Write Inactive		1		ns
t_{WRV}	Write Cycle Recovery		45		ns
t_{WR}	Write Strobe Width		60	1000	ns
t_{RI}	IRQn Reset Delay from Read Inactive			60	ns
t_{WI}	IRQn Reset Delay from Write Inactive			60	ns
RC	Read Cycle Time (RC > t_{AR} + t_{RD} + t_{RRV})		123		ns
WR	Write Cycle Time (WR > t_{AW} + t_{WR} + t_{WRV})		123		ns
DMA ACCESS TIMING					
t_{DSW}	Read or Write Signal Width		60	1000	ns
t_{DSQ}	DRQ Inactive from Read or Write Active			60	ns
t_{DKS}	DACK Signal Setup		15		ns
t_{DKH}	DACK Signal Hold		0		ns
t_{TCS}	TC Signal Setup		60		ns
t_{TCH}	TC Signal Hold from Read or Write Inactive		2		ns
INFRARED INTERFACE TIMING					
t_{CMW}	Modulation Signal Pulse Width in Sharp-IR and CEIR	Transmitter	t_{CWN} -25ns (Note 1)	t_{CWN}+25ns	
		Receiver	500		ns
t_{CMP}	Modulation Signal Period in Sharp-IR and CEIR	Transmitter	t_{CPN} -25 ns (Note 2)	t_{CPN} +25 ns	
		Receiver	t_{MMIN} (Note 3)	t_{MMAX}	
t_{BT}	Single Bit Time in UART and Sharp-IR	Transmitter	t_{BTN} - 25 ns (Note 4)	t_{BTN} + 25 ns	
		Receiver	t_{BTN} - 2%	t_{BTN} + 2%	
S_{DRT}	SIR Data Rate Tolerance. Percent of Nominal Data Rate.	Transmitter		+/- 0.87%	
		Receiver		+/- 2.0%	
t_{SJT}	SIR Leading Edge Jitter. Percent of Nominal Bit Duration.	Transmitter		+/- 2.5%	
		Receiver		+/- 6.0%	
t_{SPW}	SIR Pulse Width	Transmitter, Variable Width	(3/16) x t_{BTN} -15 ns (Note 4)	(3/16) x t_{BTN} +15 ns	
		Transmitter, Fixed Width	1.48	1.78	µs
		Receiver	1µs	(1/2) x t_{BTN}	
M_{DRT}	MIR Data Rate Tolerance. Percent of Nominal Data Rate.	Transmitter		+/- 0.1%	
		Receiver		+/- 0.15%	

www.national.com

Symbol	Parameter		Min	Max	Unit
t_{MJT}	MIR Leading Edge Jitter. Percent of Nominal Bit Duration.	Transmitter		+/- 2.9%	
		Receiver		+/- 6.0%	
t_{MPW}	MIR Pulse Width	Transmitter	t_{MWN} - 15ns (Note 5)	t_{MWN} + 15 ns	
		Receiver	60 ns	(1/2) x t_{BTN}	
F_{DRT}	FIR Data Rate Tolerance. Percent of Nominal Data Rate.	Transmitter		+/- 0.01%	
		Receiver		+/- 0.01%	
t_{FJT}	FIR Leading Edge Jitter. Percent of Nominal Chip Duration.	Transmitter		+/- 4.0%	
		Receiver		+/- 25.0%	
t_{FPW}	FIR Single Pulse Width (Note 6)	Transmitter	115	135	ns
		Receiver, Leading Edge Jitter = 0 ns	80	175	ns
		Receiver, Leading Edge Jitter = +/- 25 ns	90	150	ns
t_{DPW}	FIR Double Pulse Width (Note 6)	Transmitter	115	135	ns
		Receiver, Leading Edge Jitter = 0 ns	205	300	ns
		Receiver, Leading Edge Jitter = +/- 25 ns	215	310	ns
MISCELLANEOUS TIMING					
t_{WOD}	IRSL$_n$ Output Delay From Write Inactive			60	ns
t_{MRW}	Master Reset Pulse Width		1000		ns
t_{MRF}	Output Signals Floating From Reset Active			700	ns

Note 1: t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and CEIR modes. It is determined by the MCPW [2-0] and TXHSC bits in the IRTXMC and RCCFG registers.

Note 2: t_{CPN} is the nominal period of the modulation signal for Sharp-IR and CEIR modes. It is determined by the MCFR [4-0] and TXHSC bits in the IRTXMC and RCCFG registers.

Note 3: t_{MMIN} and t_{MMAX} define the time range within which the period of the incoming sub-carrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the content of register IRRXDC and the setting of bit RXHSC in the RCCFG register.

Note 4: t_{BTN} is the nominal bit time in UART, Sharp-IR, SIR, MIR and CEIR modes.

Note 5: t_{MWN} is the nominal pulse width for MIR mode. It is determined by the MPW [3-0] and MDRS bits in the MIR_PW and IRCR2 registers.

Note 6: The receiver pulse width requirements for various jitter values can be obtained by assuming a linear pulse-width/jitter relationship. For example, if the jitter is +/- 10 ns, the width of a single pulse must fall between 84 ns and 165 ns.
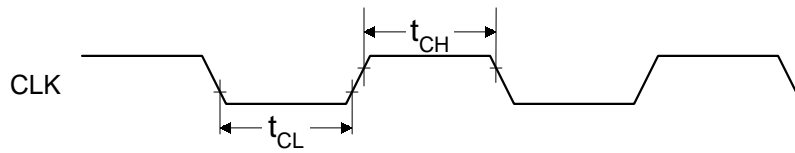
www.national.com

5.4.2 Timing Diagrams

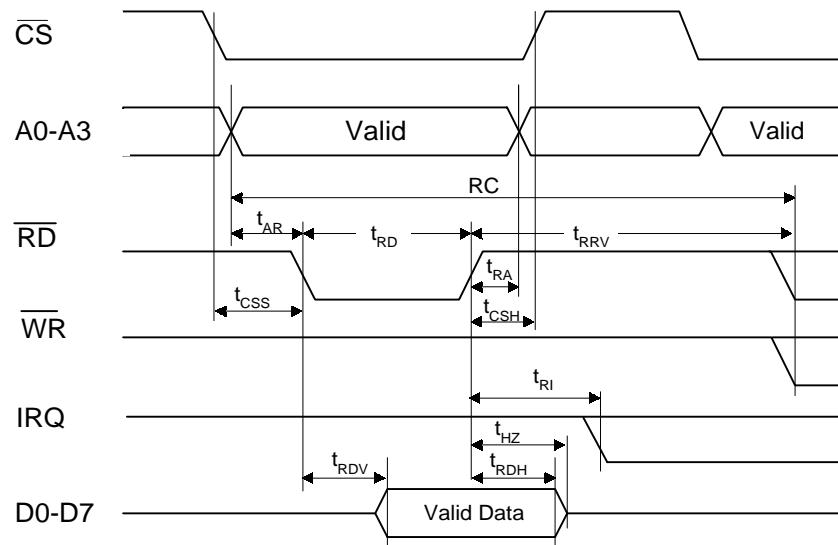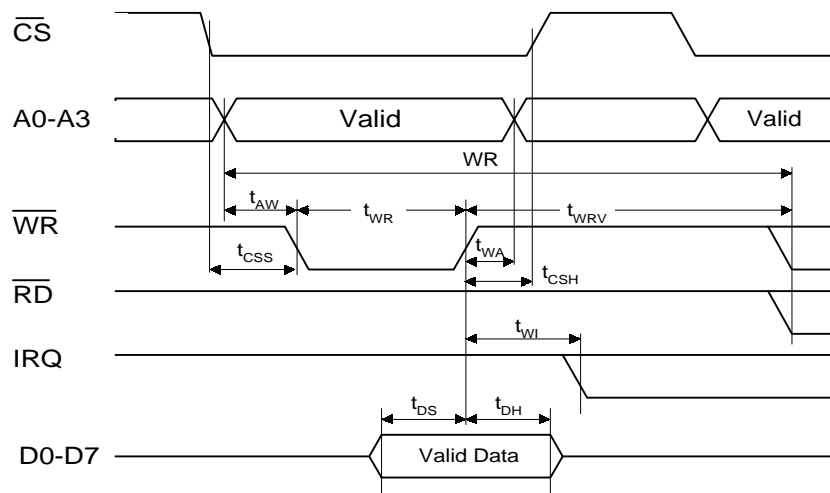**Figure 5-2. Clock Timing**

Figure 5-3. CPU Read Timing

Figure 5-4. CPU Write Timing
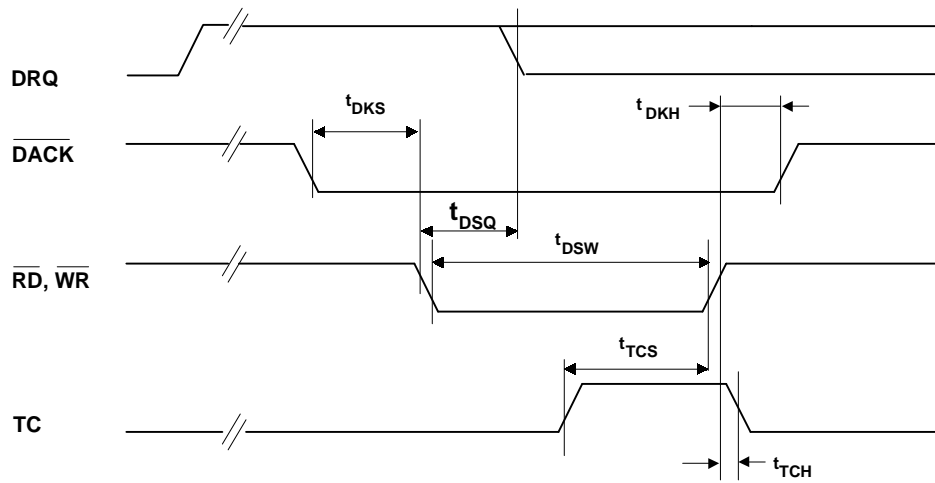
Figure 5-5. DMA Access Timing

UART

t_{BT}

Sharp-IR
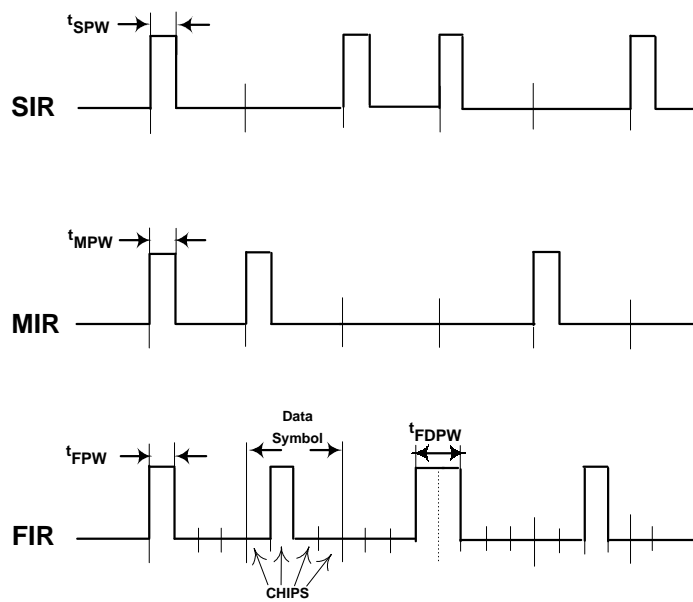**Consumer-IR**

t_{CMW} t_{CMP}
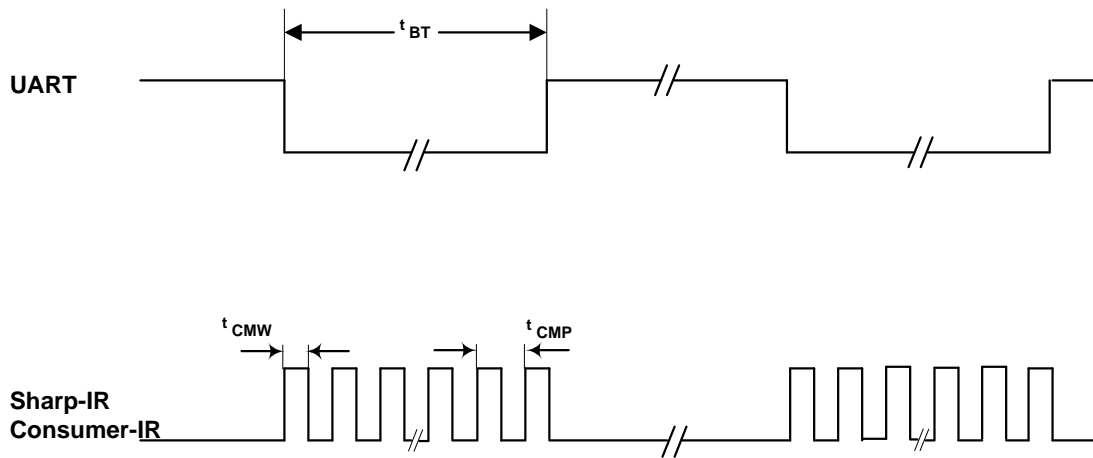
Figure 5-6. UART, Sharp-IR and CEIR Timing

SIR

t_{SPW}

MIR

t_{MPW}

FIR

t_{FPW} **Data Symbol** t_{FDPW}

CHIPS

Note: The signals shown here represent the infrared signals at the IRTX output. The infrared signals at the IRRXn inputs have opposite polarity.
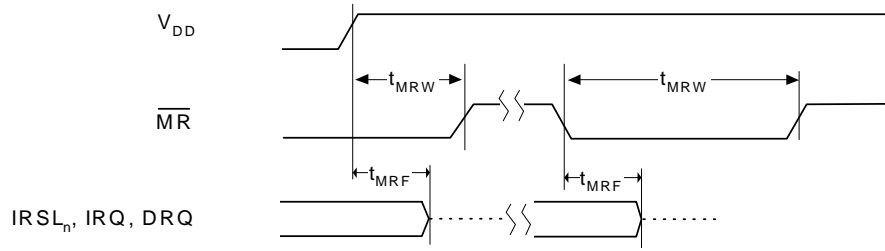
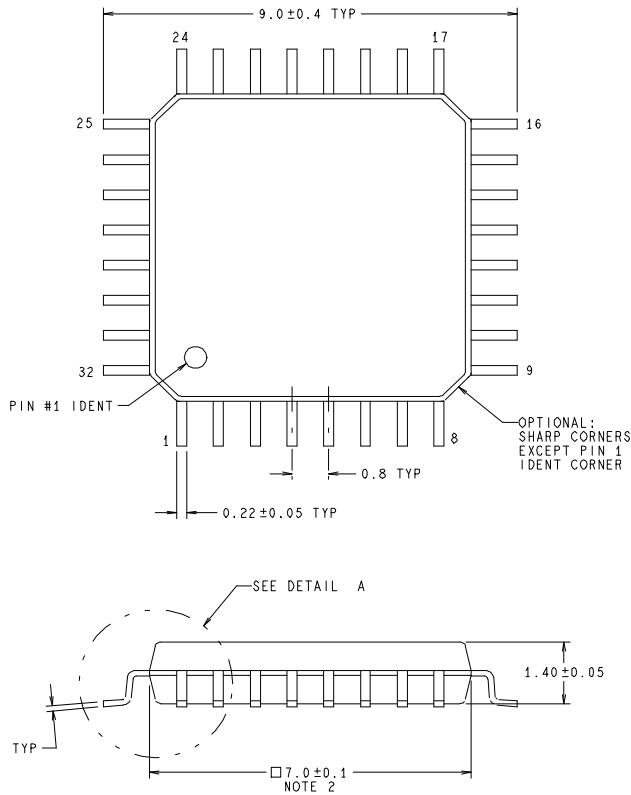**Figure 5-7. SIR, MIR and FIR Timing**

$\overline{WR}$

t_{WOD}
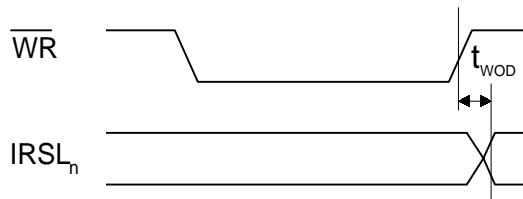
$IRSL_n$

Figure 5-8. IRSLn Write Timing

53   www.national.com

Figure 5-9. Reset Timing

www.national.com

6.0   Physical Dimensions inches(millimeters)

32-Pin Thin Quad Flat Pack

NOTES:UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   7.62 MICROMETERS MINIMUM SOLDER PLATING (85/15)
   THICKNESS ON ALLOY 42/COPPER.

2. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION.
   MAXIMUM ALLOWABLE MOLD PROTRUSION 0.15mm PER SIDE.

3. REFERENCE JEDEC REGISTRATION MO-136, VARIATION BC,
   DATED 4/93.
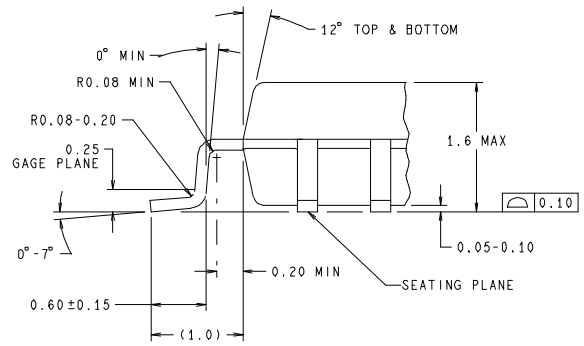
DIMENSIONS ARE IN MILLIMETERS

Figure 6-1. Thin Plastic Quad Flat Pack

Order Number PC87109VBE
NS Package Number VBE32A

PC87109VBE Advanced UART and Infrared Controller

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR COPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32

National Semiconductor Asia Pacific
Customer Response Group
Tel: 65-254-4466
Fax: 65-250-4466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179