60ns, Low Power, Single Supply, Ground-Sensing Comparator

FEATURES

- **Low Power: 450μA**
- **Fast: 60ns at 20mV Overdrive**
  85ns at 5mV Overdrive
- **Low Offset Voltage: 0.8mV**
- Operates Off Single 5V or Dual ±5V Supplies
- Input Common Mode Extends to Negative Supply
- No Minimum Input Slew Rate Requirement
- Complementary TTL Outputs
- Inputs Can Exceed Supplies without Phase Reversal
- Pin Compatible with LT1394, LT1016 and LT1116
- Output Latch Capability
- Available in 8-Lead MSOP and SO Packages

APPLICATIONS

- High Speed A/D Converters
- Zero-Crossing Detectors
- Current Sense for Switching Regulators
- Extended Range V/F Coverters
- Fast Pulse Height/Width Discriminators
- High Speed Triggers
- Line Receivers
- High Speed Sampling Circuits

DESCRIPTION

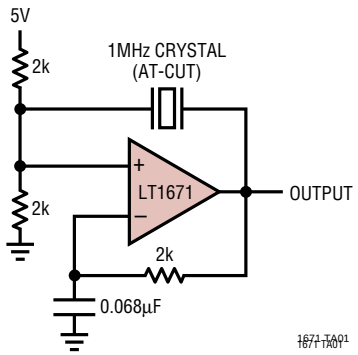
The LT®1671 is a low power 60ns comparator with complementary outputs and latch. The input common mode range extends from 1.5V below the positive supply down to the negative supply rail. Like the LT1394, LT1016 and LT1116, this comparator has complementary outputs designed to interface directly to TTL or CMOS logic. The LT1671 may operate from either a single 5V supply or dual ±5V supplies. Low offset voltage specifications and high gain allow the LT1671 to be used in precision applications.

The LT1671 is designed for improved speed and stability for a wide range of operating conditions. The output stage provides active drive in both directions for maximum speed into TTL, CMOS or passive loads with minimal cross-conduction current. Unlike other fast comparators, the LT1671 remains stable even for slow transitions through the active region, which eliminates the need to specify a minimum input slew rate.

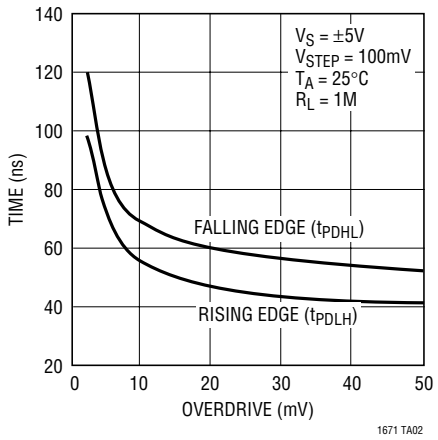
The LT1671 has an internal, TTL/CMOS compatible latch for retaining data at the outputs. The latch holds data as long as the LATCH pin is held high. Device parameters such as gain, offset and negative power supply current are not significantly affected by variations in negative supply voltage.

TYPICAL APPLICATION

1MHz Crystal Oscillator



Propagation Delay vs Overdrive

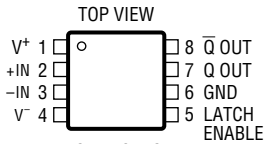


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12V
Positive Supply Voltage 7V
Negative Supply Voltage ..... –7V
Differential Input Voltage ..... ±12V
Input and Latch Current (Note 2) ..... ±10mA
Output Current (Continuous)(Note 2) ..... ±20mA

Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range (Note 3) ... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

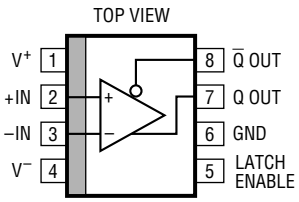
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LT1671CMS8
MS8 PART MARKING
LTCT



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1671CS8 LT1671IS8
S8 PART MARKING
1671 1671I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V^+ = 5V, V^- = –5V, $V_{OUT}(Q)$ = 1.4V, V_{LATCH} = V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$ (Note 4)			0.8	2.5	mV
			●			4.0	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		●		4		µV/°C
I_{OS}	Input Offset Current				10	100	nA
			●			150	nA
I_B	Input Bias Current	(Note 5)			120	280	nA
			●			350	nA
V_{CMR}	Input Voltage Range (Note 6)		●	–5		3.5	V
		Single 5V Supply	●	0		3.5	V
CMRR	Common Mode Rejection Ratio	$-5V \le V_{CM} \le 3.5V$, $T_A > 0°C$		55	100		dB
		$-5V \le V_{CM} \le 3.3V$, $T_A \le 0°C$		55			dB
		Single 5V Supply					
		$0V \le V_{CM} \le 3.5V$, $T_A > 0°C$		55	100		dB
		$0V \le V_{CM} \le 3.3V$, $T_A \le 0°C$		55			dB
PSRR	Power Supply Rejection Ratio	$4.6V \le V^+ \le 5.4V$	●	50	85		dB
		$-7V \le V^- \le -2V$	●	60	90		dB
A_V	Small Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		2500	5000		V/V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V^+ = 5V, V^- = –5V, $V_{OUT}(Q)$ = 1.4V, V_{LATCH} = V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	Output Voltage Swing High	$V^+ \geq 4.6V$, I_{OUT} = 400µA $V^+ \geq 4.6V$, I_{OUT} = 4mA	● ●	2.7 2.4	3.1 3.0		V V
V_{OL}	Output Voltage Swing Low	I_{OUT} = –400µA I_{OUT} = –4mA	●		0.3 0.4	0.5	V V
I^+	Positive Supply Current		 ●		450	800 1000	µA µA
I^-	Negative Supply Current		 ●		75	200 250	µA µA
V_{IH}	LATCH Pin High Input Voltage		●	2			V
V_{IL}	LATCH Pin Low Input Voltage		●			0.8	V
I_{IL}	LATCH Pin Current	V_{LATCH} = 0V	●	–1000	–250		nA
t_{PD1}	Propagation Delay	ΔV_{IN} = 100mV, V_{OD} = 20mV	 ●		60	80 110	ns ns
t_{PD2}	Propagation Delay (Note 7)	ΔV_{IN} = 100mV, V_{OD} = 5mV	 ●		85	100 130	ns ns
Δt_{PD}	Differential Propagation Delay (Note 7)	ΔV_{IN} = 100mV, V_{OD} = 5mV			15	30	ns
t_{LPD}	Latch Propagation Delay (Note 8)				60		ns
t_{SU}	Latch Setup Time (Note 8)				–15		ns
t_H	Latch Hold Time (Note 8)				35		ns
t_{PW}(D)	Minimum Disable Pulse Width				30		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This parameter is guaranteed to meet specified performance through design and characterization. It has not been tested.

Note 3: The LT1671CS8 and LT1671CMS8 are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. The LT1671IS8 is guaranteed to meet the extended temperature limits.

Note 4: Input offset voltage (V_{OS}) is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V.

Note 5: Input bias current (I_B) is defined as the average of the two input currents.

Note 6: Input voltage range is guaranteed in part by CMRR testing and in part by design and characterization.

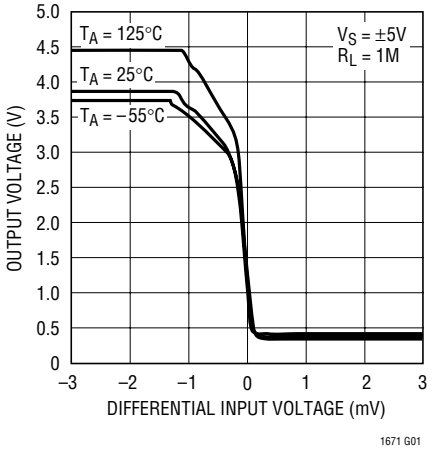
Note 7: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1671 is 100% tested with a 100mV step and 20mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} limits can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct. Propagation delay (t_{PD}) is measured with the overdrive added to the actual V_{OS}. Differential propagation delay is defined as:

$$\Delta t_{PD} = t_{PDLH} - t_{PDHL}$$

Note 8: Latch propagation delay (t_{LPD}) is the delay time for the output to respond when the LATCH pin is deasserted. Latch setup time (t_{SU}) is the interval in which the input signal must remain stable prior to asserting the latch signal. Latch hold time (t_H) is the interval after the latch is asserted in which the input signal must remain stable.

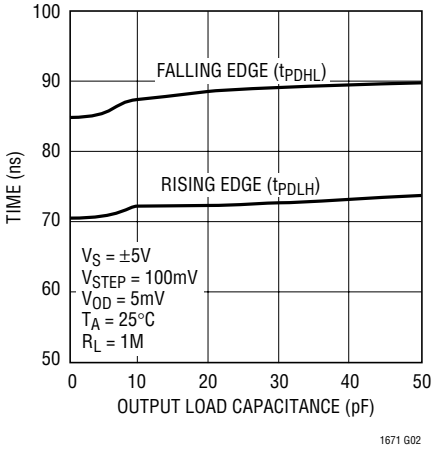
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Characteristics



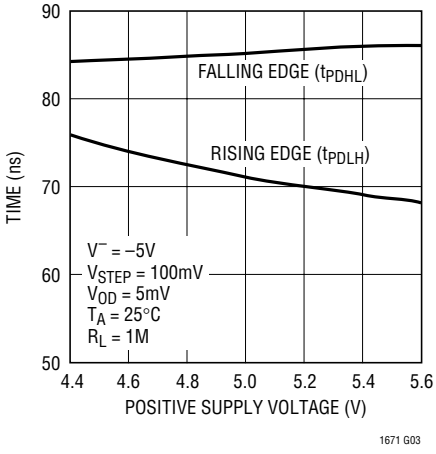
1671 G01

Propagation Delay vs Load Capacitance



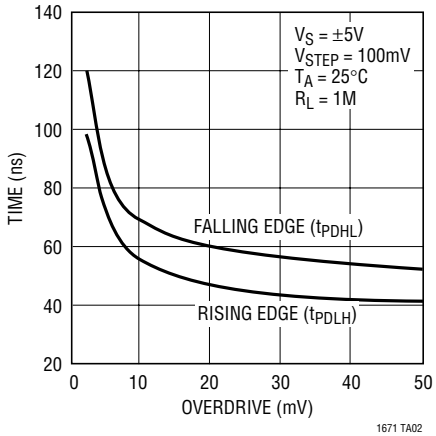
1671 G02

Propagation Delay vs Positive Supply Voltage



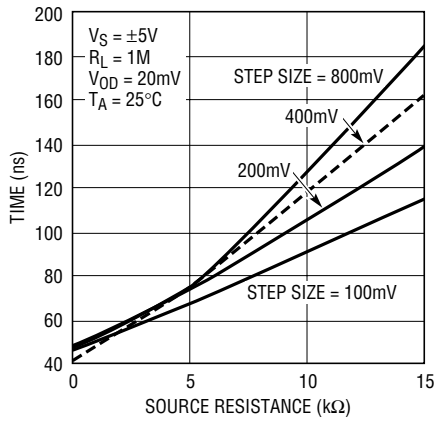
1671 G03

Propagation Delay vs Input Overdrive



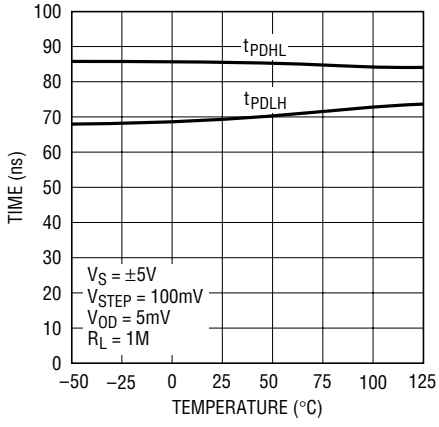
1671 TA02

Propagation Delay vs Source Resistance



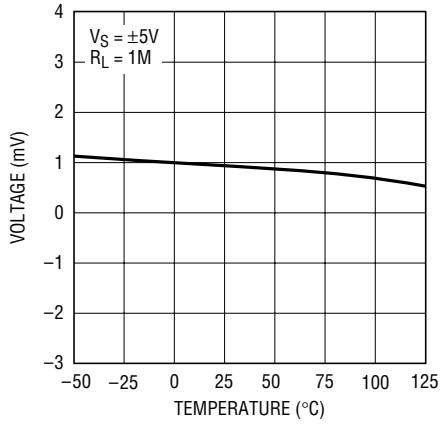
1671 G05

Propagation Delay vs Temperature



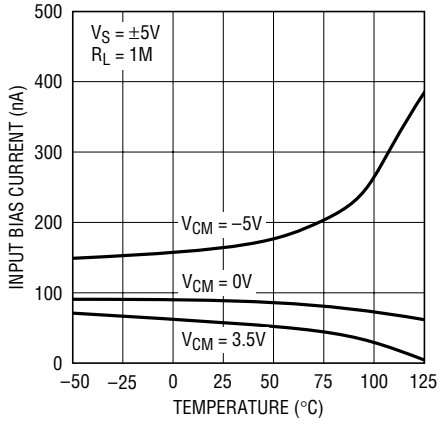
1671 G06

Input Offset Voltage vs Temperature



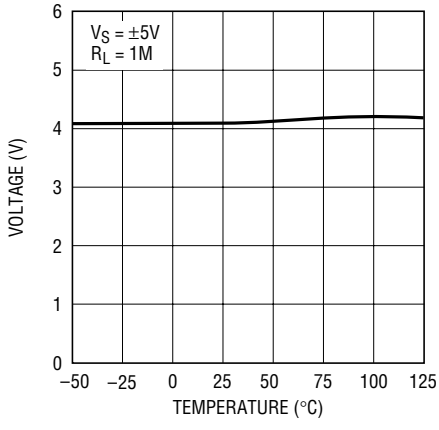
1671 G07

Input Bias Current vs Temperature



1671 G08

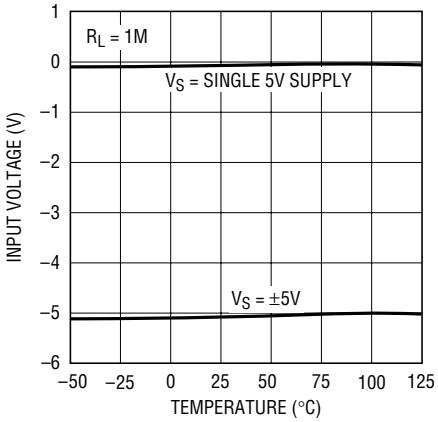
Positive Common Mode Limit vs Temperature



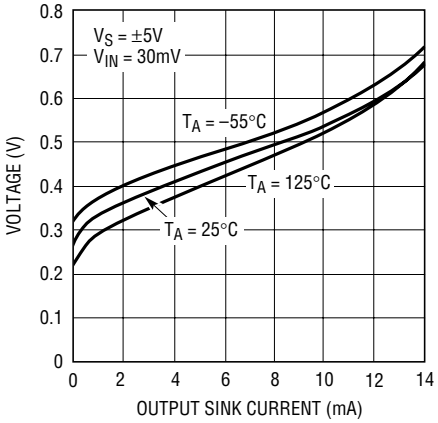
1671 G09

TYPICAL PERFORMANCE CHARACTERISTICS

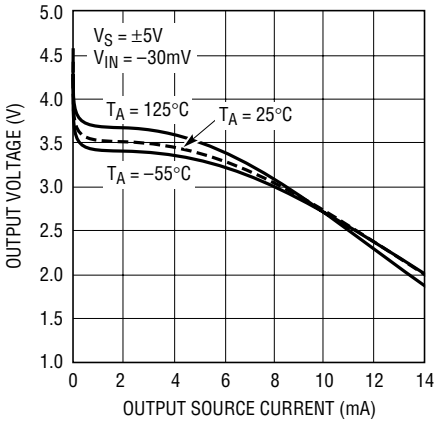
Negative Common Mode Limit vs Temperature



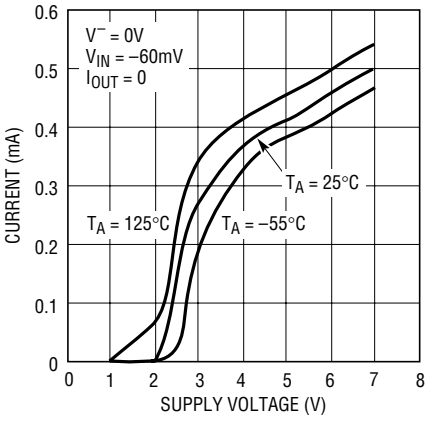
Output Low Voltage (V_{OL}) vs Output Sink Current



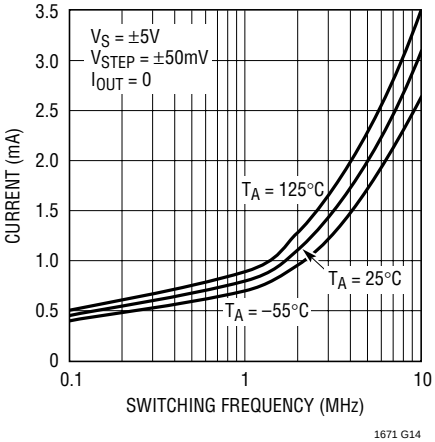
Output High Voltage (V_{OH}) vs Output Source Current



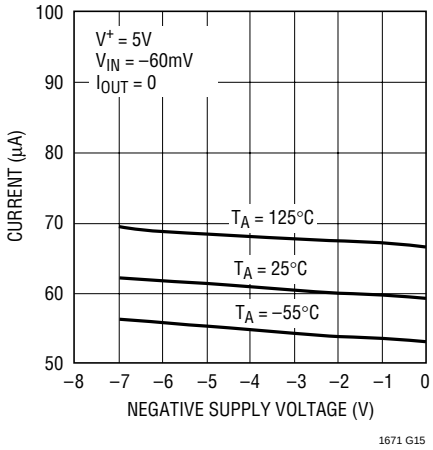
Positive Supply Current vs V^+ Supply Voltage



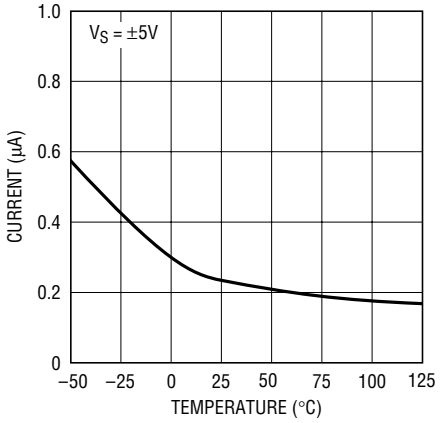
Positive Supply Current vs Switching Frequency



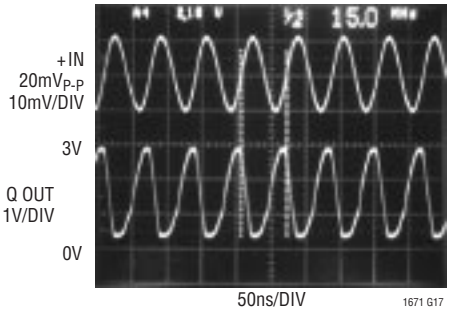
Negative Supply Current vs V^- Supply Voltage



Latch Pin Current vs Temperature

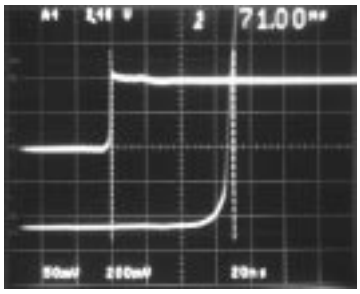


Response to 15MHz ±10mV Sine Wave

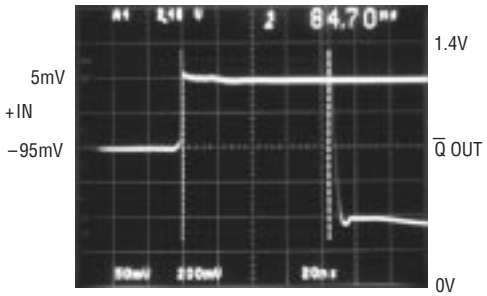


TYPICAL PERFORMANCE CHARACTERISTICS

t_{PD}^+ Response Time to 5mV Overdrive



t_{PD}^- Response Time to 5mV Overdrive



PIN FUNCTIONS

V^+ (Pin 1): Positive Supply Voltage. Normally 5V.

+IN (Pin 2): Noninverting Input.

–IN (Pin 3): Inverting Input.

V^- (Pin 4): Negative Supply Voltage. Normally either 0V or –5V.

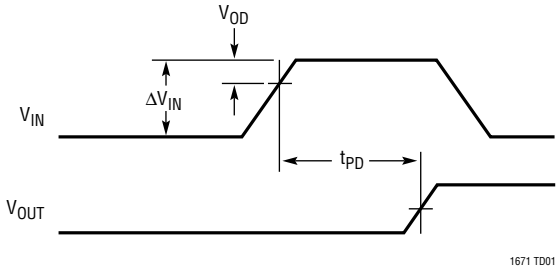
LATCH ENABLE (Pin 5): Latch Control Pin. When high, the outputs remain in a latched condition, independent of the current state of the inputs.

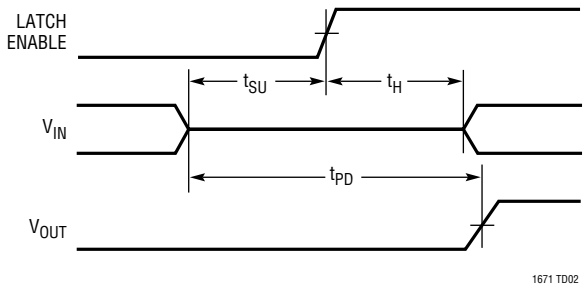
GND (Pin 6): Ground.

Q OUT (Pin 7): Noninverting Logic Output. This pin is high when +IN is above –IN and LATCH ENABLE is low.

$\overline{Q}$ OUT (Pin 8): Inverting Logic Output. This pin is low when +IN is above –IN and LATCH ENABLE is low.

TIMING DIAGRAMS





APPLICATIONS INFORMATION

Common Mode Considerations

The LT1671 is specified for a common mode range of –5V to 3.5V on a ±5V supply or a common mode range of 0V to 3.5V on a single 5V supply. A more general consideration is that the common mode range is 0V below the negative supply and 1.5V below the positive supply, independent of the actual supply voltage. The criterion for common mode limit is that the output still responds correctly to a small differential input signal.

When either input signal falls below the negative common mode limit, the internal PN diode formed with the substrate can turn on, resulting in significant current flow through the die. An external Schottky clamp diode between the input and the negative rail can speed up recovery from negative overdrive by preventing the substrate diode from turning on.

The zero crossing detector in Figure 1 demonstrates the use of a fast clamp diode. The zero crossing detector terminates the transmission line at its 50Ω characteristic impedance. Negative inputs should not fall below –2V to keep the signal current within the clamp diode's maximum forward rating. Positive inputs should not exceed the devices absolute maximum ratings nor the power rating on the terminating resistor.

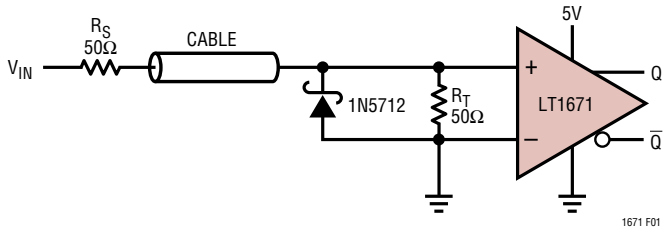


Figure 1. Fast Zero Crossing Detector

Either input may go above the positive common mode limit without damaging the comparator. The upper voltage limit is determined by an internal diode from each input to the positive supply. The input may go above the positive supply as long as it does not go far enough above it to conduct more than 10mA. Functionality will continue if the remaining input stays within the allowed common mode range. There will, however, be an increase in propagation delay as the input signal switches back into the common mode range.

Input Bias Current

Input bias current is measured with the output held at 1.4V. As with any PNP differential input stage, the LT1671 bias current flows out of the device. It will go to zero on an input which is high and double on an input which is low.

LATCH Pin Dynamics

The LATCH pin is intended to retain input data (output latched) when the LATCH pin goes high. The pin will float to a high state when disconnected, so a flow-through condition requires that the LATCH pin be grounded. The LATCH pin is designed to be driven with either a TTL or CMOS output. It has no built-in hysteresis.

To guarantee data retention, the input signal must remain valid at least 35ns after the latch goes high (hold time), and must be valid at least –15ns before the latch goes high (setup time). The negative setup time simply means that the data arriving 15ns after (rather than before) the latch signal is valid. When the latch signal goes low, new data will appear at the output in approximately 60ns (latch propagation delay).

Measuring Response Time

To properly measure the response of the LT1671 requires an input signal source with very fast rise times and exceptionally clean settling characteristics. The last requirement comes about because the standard comparator test calls for an input step size that is large compared to the overdrive amplitude. Typical test conditions are 100mV step size with 5mV overdrive. This requires an input signal that settles to within 1% (1mV) of final value in only a few nanoseconds with no ringing or settling tail. Ordinary high speed pulse generators are not capable of generating such a signal, and in any case, no ordinary oscilloscope is capable of displaying the waveform to check its fidelity. Some means must be used to inherently generate a fast, clean edge with known final value. The circuit shown in Figure 2 is the best electronic means of generating a fast, clean step to test comparators. It uses a very fast transistor in a common base configuration. The transistor is switched off with a fast edge from the generator and the collector voltage settles to exactly 0V in just a few nanoseconds. The most important feature of this

APPLICATIONS INFORMATION

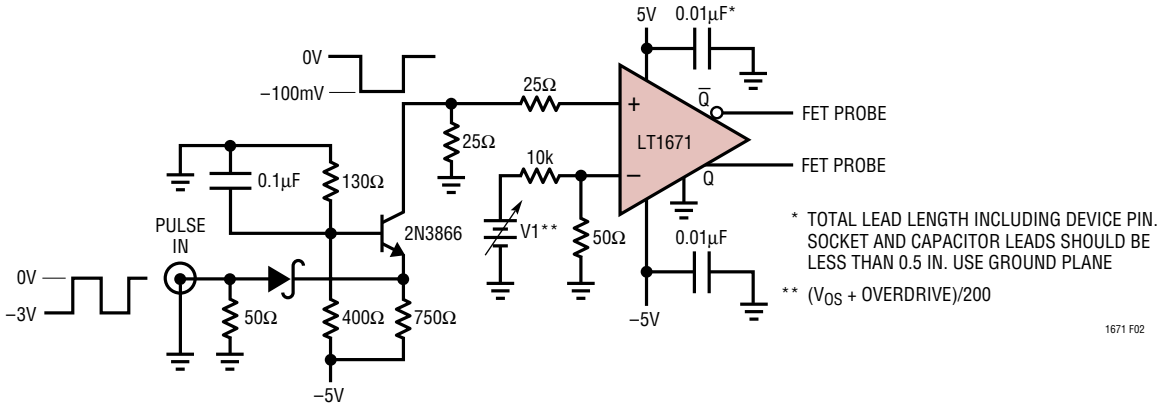


Figure 2. Response Time Test Circuit

circuit is the lack of feedthrough from the generator to the comparator input. This prevents overshoot on the comparator input, which would give a false fast reading on comparator response time.

To adjust the circuit for exactly 5mV overdrive, V1 is adjusted so that the LT1671 output under test settles to 1.4V (in the linear region). Then V1 is changed by –1V to set overdrive to 5mV.

High Speed Design Techniques

A substantial amount of design effort has made the LT1671 relatively easy to use. It is much less prone to oscillation than some slower comparators, even with slow input signals. However, as with any high speed comparator, there are a number of problems which may arise because of PC board layout and design. The most common problem involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move with changing internal current levels of the connected devices. This will almost always result in improper operation. In addition, adjacent devices connected through an unbypassed supply can interact with each other through the finite supply impedances. Bypass capacitors furnish a simple solution to this problem by providing a local reservoir of energy at the device, keeping supply impedances low.

Bypass capacitors should be as close as possible to the LT1671. A good high frequency capacitor such as a 0.1µF ceramic is recommended, in parallel with a larger capacitor such as a 4.7µF tantalum.

Poor trace routes and high source impedances are also common sources of problems. Be sure to keep trace lengths as short as possible, and avoid running any output trace adjacent to an input trace to prevent unnecessary coupling. If output traces are longer than a few inches, be sure to terminate them with a resistor to eliminate any reflections that may occur. Resistor values are typically 250Ω to 400Ω. Also, be sure to keep source impedances as low as possible, preferably 1kΩ or less.

About Level Shifts

The LT1671's logic output will interface with many circuits directly. Many applications, however, require some form of level shifting of the output swing. With LT1671-based circuits this is not trivial because it is desirable to maintain very low delay in the level shifting stage. When designing level shifters, keep in mind that the TTL output of the LT1671 is a sink-source pair (Figure 3) with good ability to drive capacitance (such as feedforward capacitors). Figure 4 shows a noninverting voltage gain stage with a 15V output. When the LT1671 switches, the base-emitter voltages at the 2N2369 reverse, causing it to switch very quickly. The 2N3866 emitter-follower gives a low impedance output and the Schottky diode aids current sink capability.

APPLICATIONS INFORMATION

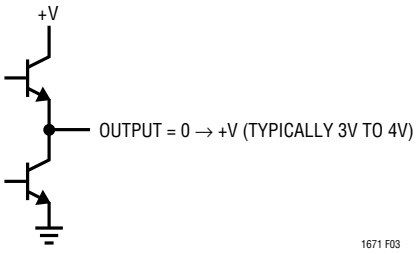


Figure 3. Simplified LT1671 Output Stage

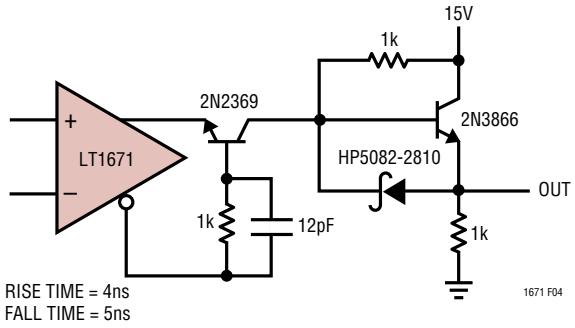


Figure 4. Level Shift Has Noninverting Voltage Gain

Figure 5 is a very versatile stage. It features a bipolar swing that is set by the output transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the LT1671 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1671's output transition, but Q2's switching is clean with 3ns delay on the rise and fall of the pulse. Figure 6 is similar to Figure 4 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET that switches 1A at 15V. Most of the 7ns to 9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high f_T. To get the kind of results shown, switching times in the nanosecond range and an f_T approaching 1GHz are required.

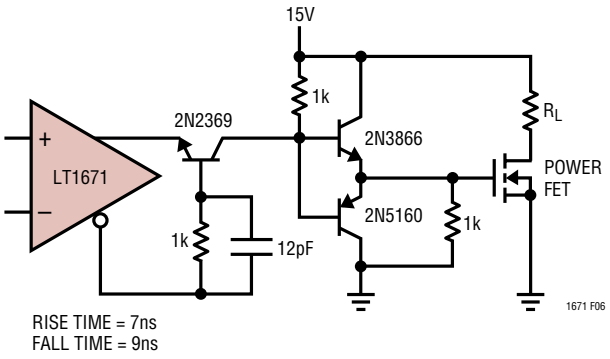


Figure 6. Noninverting Voltage Gain Level Shift

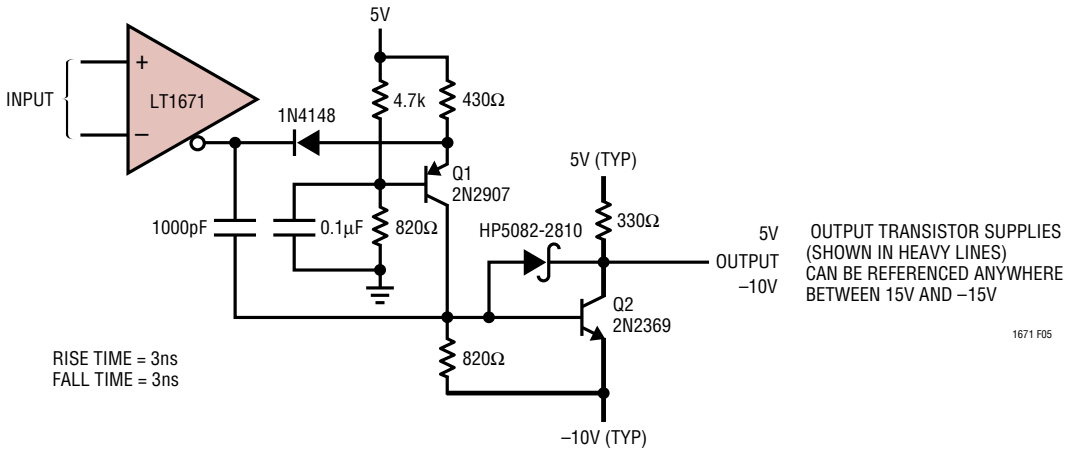


Figure 5. Level Shift with Inverting Voltage Gain—Bipolar Swing

APPLICATIONS INFORMATION

Crystal Oscillators

Figure 7 shows a crystal oscillator circuit. In the circuit, the resistors at the LT1671's positive input set a DC bias point. The 2k-0.068µF path sets up phase shifted feedback and the circuit looks like a wideband unity-gain follower at DC. The crystal's path provides resonant positive feedback and stable oscillation occurs.

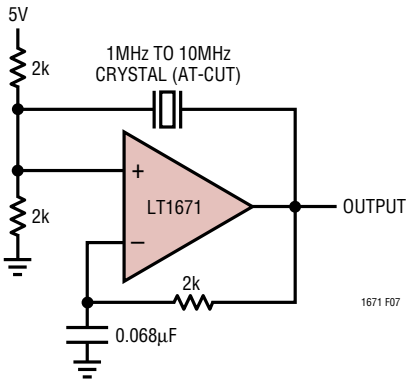


Figure 7. 1MHz to 10MHz Crystal Oscillator

Switchable Output Crystal Oscillator

Figure 8 permits crystals to be electronically switched by logic commands. This circuit is similar to the previous examples, except that oscillation is only possible when one of the logic inputs is biased high.

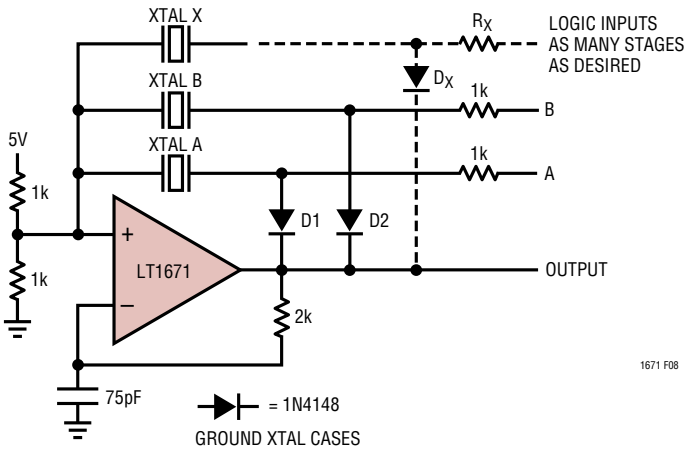
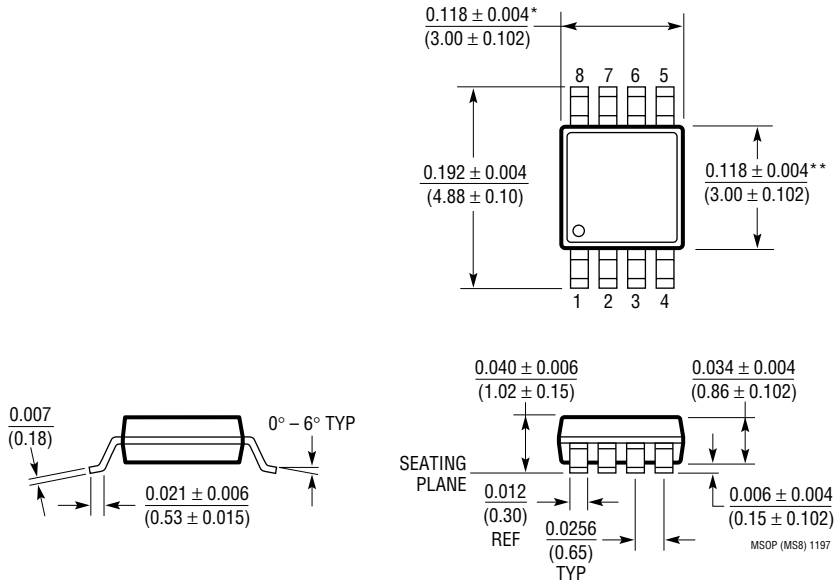


Figure 8. Switchable Output Crystal Oscillator. Biasing A or B High Places Associated Crystal in Feedback Path. Additional Crystal Branches Are Permissible

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

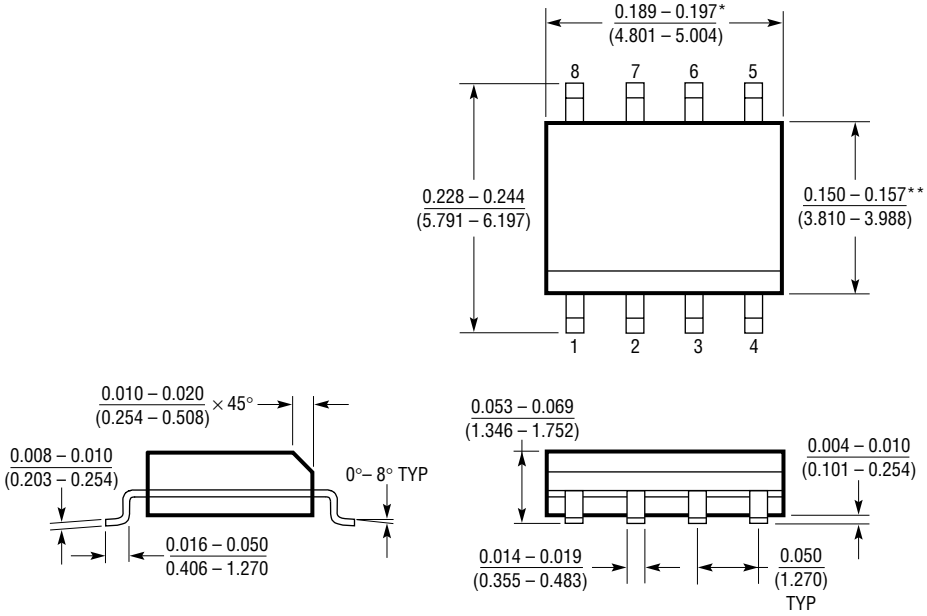
MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

4MHz Adaptive Trigger Circuit

Line and fiber-optic receivers often require an adaptive trigger to compensate for variations in signal amplitude and DC offsets. The circuit in Figure 9 triggers on 2mV to 175mV signal from 100Hz to 4MHz while operating from a single 5V rail. A1, operating at a gain of 15, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of the midpoint of A1's output signal appears at the junction of the 500pF capacitor and the 3MΩ units. This point always sits midway between the signal's excursions, regardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1671's positive input. The LT1671's negative input is biased directly from A1's output. The LT1671's output, the circuit's output, is unaffected by >85:1 signal amplitude variations. Bandwidth limiting in A1 does not affect triggering because the adaptive trigger threshold varies ratiometrically to maintain circuit output.

Figure 10 shows operating waveforms at 4MHz. Trace A's input produces Trace B's amplified output at A1. The comparator's output is Trace C.

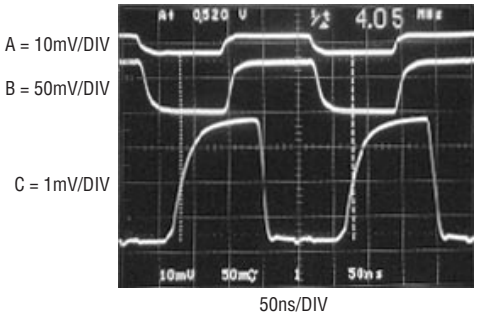


Figure 10. Adaptive Trigger Responding to a 4MHz, 5mV Input. Input Amplitude Variations from 2mV to 175mV Are Accommodated

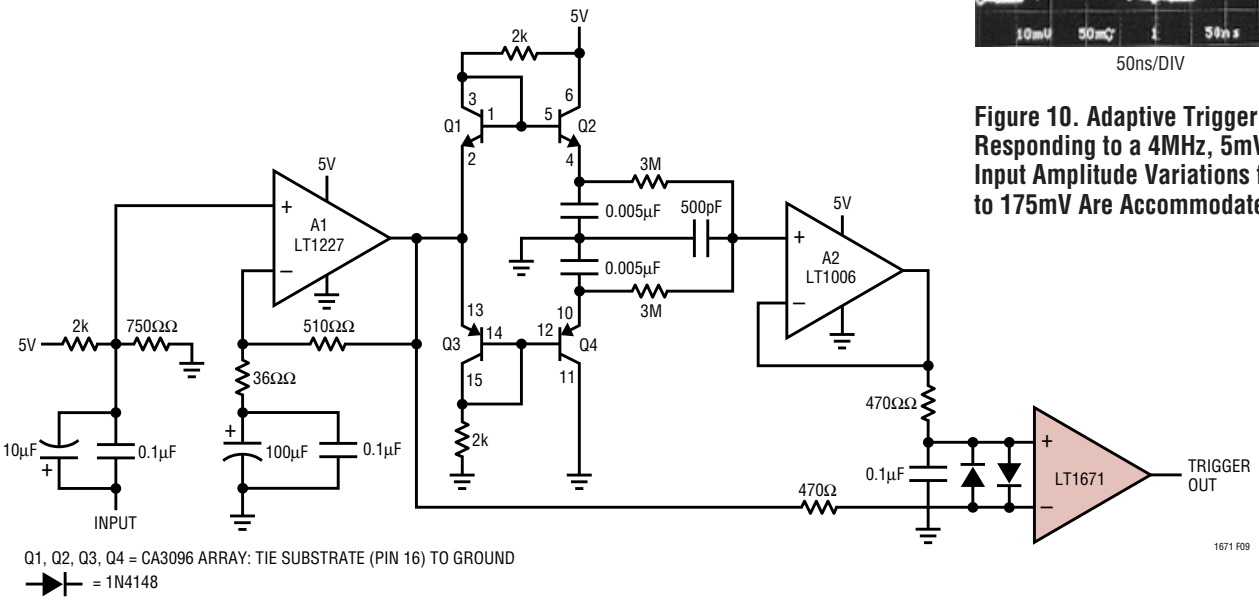


Figure 9. 4MHz Single Supply Adaptive Trigger. Output Comparator's Threshold Varies Ratiometrically with Input Amplitude, Maintaining Data Integrity over >85:1 Input Amplitude Range

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1016	UltraFast™ Precision Comparator	Industry Standard 10ns Comparator
LT1116	12ns Single Supply Ground-Sensing Comparator	Single Supply Version of LT1016
LT1394	UltraFast Single Supply Comparator	7ns, 6mA Single Supply Comparator
LT1720	UltraFast Dual Single Supply Comparator	Dual 4.5ns, 4mA Single Supply Comparator

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