



TDA7429

DIGITALLY CONTROLLED AUDIO PROCESSOR WITH SURROUND SOUND MATRIX

1 FEATURES

- 3 STEREO INPUTS
- INPUT ATTENUATION CONTROL IN 0.5dB STEP
- TREBLE MIDDLE AND BASS CONTROL
- THREE SURROUND MODES ARE AVAILABLE
 - MUSIC: 4 SELECTABLE RESPONSES
 - MOVIE AND SIMULATED: 256 SELECTABLE RESPONSES
- FOUR SPEAKERS ATTENUATORS:
 - 4 INDEPENDENT SPEAKERS CONTROL IN 1dB STEPS FOR BALANCE FACILITY
 - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS

2 DESCRIPTION

The TDA7429 is volume tone (bass middle and treble) balance (Left/Right) processors for quality audio applications in TV and Hi-Fi systems.

Figure 1. Package



Table 1. Order Codes

Part Number	Package
TDA7429S	SDIP42
TDA7429T	TQFP44
TDA7429T13TR	Tape & Reel

It reproduces surround sound by using programmable phase shifters and a signal matrix. Control of all the functions is accomplished by serial bus. The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

Figure 2. Pin Connection (TQFP44)

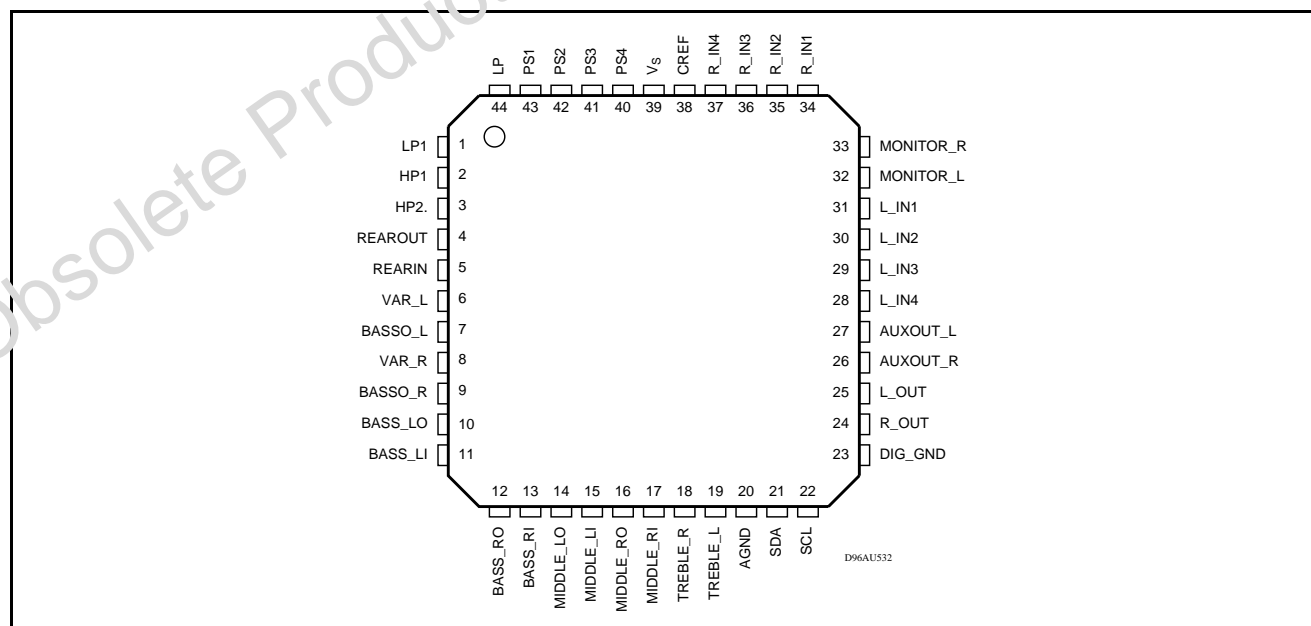


Figure 3. PIN CONNECTION (SDIP42)

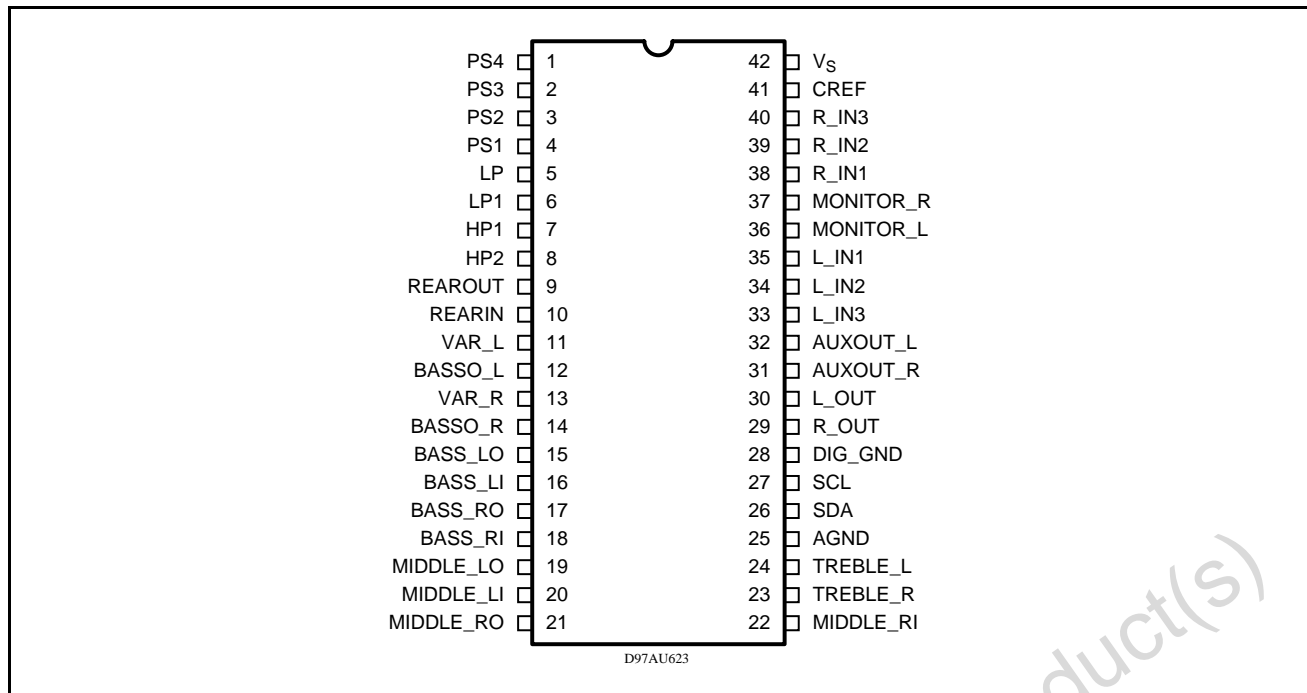


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _S	Operating Supply Voltage	11	V
T _{amb}	Operating Ambient Temperature	0 to 70	°C
T _{stg}	Storage Temperature Range	-55 to 150	°C

Table 3. Quick Reference Data

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _S	Supply Voltage	7	9	10.2	V
V _{CL}	Max Input Signal Handling	2			V _{RMS}
THD	Total Harmonic Distortion V = 0.1V _{rms} f = 1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio V _{out} = 1V _{rms} (mode = OFF)		106		dB
S _C	Channel Separation f = 1KHz		90		dB
	Treble Control (2dB step)	-14		14	dB
	Middle Control (2dB step)	-14		14	dB
	Bass Control (2dB step)	-14		14	dB
	Balance Control 1dB step (LCH, RCH)	-79		0	dB
	Mute Attenuation		100		dB

Table 4. Thermal Data

Symbol	Parameter	Value	Unit
R _{th j-pin}	Thermal Resistance Junction-pins	85	°C/W

Figure 4. TEST CIRCUIT (TDA7429S)

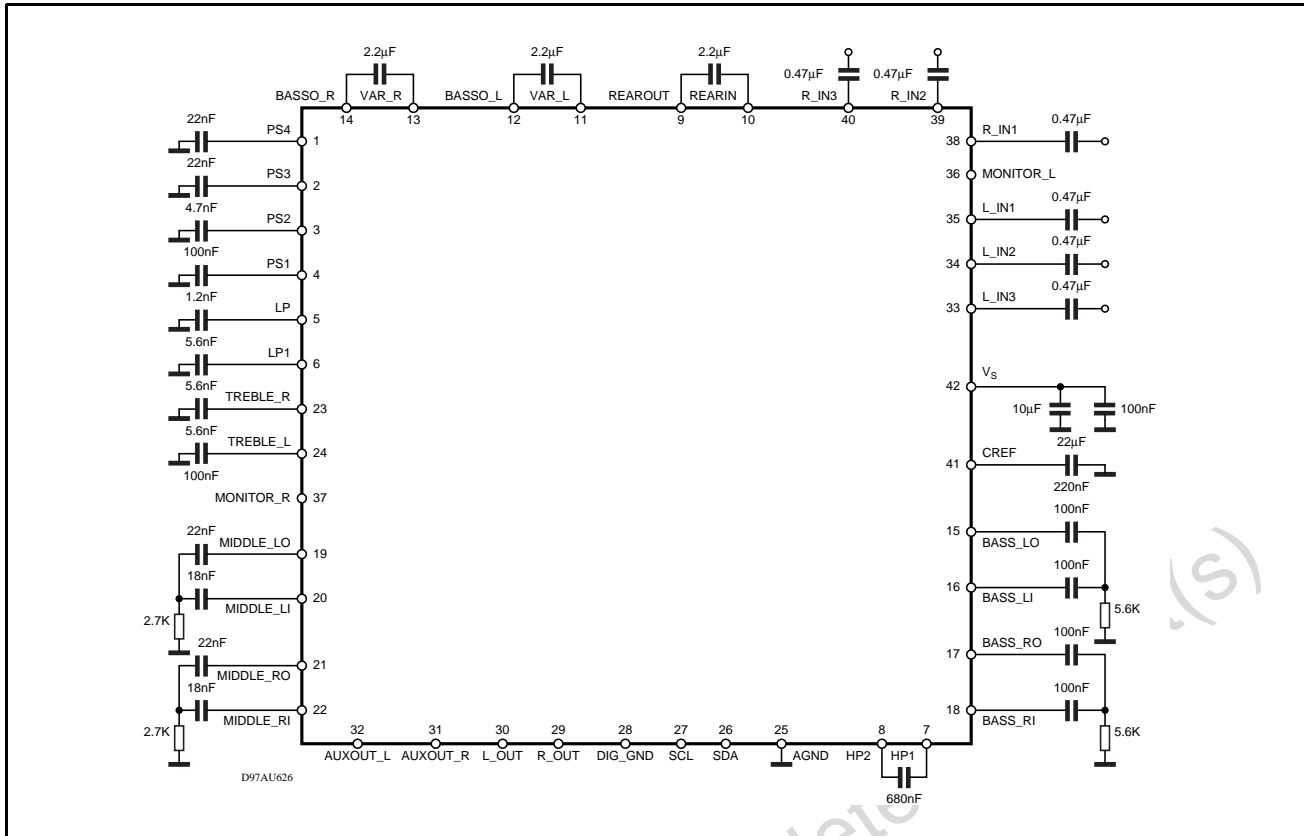


Figure 5. TEST CIRCUIT (TDA7429T)

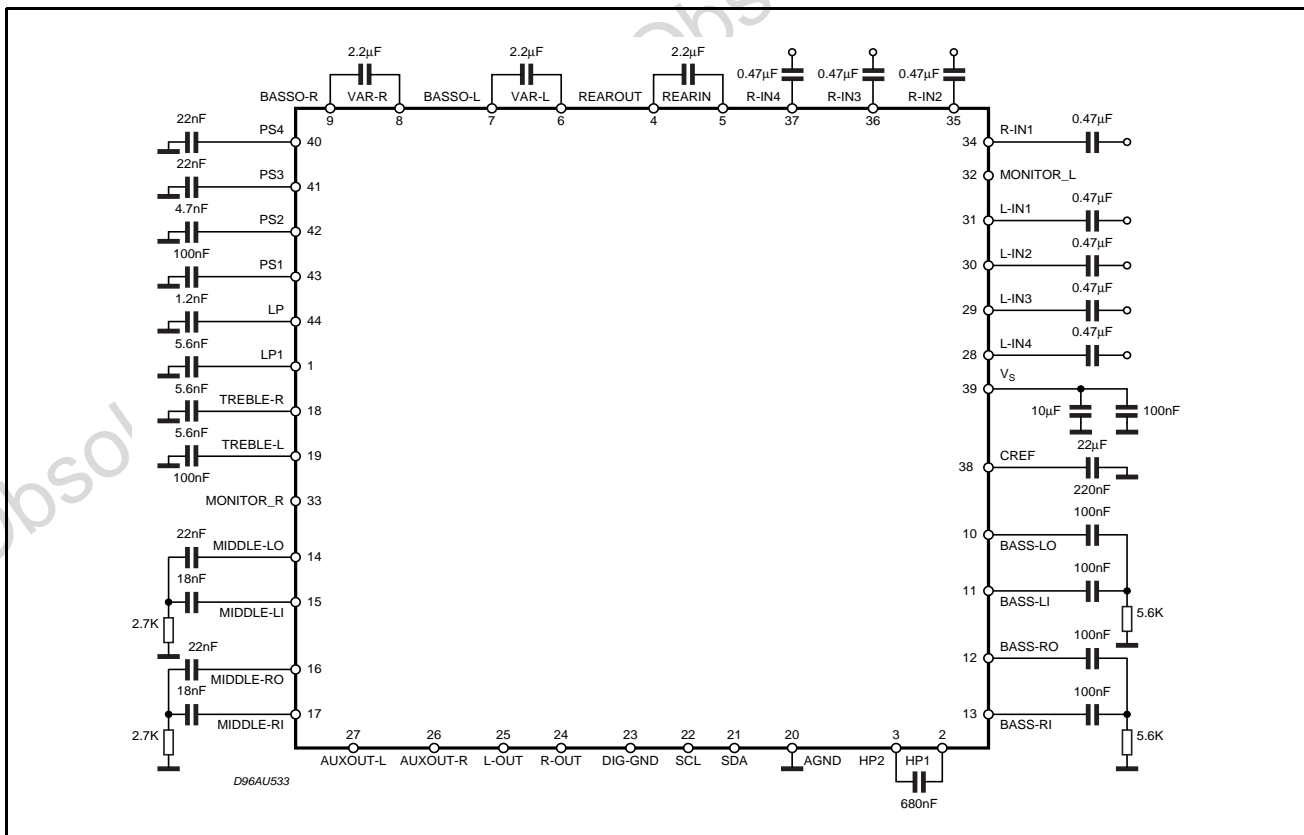


Figure 6. Block Diagram (TDA7429T)

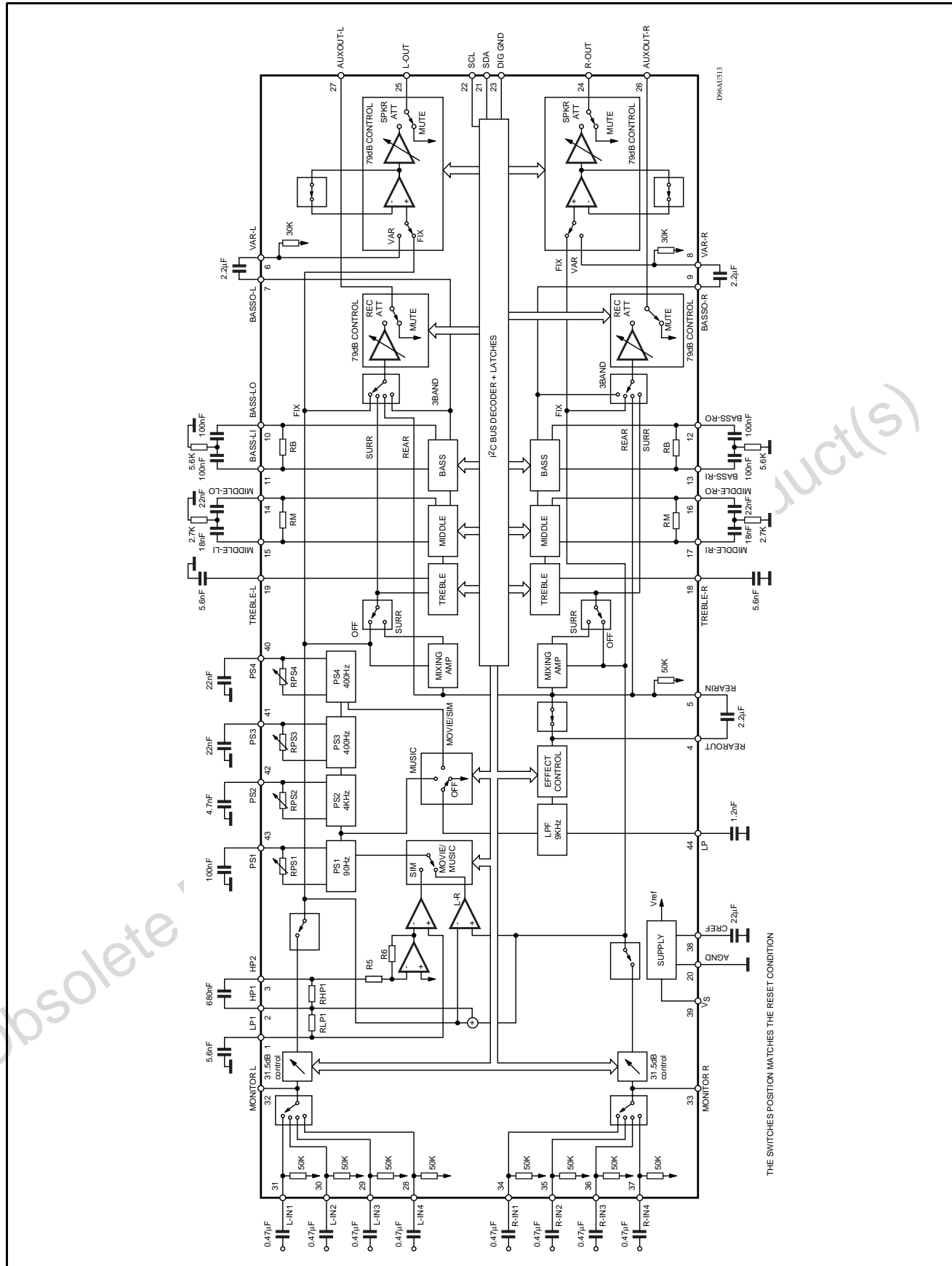


Figure 7. Block Diagram (TDA7429S)

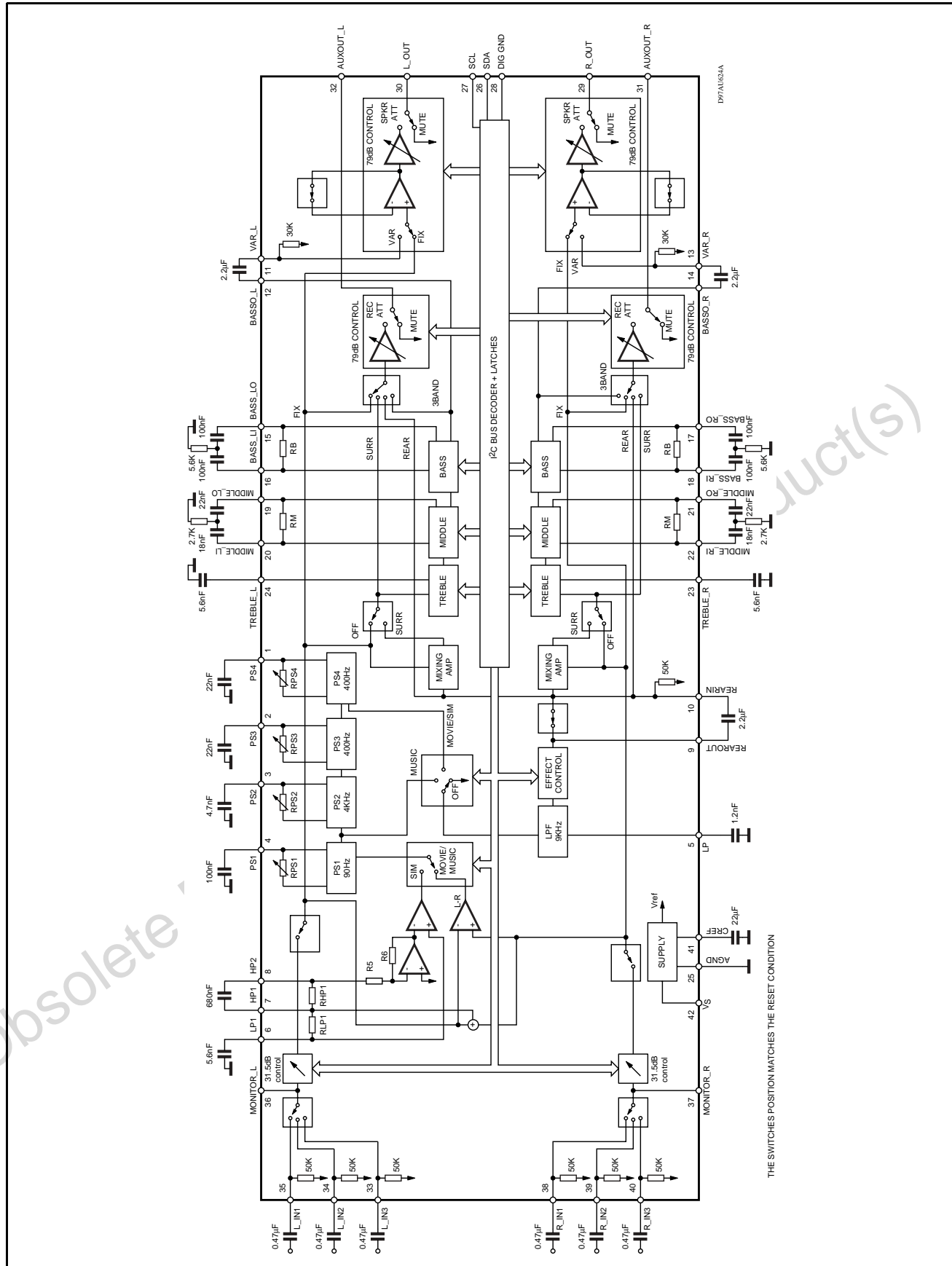


Table 5. Electrical Characteristics (refer to the test circuit $T_{amb} = 25^{\circ}\text{C}$, $V_S = 9\text{V}$, $R_L = 10\text{K}\Omega$, $V_{in} = 1\text{V}_{rms}$; $R_G = 600\Omega$, all controls flat ($G = 0\text{dB}$), $L+R \text{ CTRL} = +4\text{dB}$, $\text{MODE} = \text{OFF}$; $f = 1\text{KHz}$ unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		7	9	10.2	V
I_S	Supply Current		10	18	26	mA
SVR	Ripple Rejection	$L_{CH} / R_{CH \text{ out}}$, Mode = OFF	60	80		dB
INPUT STAGE						
R_{IN}	Input Resistance		35	50	65	$\text{K}\Omega$
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		V_{rms}
C_{RANGE}	Control Range			31.5		dB
$A_{V_{MIN}}$	Min. Attenuation		-1	0	1	dB
$A_{V_{MAX}}$	Max. Attenuation		31	31.5	32	dB
A_{STEP}	Step Resolution			0.5	1	dB
BASS CONTROL						
G_b	Control Range	Max. Boost/cut	± 11.5	± 14.0	± 16.0	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		32	44	56	$\text{K}\Omega$
MIDDLE CONTROL						
G_m	Control Range	Max. Boost/cut	± 11.5	± 14.0	± 16.0	dB
M_{STEP}	Step Resolution		1	2	3	dB
R_M	Internal Feedback Resistance		17.5	25	32.5	$\text{K}\Omega$
TREBLE CONTROL						
G_t	Control Range	Max. Boost/cut	± 13.0	± 14.0	± 15.0	dB
T_{STEP}	Step Resolution		1	2	3	dB
EFFECT CONTROL						
C_{RANGE}	Control Range		-21		-6	dB
S_{STEP}	Step Resolution		0.5	1	1.5	dB
SURROUBND SOUBND MATRIX PHASE						
R_{PS10}	Phase Shifter 1: $D1 = 0, D0 = 0$		8.3	11.8	15.2	$\text{K}\Omega$
R_{PS11}	Phase Shifter 1: $D1 = 0, D0 = 1$		10	14.1	18.3	$\text{K}\Omega$
R_{PS12}	Phase Shifter 1: $D1 = 1, D0 = 0$		12.6	17.9	23.3	$\text{K}\Omega$
R_{PS13}	Phase Shifter 1: $D1 = 1, D0 = 1$		26.4	37.3	48.85	$\text{K}\Omega$
R_{PS20}	Phase Shifter 2: $D3 = 0, D2 = 0$		4	5.6	7.2	$\text{K}\Omega$

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SURROUND SOUND MATRIX						
TEST CONDITION (Phase Resistor Selection D0=0, D1=1, D2=0, D3=1, D4=0, D5=1, D6=0, D7=1)						
RPS21	Phase Shifter 2: D3 = 0, D2 = 1		4.8	6.8	8.7	K Ω
RPS22	Phase Shifter 2: D3 = 1, D2 = 0		6	8.4	10.9	K Ω
RPS23	Phase Shifter 2: D3 = 1, D2 = 1		12.9	18.3	23.7	K Ω
RPS30	Phase Shifter 3: D5 = 0, D4 = 0		8.5	12.1	15.6	K Ω
RPS31	Phase Shifter 3: D5 = 0, D4 = 1		10.2	14.5	18.7	K Ω
RPS32	Phase Shifter 3: D5 = 1, D4 = 0		12.7	18.1	23.3	K Ω
RPS33	Phase Shifter 3: D5 = 1, D4 = 1		27.4	39.1	50.75	K Ω
RPS40	Phase Shifter 4: D7 = 0, D6 = 0		8.5	12.1	15.6	K Ω
RPS41	Phase Shifter 4: D7 = 0, D6 = 1		10.2	14.5	18.7	K Ω
RPS42	Phase Shifter 4: D7 = 1, D6 = 0		12.7	18.1	23.3	K Ω
RPS43	Phase Shifter 4: D7 = 1, D6 = 1		27.4	39.1	50.75	K Ω
G _{OFF}	In-phase Gain (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V _{p-p} , R _{in} → R _{out} , L _{in} → L _{out}	-1	0	1	dB
DG _{OFF}	LR In-phase Gain Difference (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V _{p-p} , R _{in} → R _{out} , L _{in} → L _{out}	-1	0	1	dB
G _{MOV}	In-phase Gain (Movie)	Movie mode, Effect Ctrl = -6dB 1kHz, 1.4 V _{p-p} , R _{in} → R _{out} , L _{in} → L _{out}		8		dB
DG _{MOV}	LR In-phase Gain Difference (Movie)	Movie mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} (R _{in} → R _{out}) - (L _{in} → L _{out})		0		dB
G _{MUS}	In-phase Gain (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} (R _{in} → R _{out}), (L _{in} → L _{out})		7		dB
DG _{MUS}	LR In-phase Gain Difference (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} (R _{in} → R _{out}), (L _{in} → L _{out})		0		dB
L _{MON1}	Simulated L Output 1	Simulated Mode, Effect Ctrl = -6dB Input signal of 250Hz, 1.4 V _{p-p} , R _{in} and L _{in} → L _{out}		4.5		dB
L _{MON2}	Simulated L Output 2	Simulated Mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} , R _{in} and L _{in} → L _{out}		-4.0		dB
L _{MON3}	Simulated L Output 3	Simulated Mode, Effect Ctrl = -6dB Input signal of 3.6kHz, 1.4 V _{p-p} , R _{in} and L _{in} → L _{out}		7.0		dB
R _{MON1}	Simulated R Output 1	Simulated Mode, Effect Ctrl = -6dB Input signal of 250Hz, 1.4 V _{p-p} , R _{in} and L _{in} → R _{out}		-4.5		dB

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R _{MON2}	Simulated R Output 2	Simulated Mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} , R _{in} and L _{in} → R _{out}		3.8		dB
R _{MON3}	Simulated R Output 3	Simulated Mode, Effect Ctrl = -6dB Input signal of 3.6kHz, 1.4 V _{p-p} , R _{in} and L _{in} → R _{out}		- 20		dB
R _{LP1}	Low Pass Filter Resistance		7	10	13	KΩ
R _{HPI}	High Pass Filter Resistance		42	60	78	KΩ
R _{LPF}	LP Pin Impedance		7	10	13	KΩ
SPEAKER & AUX ATTENUATORS						
C _{RANGE}	Control Range			79		dB
S _{STEP}	Step Resolution		-0.5	1	1.5	dB
E _A	Attenuation set error	A _v = 0 to -20dB	-1.5	0	1.5	dB
		A _v = -20 to -79dB	-3	0	2	dB
V _{DC}	DC Steps	adjacent att. steps	-3	0	3	mV
A _{MUTE}	Output Mute Condition		+70	100		dB
R _{VEA}	Input Impedance		21	30	39	KΩ
AUDIO OUTPUTS						
N _{O(OFF)}	Output Noise (OFF)	Output Mute, Flat BW = 20Hz to 20KHz		4 5		μV _{rms} μV _{rms}
N _{O(MOV)}	Output Noise (Movie)	Mode = Movie BW = 20Hz to 20KHz		30		μV _{rms}
N _{O(MUS)}	Output Noise (Music)	Mode = Music BW = 20Hz to 20KHz		30		μV _{rms}
N _{O(MON)}	Output Noise (Simulated)	Mode Simulated BW = 20Hz to 20KHz		30		μV _{rms}
d	Distorsion	A _v = 0 ; V _{in} = 1V _{rms}		0.01	0.1	%
S _C	Channel Separation		70	90		dB
V _{OCL}	Clipping Level	d = 0.3%	2	2.5		V _{rms}
R _{OUT}	Output Resistance		25	50	85	Ω
V _{OUT}	DC Voltage Level			3.8		V
MONITOR OUTPUTS						
d	Distorsion	A _v = 0 ; V _{in} = 1V _{rms}		0.01	0.1	%
S _C	Channel Separation		70	90		dB
V _{OCL}	Clipping Level	d = 0.3%	2	2.5		V _{rms}
R _{OUT}	Output Resistance		20	50	85	Ω
V _{OUT}	DC Voltage Level			4.5		V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BUS INPUTS						
V _{IL}	Input Low Voltage				1	V
V _{IH}	Input High Voltage		3			V
I _{IN}	Input Current		-5		+5	mA
V _O	Output Voltage SDA Acknowledge	I _O = 1.6mA			0.4	V

3 I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7429 and viceversa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

3.1 Data Validity

As shown in fig. 8, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

3.2 Start and Stop Conditions

As shown in fig.9 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

3.3 Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

3.4 Acknowledge

The master (mP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 10). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

3.5 Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the μ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

Figure 8. Data validity on the I²C bus

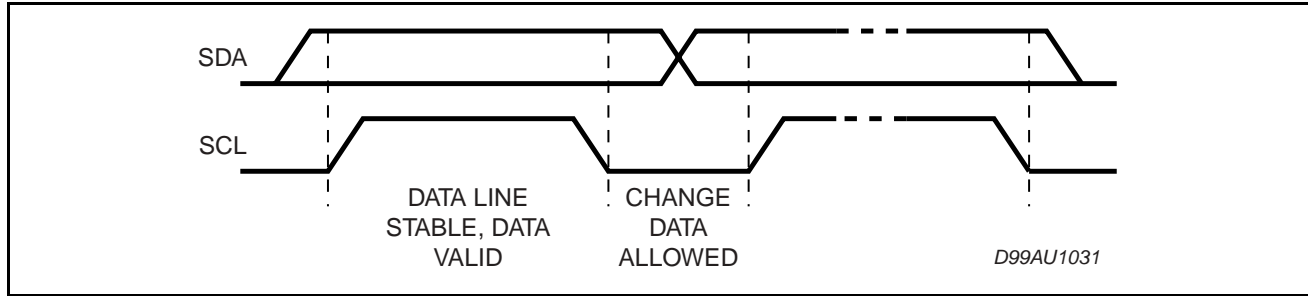


Figure 9. Timing Diagram of I²C bus

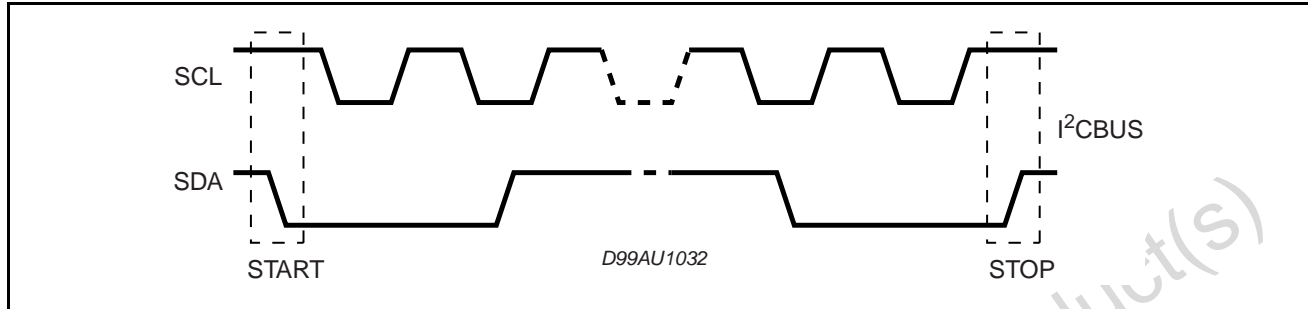
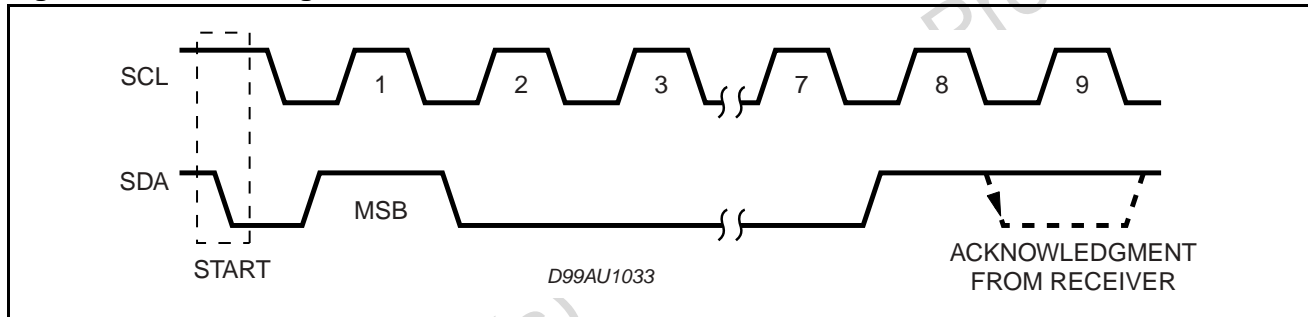


Figure 10. Acknowledge on the I²C bus



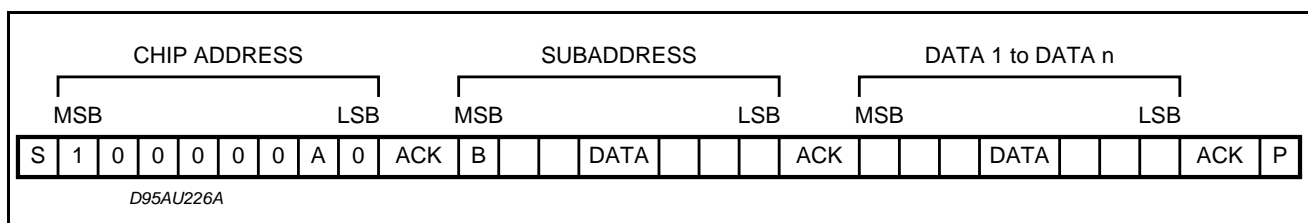
4 SOFTWARE SPECIFICATION

4.1 Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7429 address
- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)

Figure 11.

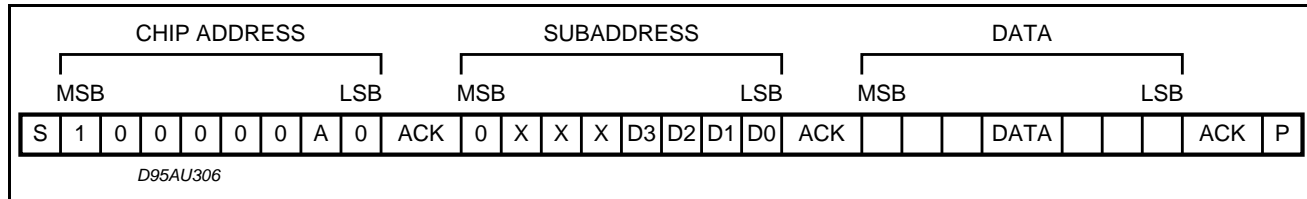


5 EXAMPLES

5.1 No Incremental Bus

The TDA7429 receives a start condition, the correct chip address, a subaddress with the MSB = 0 (no incremental bus), N-datas (all these datas concern the subaddress selected), a stop condition.

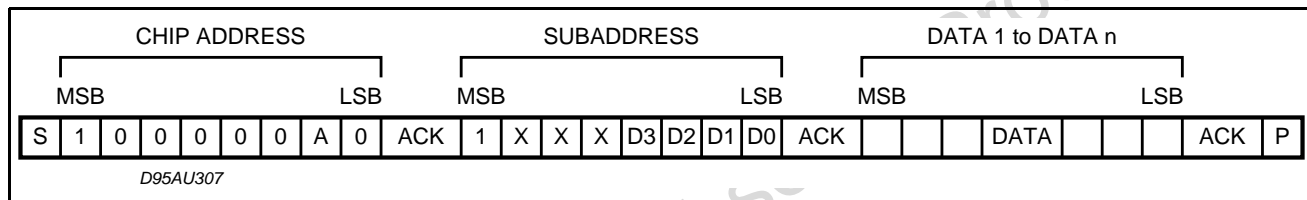
Figure 12.



5.2 Incremental Bus

The TDA7429 receives a start condition, the correct chip address, a subaddress with the MSB = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "1XXX1010" to "1XXX1111" of DATA are ignored. The DATA 1 concern the subaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receives the stop condition.

Figure 13.



6 DATA BYTES

Address = 80(HEX)

6.1 Function Selection

Table 6. The first byte (Subaddress)

MSB			LSB					SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
B	X	X	X	0	0	0	0	INPUT ATTENUATION
B	X	X	X	0	0	0	1	SURROUND & OUT & EFFECT CONTROL
B	X	X	X	0	0	1	0	PHASE RESISTOR
B	X	X	X	0	0	1	1	BASS & NATURAL BASE
B	X	X	X	0	1	0	0	MIDDLE & TREBLE
B	X	X	X	0	1	0	1	SPEAKER ATTENUATION "L"
B	X	X	X	0	1	1	0	SPEAKER ATTENUATION "R"
B	X	X	X	0	1	1	1	AUX ATTENUATION "L"
B	X	X	X	1	0	0	0	AUX ATTENUATION "R"
B	X	X	X	1	0	0	1	INPUT MULTIPLEXER, & AUX OUT

B = 1 incremental bus; active

B = 0 no incremental bus;

X = indifferent 0,1

Table 7. INPUT ATTENUATION SELECTION

MSB							LSB	INPUT ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	0.5 dB STEPS
X					0	0	0	0
X					0	0	1	-0.5
X					0	1	0	-1
X					0	1	1	-1.5
X					1	0	0	-2
X					1	0	1	-2.5
X					1	1	0	-3
X					1	1	1	-3.5
								4 dB STEPS
X		0	0	0				0
X		0	0	1				-4
X		0	1	0				-8
X		0	1	1				-12
X		1	0	0				-16
X		1	0	1				-20
X		1	1	0				-24
X		1	1	1				-28

INPUT ATTENUATION = 0 ~ -31.5dB

Table 8.

D7	D6	D5	D4	D3	D2	D1	D0	REAR SWITCH
X	0							REARIN, REAROUT PIN
								ACTIVE
X	1							NO REARIN, REAROUT PIN

Table 9. SURROUND SELECTION

MSB							LSB		SURROUND MODE
D7	D6	D5	D4	D3	D2	D1	D0		
X						0	0	SIMULATED	
X						0	1	MUSIC	
X						1	0	OFF	
X						1	1	MOVIE	
								OUT	
X					0			VAR	
X					1			FIX	
EFFECT CONTROL									
X	0	0	0	0				-6	
X	0	0	0	1				-7	
X	0	0	1	0				-8	
X	0	0	1	1				-9	
X	0	1	0	0				-10	
X	0	1	0	1				-11	
X	0	1	1	0				-12	
X	0	1	1	1				-13	
X	1	0	0	0				-14	
X	1	0	0	1				-15	
X	1	0	1	0				-16	
X	1	0	1	1				-17	
X	1	1	0	0				-18	
X	1	1	0	1				-19	
X	1	1	1	0				-20	
X	1	1	1	1				-21	

Table 10. PHASE RESISTOR SELECTION

MSB							LSB		SURROUND PHASE RESISTOR
D7	D6	D5	D4	D3	D2	D1	D0	PHASE SHIFT 1 (K Ω)	
						0	0	12	
						0	1	14	
						1	0	18	
						1	1	37	
PHASE SHIFT 2 (KΩ)									
				0	0			6	
				0	1			7	
				1	0			8	
				1	1			18	
PHASE SHIFT 3 (KΩ)									
		0	0					12	
		0	1					14	
		1	0					18	
		1	1					39	
PHASE SHIFT 4 (KΩ)									
0	0							12	
0	1							14	
1	0							18	
1	1							39	

Table 13. MIDDLE & TREBLE SELECTION

MSB				LSB				MIDDLE
D7	D6	D5	D4	D3	D2	D1	D0	2 dB STEPS
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14
								TREBLE
								2 dB STEPS
0	0	0	0					-14
0	0	0	1					-12
0	0	1	0					-10
0	0	1	1					-8
0	1	0	0					-6
0	1	0	1					-4
0	1	1	0					-2
0	1	1	1					0
1	1	1	1					0
1	1	1	0					2
1	1	0	1					4
1	1	0	0					6
1	0	1	1					8
1	0	1	0					10
1	0	0	1					12
1	0	0	0					14

Table 14. INPUT/RECOUT L & R SELECTION

MSB							LSB	INPUT MULTIPLEXER
D7	D6	D5	D4	D3	D2	D1	D0	
X					0	0	0	IN2
X					0	1	0	IN3
X					1	0	0	IN4
X					1	1	0	IN1
								AUX OUT "L"
X			0	0			0	VER 1 (3BAND)
X			0	1			0	VER 2 (SURR)
X			1	0			0	VER 3 (REAR)
X			1	1			0	FIX
								AUX OUT "R"
X	0	0					0	VER 1 (3BAND)
X	0	1					0	VER 2 (SURR)
X	1	0					0	VER 3 (REAR)
X	1	1					0	FIX

Table 15.

POWER ON RESET	
BASS & MIDDLE	2dB
TREBLE	0dB
SURROUND & OUT CONTROL+ EFFECT CONTROL	OFF + FIX + MAX ATTENUATION
SPEAKER/AUX ATTENUATION L & R	MUTE
INPUT ATTENUATION + REAR SWITCH	MAX ATTENUATION + ON
NATURAL BASE	OFF
INPUT	IN1

Figure 14. PIN: VOUT REF

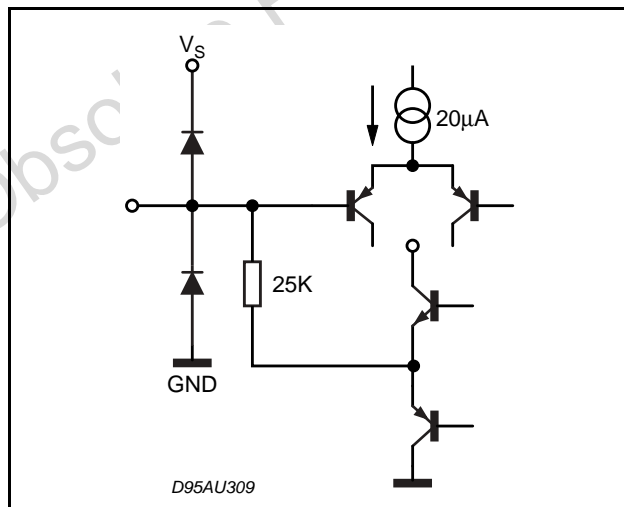


Figure 15. PIN: TREBLE-L, TREBLE-R

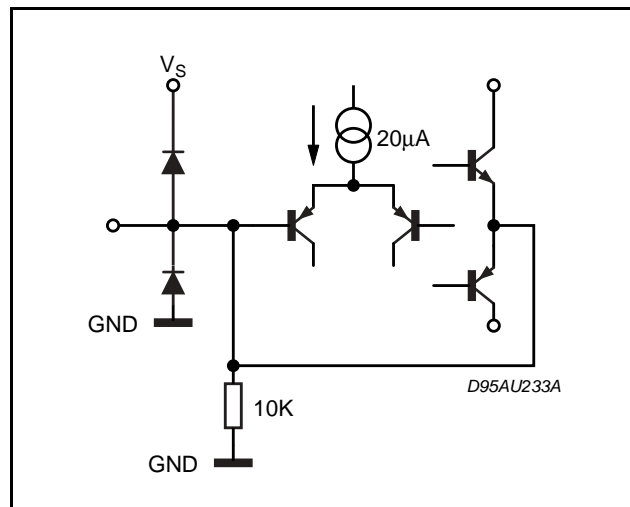


Figure 16. PIN: HP1

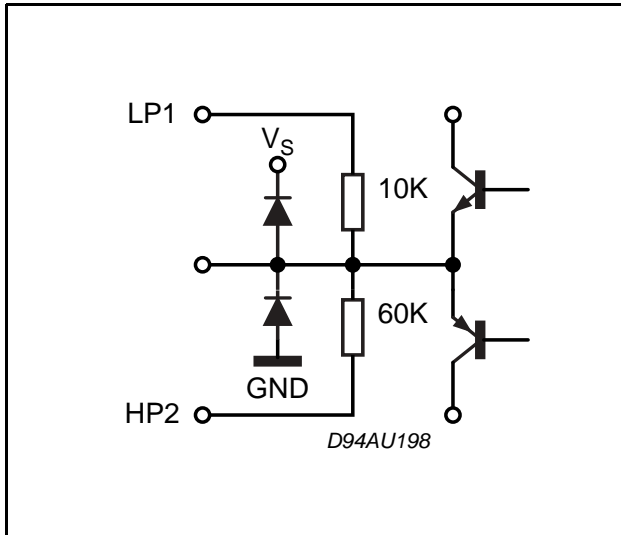


Figure 19. PIN: L-IN, R-IN, L-IN2, R-IN2, L-IN3, R-IN3, L-IN4, R-IN4,

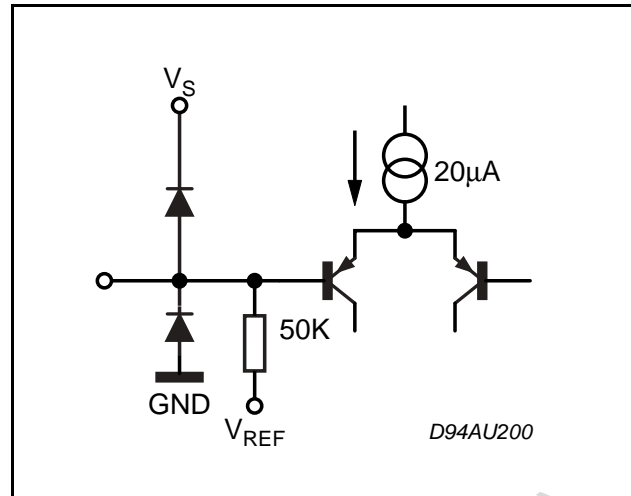


Figure 17. PIN: HP2

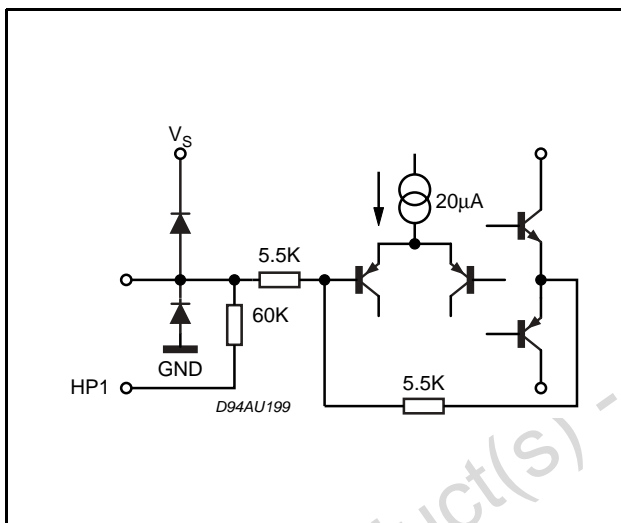


Figure 20. PIN: LP1

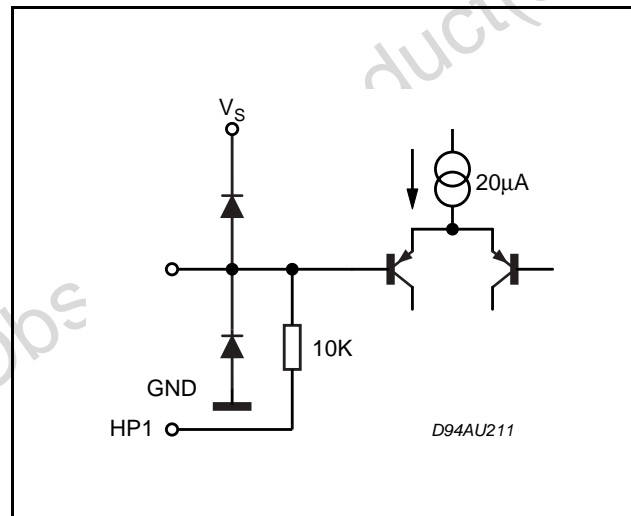


Figure 18. PIN: VAR-L, VAR-R,

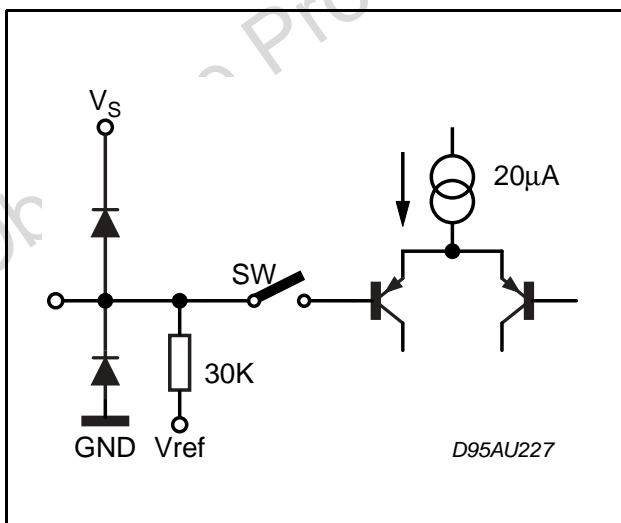


Figure 21. PIN: CREF

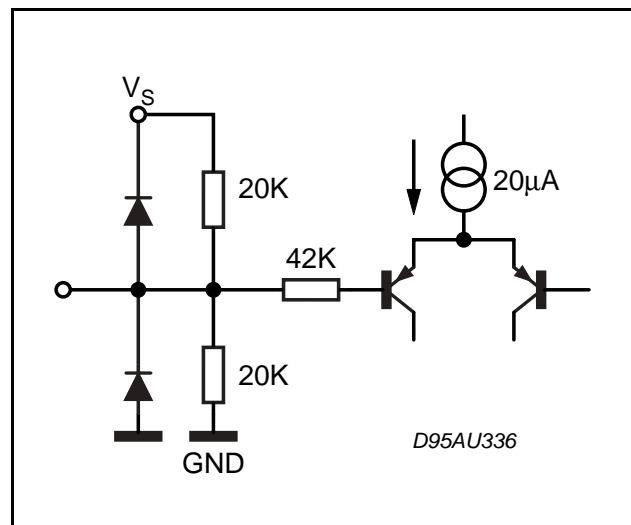


Figure 22. PIN: SCL, SDA

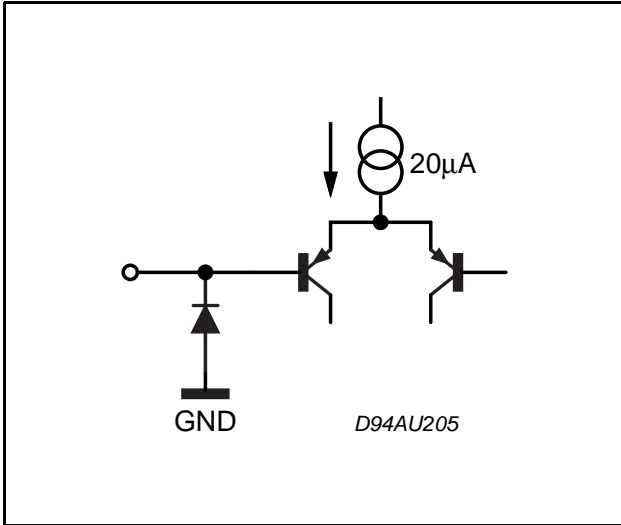


Figure 23. PIN: PS1, PS2, PS3, PS4, LP

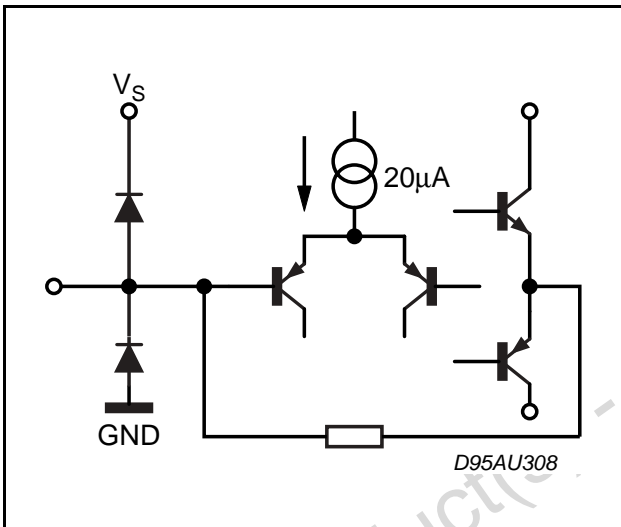


Figure 24. PIN: REARIN

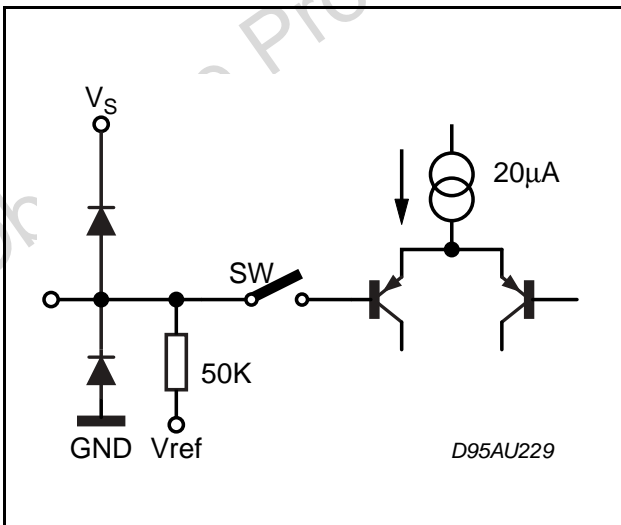


Figure 25. PIN: L-OUT, R-OUT, MONITOR-L, MONITOR-R REAROUT, BASSO-L, BASSO-R, AUXOUT_L, AUXOUT_R

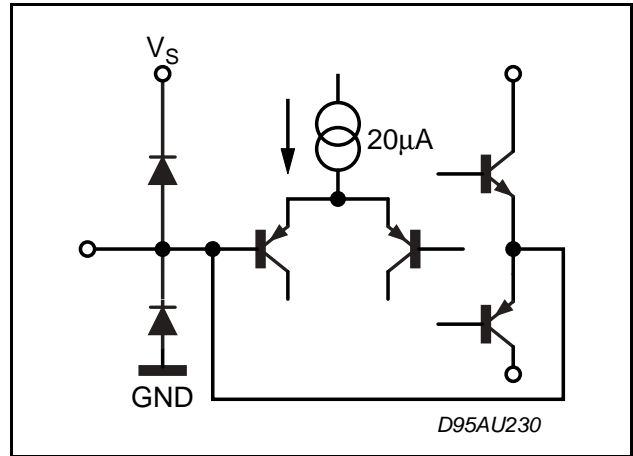


Figure 26. PIN: BASS-LI, BASS-RI, MIDDLE-LI, MIDDLE-RI,

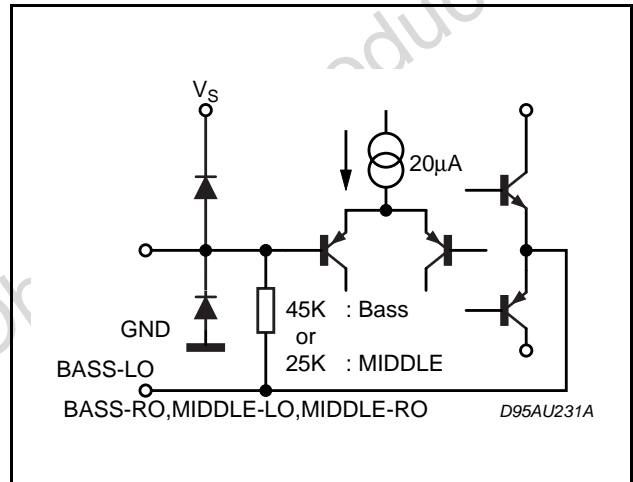


Figure 27. PIN: BASS-LO, BASS-RO, MIDDLE-LO, MIDDLE-RO,

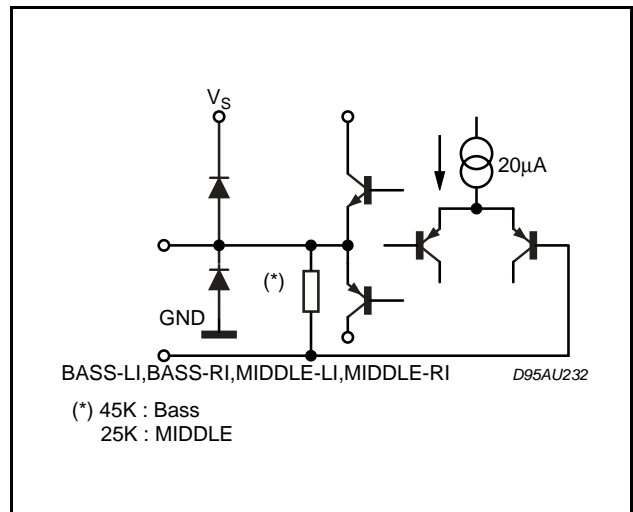
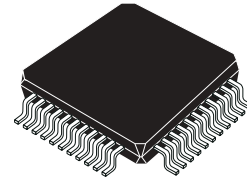


Figure 28. TQFP44 (10 x 10) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0° (min.), 3.5° (typ.), 7° (max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10 x 1.4mm)

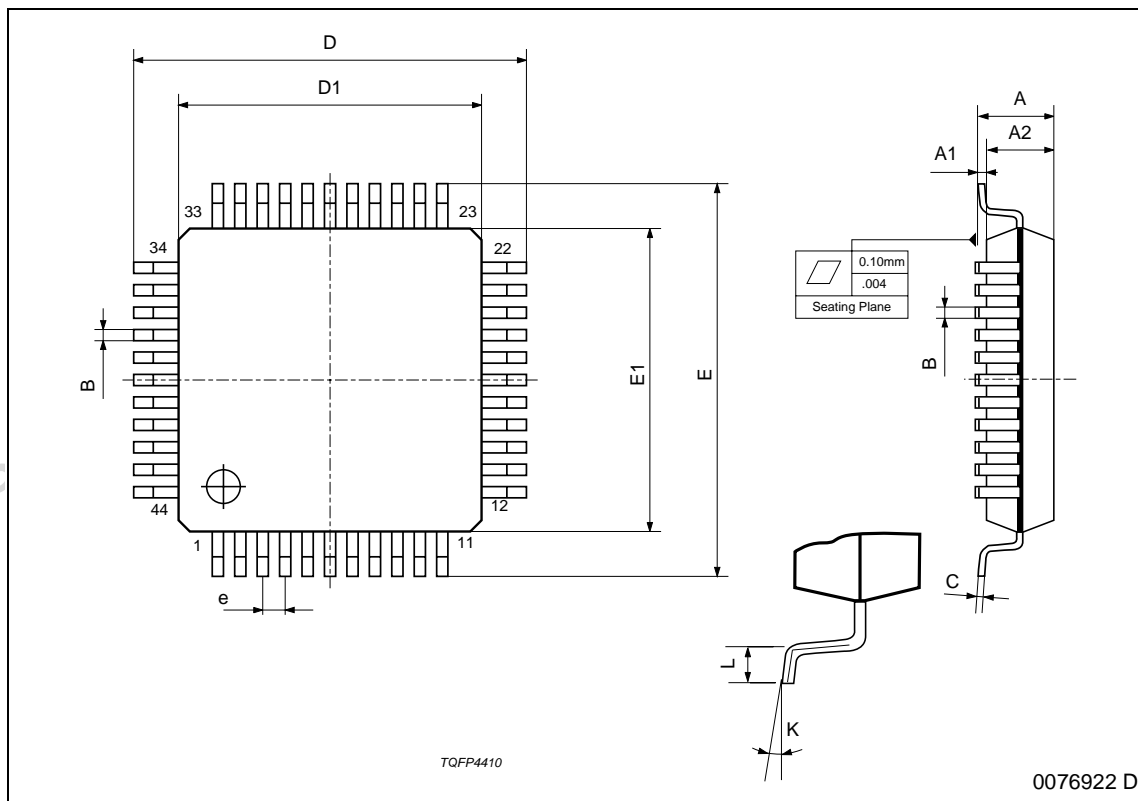
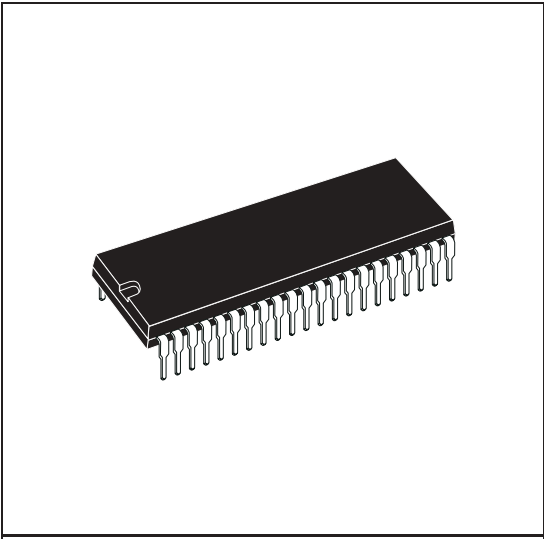


Figure 29. SDIP42 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.38	0.46	0.56	0.0149	0.0181	0.0220
B1	0.89	1.02	1.14	0.035	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	36.58	36.83	37.08	1.440	1.450	1.460
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140

OUTLINE AND MECHANICAL DATA



SDIP42 (0.600")

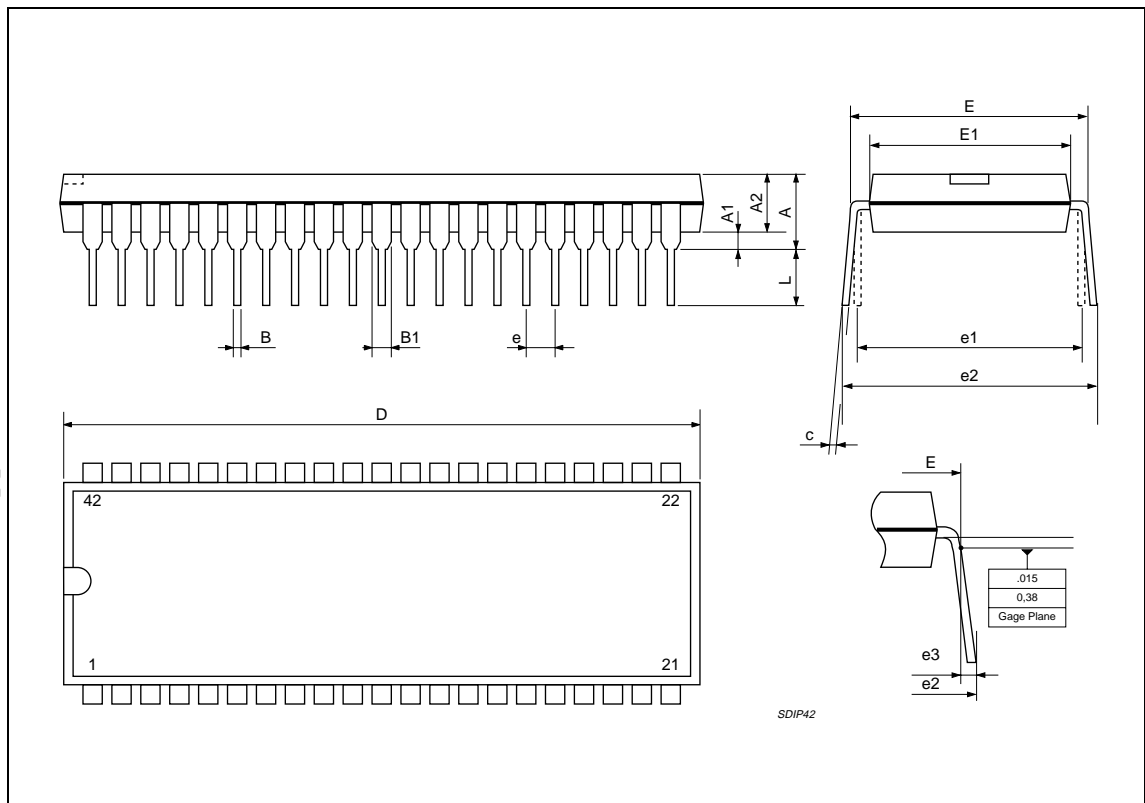


Table 16. Revision History

Date	Revision	Description of Changes
January 2004	5	First Issue in EDOCS DMS
June 2004	6	Changed the Style-sheet in compliance to the new "Corporate Technical Publications Design Guide"

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