Data Sheet | December 7, 2005 | FN6118.0

Multi-Channel Buffers Plus V_{COM} Driver

The ISL24003 integrates eighteen gamma buffers and a single V_{COM} buffer for use in large panel LCD displays of 10” and greater. Half of the gamma channels in each device are designed to swing to the upper supply rail, with the other half designed to swing to the lower rail. The output capability of each channel is 10mA continuous, with 120mA peak. The gamma buffers feature a 10MHz 3dB bandwidth specification and a 9V/µs slew rate.

The V_{COM} amplifier is designed to swing from rail to rail. The output current capability of the V_{COM} in the ISL24003 is 60mA continuous, 150mA peak, and a slew rate of 50V/µs.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG DWG. #
ISL24003IRZ (Note)	ISL24003IRZ	-	44 Ld 7x7mm QFN (Pb-free)	MDP0046
ISL24003IRZ-T7 (Note)	ISL24003IRZ	7”	44 Ld 7x7mm QFN (Pb-free)	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

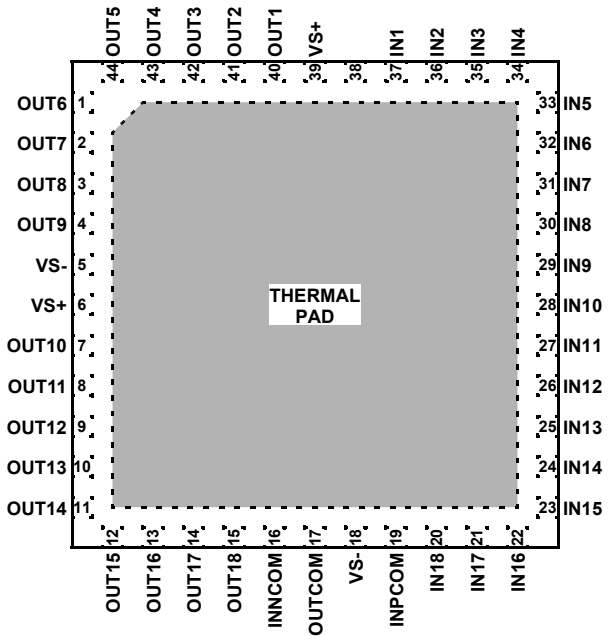
- 18-channel gamma buffers
  - 9 channels swing to the upper supply
  - 9 channels swing to the lower supply
  - 10mA continous output current
- Single V_{COM} amplifier
  - 180mA short circuit output current
  - 35MHz -3dB Bandwidth
  - 70V/µs slew rate
- Low supply current
- Pb-free plus anneal available (RoHS compliant)

Applications

- TFT-LCD monitors
- LCD televisions
- Industrial flat panel displays

Pinout

ISL24003
(44 LD 7X7MM QFN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and V_S- . . . . . +18V
Input Voltage . . . . . V_S- -0.5V, V_S+ +0.5V
Maximum Continuous Output Current ($V_{OUT1-18}$) 10mA
Maximum Continuous Output Current (V_{OUTA}) 60mA
Power Dissipation . . . . . See Curves
Maximum Die Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +15V, V_S- = 0, R_L = 10kΩ, C_L = 10pF to 0V, T_A = 25°C unless otherwise specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		2	20	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			10		MΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	1V ≤ V_{OUT} ≤ 14V	0.992		1.008	V/V
CMIR	Input Voltage Range	IN1 to IN9	1.5		V_S+	V
		IN10 to IN18	0		V_S+ -1.5	V
INPUT CHARACTERISTICS (V_{COM} BUFFER)						
V_{OS}	Input Offset Voltage	V_{CM} = 7.5V		1	15	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		3		µV/°C
I_B	Input Bias Current	V_{CM} = 7.5V		2	50	nA
R_{IN}	Input Impedance			10		MΩ
C_{IN}	Input Capacitance			1.35		pF
V_{REG}	Load Regulation	V_{COM} = 7.5V, -60mA < I_L < 60mA	-25		+20	mV
$CMIR_{COM}$	Input Voltage Range V_{COM}		0		V_S+	V
A_{VOL}	Open Loop Gain	R_L = 1kΩ	55	70		dB
CMRR	Common Mode Rejection Ratio		50	65		dB
OUTPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V_{OH}	High Output Voltage - (Output 1-2)	V_{IN} = 15V, I_O = 5mA	14.85	14.9		V
	High Output Voltage - (Output 3-9)		14.8	14.85		V
	High Output Voltage - (Output 10-18)	V_{IN} = 13.5V, I_O = 5mA	13.45	13.5		
V_{OL}	Low Output Voltage - (Output 1-9)	V_{IN} = 1.5V, I_O = 5mA		1.5	1.55	V
	Low Output Voltage - (Output 10-16)	V_{IN} = 0V, I_O = 5mA		150	200	mV
	Low Output Voltage - (Output 17-18)			100	150	mV
I_{SC}	Short Circuit Current		100	130		mA
OUTPUT CHARACTERISTICS (V_{COM} BUFFER)						
V_{OH}	High Level Saturated Output Voltage	V_S+ = 15V, I_O = -5mA, V_I = 15V	14.85	14.9		V
V_{OL}	Low Level Saturated Output Voltage	V_S+ = 15V, I_O = -5mA, V_I = 0V		0.1	0.15	V
I_{SC}	Short Circuit Current		150	180		mA

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Electrical Specifications $V_S+ = +15V$, $V_S- = 0$, $R_L = 10k\Omega$, $C_L = 10pF$ to 0V, $T_A = 25°C$ unless otherwise specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	Reference buffer V_S from 5V to 15V	50	80		dB
		V_{COM} buffer, V_S from 5V to 15V	55	80		dB
I_S	Total Supply Current		8.0	11.5	15.5	mA
DYNAMIC PERFORMANCE (BUFFER AMPLIFIERS)						
SR	Slew Rate (Note 2)		4.5	9		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 10pF$		10		MHz
CS	Channel Separation			70		dB
ISL24003 DYNAMIC PERFORMANCE (V_{COM} AMPLIFIERS)						
SR	Slew Rate (Note 2)	$-4V \le V_{OUT} \le 4V$, 20% to 80%	50	70		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		350		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 10pF$		35		MHz
CS	Channel Separation			70		dB

NOTES:

1. Measured over operating temperature range.
2. Slew rate is measured on rising and falling edges.

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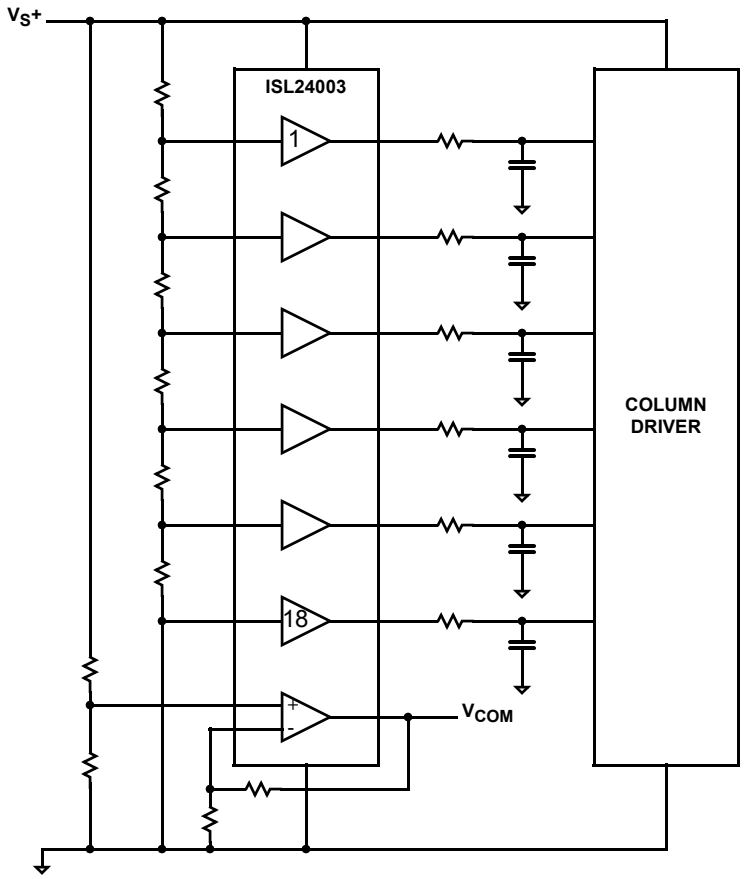
Pin Descriptions

PIN NAME	ISL24003	PIN FUNCTION
6, 39	VS+	Positive supply voltage
40-44, 1-4	OUT1-9	Output gamma channel 1-9
7-15	OUT10-18	Output gamma channel 10-18
16	INNCOM	Negative Input V_{COM}
17	OUTCOM	Output, V_{COM}
5,18	VS-	Negative supply voltage
19	INPCOM	Positive Input V_{COM}
20-28	IN10-18	Input gamma channel 10-18
29-37	IN1-9	Input gamma channel 1-9
38	NC	No connect

Block Diagram



NOTE: ISL24003 integrates 18 gamma buffers.

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Typical Performance Curves

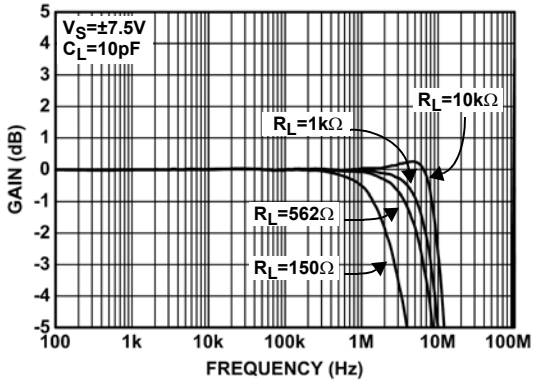

FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS R_{LOAD} (BUFFER)

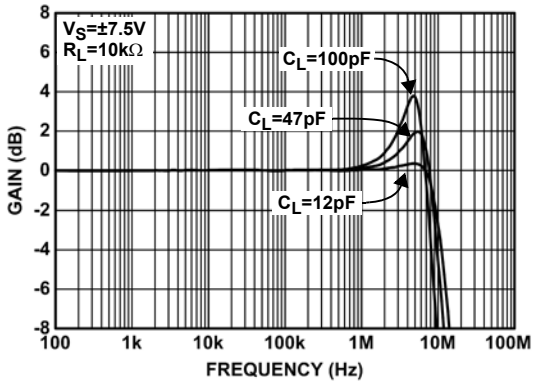

FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS C_{LOAD} (BUFFER)

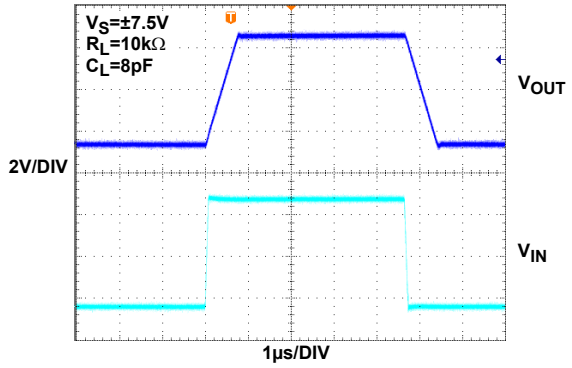

FIGURE 3. LARGE SIGNAL TRANSIENT RESPONSE (BUFFER)

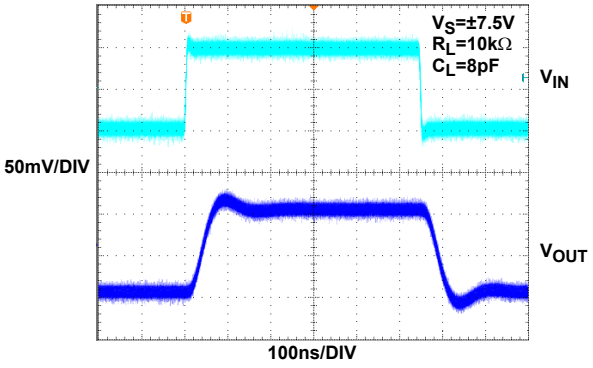

FIGURE 4. SMALL SIGNAL TRANSIENT RESPONSE (BUFFER)

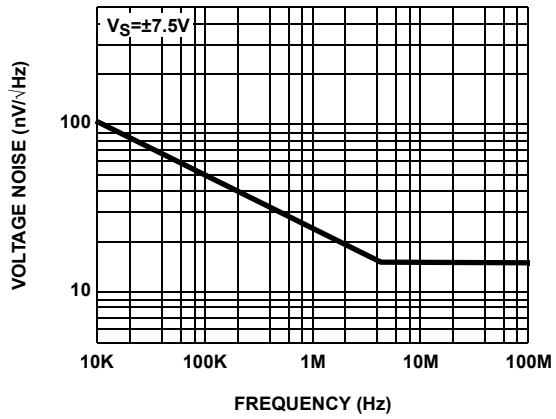

FIGURE 5. INPUT NOISE SPECIAL DENSITY vs FREQUENCY (BUFFER)

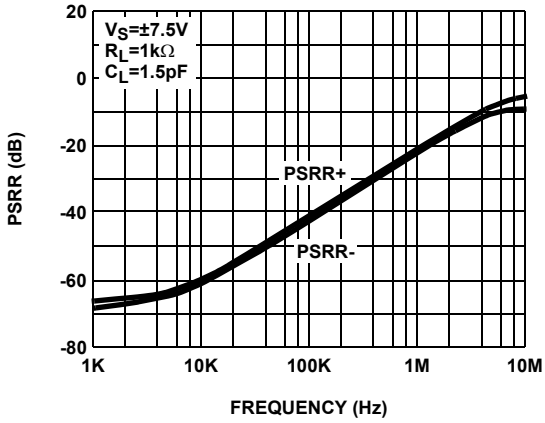

FIGURE 6. PSRR vs FREQUENCY (BUFFER)

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Typical Performance Curves (Continued)

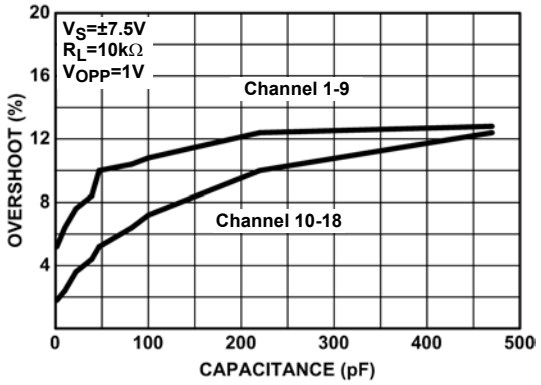

FIGURE 7. OVERSHOOT vs CAPACITANCE LOAD (BUFFER)

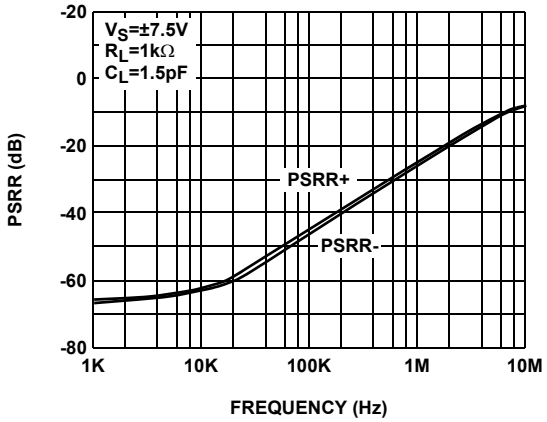

FIGURE 8. PSRR vs FREQUENCY (V_{COM})

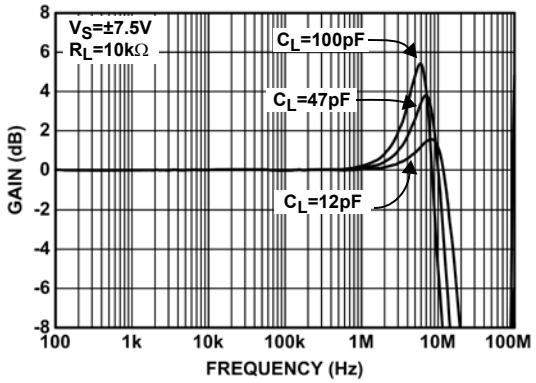

FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS C_{LOAD} (V_{COM})

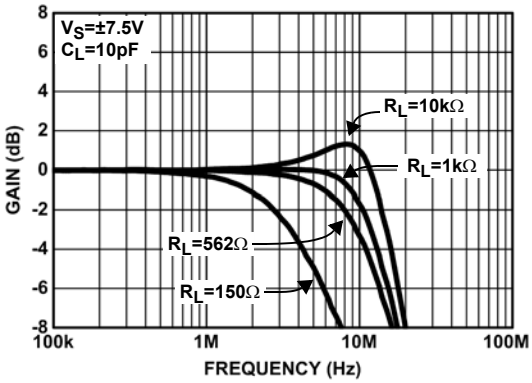

FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS R_{LOAD} (V_{COM})

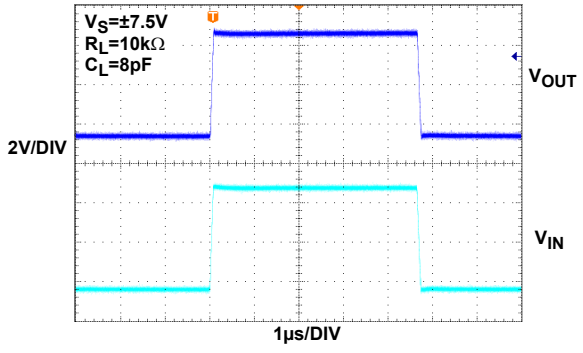

FIGURE 11. LARGE SIGNAL TRANSIENT RESPONSE (V_{COM})

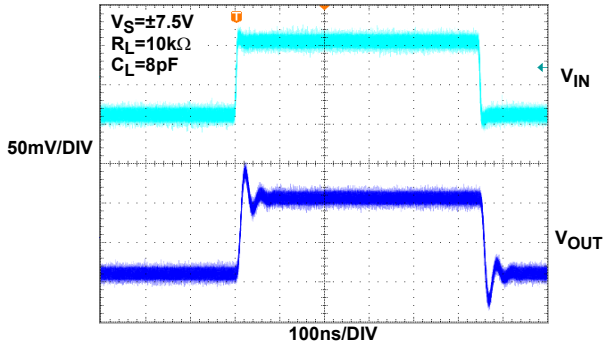

FIGURE 12. SMALL SIGNAL TRANSIENT RESPONSE (V_{COM})

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Typical Performance Curves (Continued)

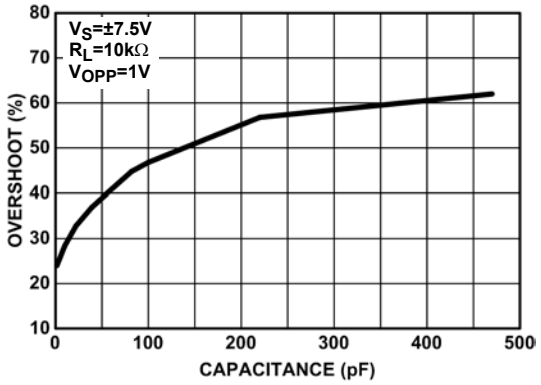

FIGURE 13. OVERSHOOT vs CAPACITANCE LOAD (V_{COM})

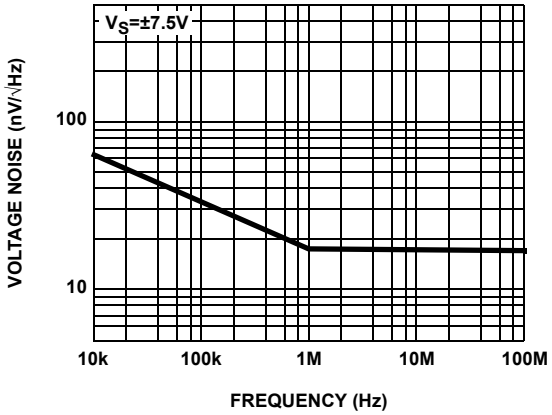

FIGURE 14. INPUT NOISE SPECIAL DENSITY vs FREQUENCY (V_{COM})

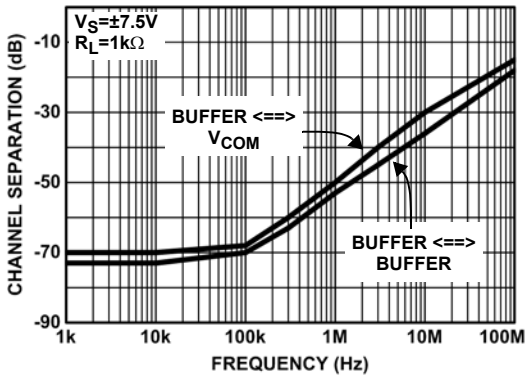

FIGURE 15. CHANNEL SEPARATION

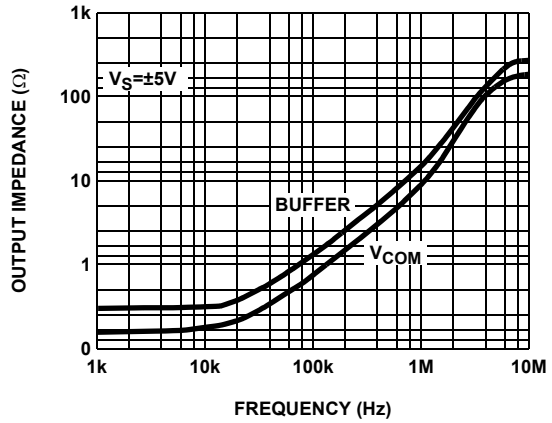

FIGURE 16. OUTPUT IMPEDANCE vs FREQUENCY

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Description of Operation and Application Information

Product Description

The ISL24003 are fabricated using a high voltage CMOS process. They exhibit rail to rail input and output capability and have very low power consumption. When driving a load of 10K and 12pF, the buffers have a -3dB bandwidth of 10MHz and exhibit 9V/µs slew rate. The V_{COM} amplifier has a -3dB bandwidth of 12MHz and exhibit 10V/µs slew rate.

Input, Output, and Supply Voltage Range

The ISL24003 are specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range from 4.5V to 16.5V.

The input common-mode voltage range of the ISL24003 within 500mV beyond the supply rails. The output swings of the buffers and V_{COM} amplifier typically extend to within 100mV of the positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage even closer to each supply rails.

Output Phase Reversal

The ISL24003 are immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Although the device's output will not change phase, the input's over-voltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diode placed in the input stage of the device begin to conduct and over-voltage damage could occur.

Output Drive Capability

The ISL24003 do not have internal short-circuit protection circuitry. The buffers will limit the short circuit current to 120mA and the V_{COM} amplifier will limit the short circuit current to 150mA if the outputs are directly shorted to the positive or the negative supply. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output continuous current never exceeds 10mA for the buffers and 60mA for the V_{COM} amplifier. These limits are set by the design of the internal metal interconnections.

The Unused Buffers

It is recommended that any unused buffers should have their inputs tied to ground plane.

Power Dissipation

With the high-output drive capability of the ISL24003, it is possible to exceed the 125°C “absolute-maximum junction temperature” under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the buffer to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = V_S \times I_S + \Sigma i \times [(V_S+ - V_{OUT}i) \times I_{LOAD}i] + (V_S+ - V_{OUT}) \times I_{LA}$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_S + \Sigma i \times [(V_{OUT}i - V_S-) \times I_{LOAD}i] + (V_{OUT} - V_S-) \times I_{LA}$$

when sinking.

where:

- i = 1 to total number of buffers
- V_S = Total supply voltage of buffer and V_{COM}
- I_{SMAX} = Total quiescent current
- $V_{OUT}i$ = Maximum output voltage of the application
- V_{OUT} = Maximum output voltage of V_{COM}
- $I_{LOAD}i$ = Load current of buffer
- I_{LA} = Load current of V_{COM}

If we set the two P_{DMAX} equations equal to each other, we can solve for the R_{LOAD}'s to avoid device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves.

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Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, one 0.1µF ceramic capacitor should be placed from the V_S+ pin to ground. A 4.7µF tantalum capacitor should then be connected from the V_S+ pin to ground. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Important Note: The metal plane used for heat sinking of the device is electrically connected to the negative supply potential (V_S-). If V_S- is tied to ground, the thermal pad can be connected to ground. Otherwise, the thermal pad must be isolated from any other power planes.

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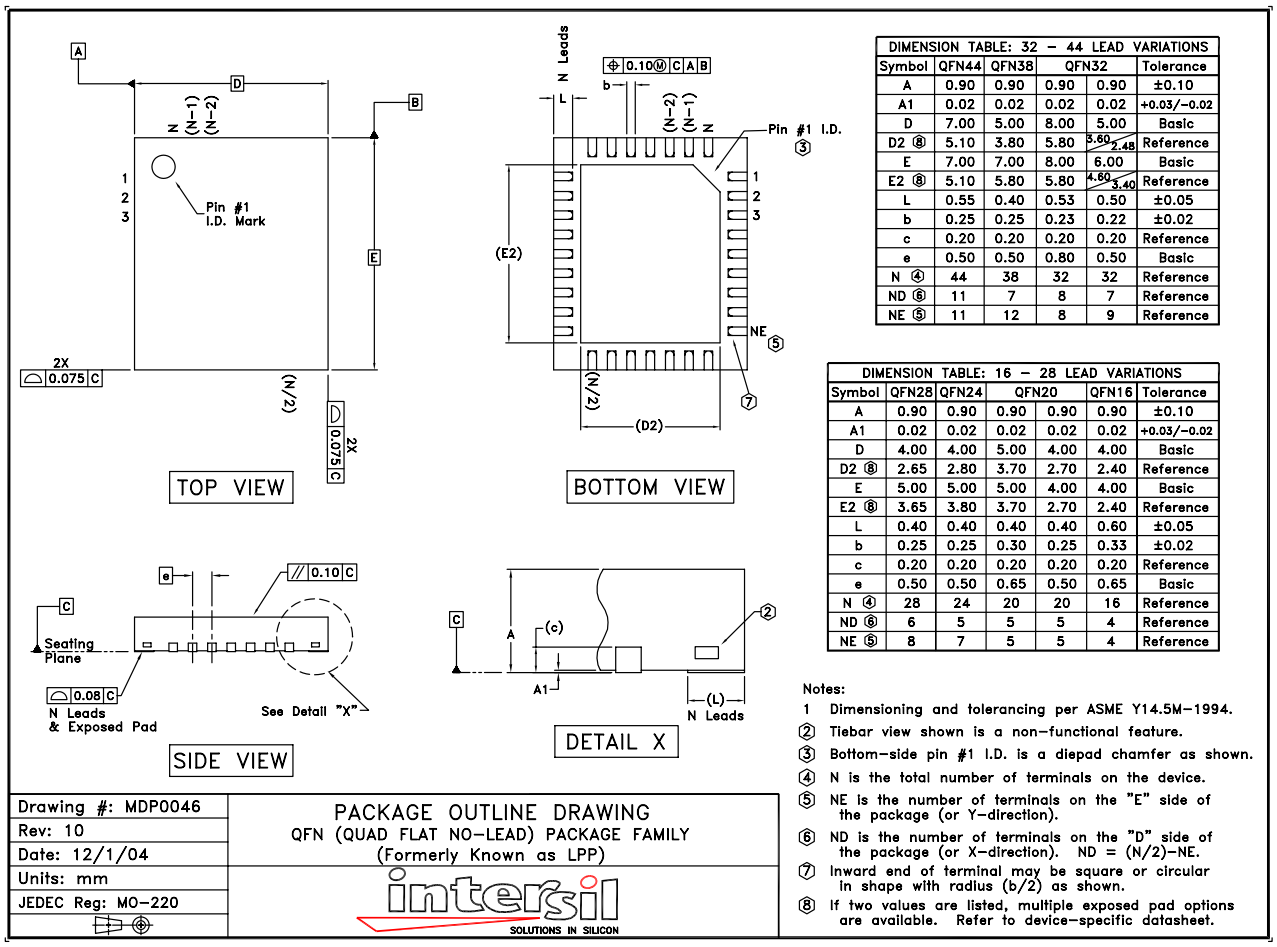
QFN Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32		Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/−0.02
D	7.00	5.00	8.00	5.00	Basic
D2 ⑧	5.10	3.80	5.80	3.60 / 2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 ⑧	5.10	5.80	5.80	4.60 / 3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N ④	44	38	32	32	Reference
ND ⑥	11	7	8	7	Reference
NE ⑤	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS						
Symbol	QFN28	QFN24	QFN20		QFN16	Tolerance
A	0.90	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	0.02	+0.03/−0.02
D	4.00	4.00	5.00	4.00	4.00	Basic
D2 ⑧	2.65	2.80	3.70	2.70	2.40	Reference
E	5.00	5.00	5.00	4.00	4.00	Basic
E2 ⑧	3.65	3.80	3.70	2.70	2.40	Reference
L	0.40	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.30	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.65	0.50	0.65	Basic
N ④	28	24	20	20	16	Reference
ND ⑥	6	5	5	5	4	Reference
NE ⑤	8	7	5	5	4	Reference

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Tiebar view shown is a non–functional feature.
3. Bottom–side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y–direction).
6. ND is the number of terminals on the "D" side of the package (or X–direction). ND = (N/2)–NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device–specific datasheet.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>

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