Rev 1; 10/08

MAXIM

I²C Gamma and V_{COM} Buffer with EEPROM

DS3514

General Description

The DS3514 is a programmable gamma and V_{COM} voltage generator that supports both real-time updating as well as multibyte storage of gamma/V_{COM} data in on-chip EEPROM memory. An independent 10-bit DAC, two 10-bit data registers, and four words of EEPROM memory are provided for each individually addressable gamma or V_{COM} channel. High-performance buffer amplifiers are integrated on-chip, providing rail-to-rail, low-power (400µA/gamma channel) operation. The V_{COM} channel features a high current drive (> 250mA peak) and a fast-settling buffer amplifier optimized to drive the V_{COM} node of a wide range of TFT-LCD panels.

Programming occurs through an I²C-compatible serial interface. Interface performance and flexibility are enhanced by a pair of independently loaded data latches per channel, as well as support for I²C speeds up to 400kHz. The multitable EEPROM memory enables a rich variety of display system enhancements, including support for temperature or light-level dependent gamma tables, enabling of factory or field automated display adjustment, and support for backlight dimming algorithms to reduce system power. Upon power-up and depending on mode, DAC data is selected from EEPROM by the S0/S1 pins or from a fixed memory address.

Applications

TFT-LCD Gamma and V_{COM} Buffer

Adaptive Gamma and V_{COM} Adjustment (Real Time by I²C, Select EEPROM Through I²C or S0/S1 Pins)

Industrial Process Control

Features

- **10-Bit Gamma Buffers, 14 Channels**
- **8-Bit V_{COM} Buffer, 1 Channel**
- **Four 10-Bit EEPROM Words per Channel**
- **Low-Power 400µA/ch Gamma Buffers**
- **I²C-Compatible Serial Interface**
- **Flexible Control from I²C or Pins**
- **9.0V to 15.0V Analog Supply**
- **2.7V to 5.5V Digital Supply**
- **48-Pin TQFN Package (7mm x 7mm)**

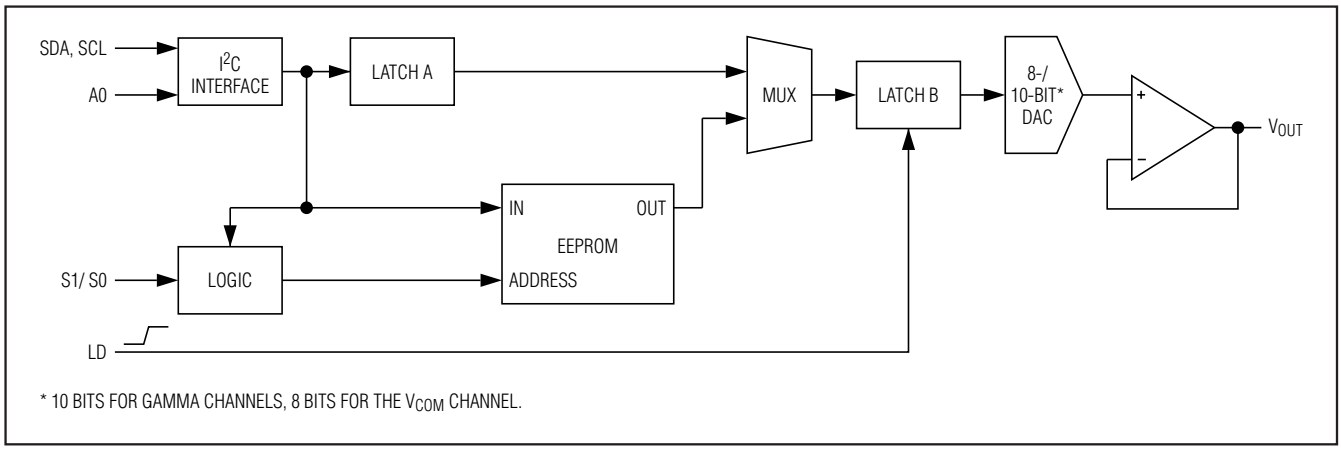
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3514T+	-45°C to +95°C	48 TQFN-EP*
DS3514T+T&R	-45°C to +95°C	48 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

Pin Configuration and Typical Operating Circuit appear at end of data sheet.

Gamma or V_{COM} Channel Functional Diagram



* 10 BITS FOR GAMMA CHANNELS, 8 BITS FOR THE V_{COM} CHANNEL.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

I²C Gamma and V_{COM} Buffer with EEPROM

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD} Relative to GND .....-0.5V to +16V
Voltage Range on VRL, VRH, GHH, GHM, GLM, GLL Relative to GND.....-0.5V to (V_{DD} + 0.5V), not to exceed 16V
Voltage Range on V_{CC} Relative to GND .....-0.5V to +6V
Voltage Range on SDA, SCL, A0, LD, S0, S1 Relative to GND .....-0.5V to (V_{CC} + 0.5V), not to exceed 6V

Junction Temperature.....+125°C
Operating Temperature Range .....-45°C to +95°C
Programming Temperature Range .....0°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -45°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage	V_{CC}	(Notes 1, 2)	2.7		5.5	V
Analog Supply Voltage	V_{DD}	(Note 1)	9.0		15.0	V
VRH, VRL Voltage	V_{VCOM}	Applies to V_{COM} output	2.0		V_{DD} - 2.0	V
GHH, GHM, GLM, GLL Voltage	$V_{GM1–14}$	Applies to GM1–GM14	GND + 0.2		V_{DD} - 0.2	V
Input Logic 1 (SCL, SDA, A0, S0, S1, LD)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SCL, SDA, A0, S0, S1, LD)	V_{IL}		-0.3		0.3 x V_{CC}	V
V_{COM} Load Capacitor	C_D		1			µF
VCAP Compensation Capacitor	C_{COMP}		0.1			µF

INPUT ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -45°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (SDA, SCL, A0, S0, S1, LD)	I_L		-1		+1	µA
V_{DD} Supply Current	I_{DD}	(Note 3)		5	10	mA
V_{CC} Supply Current, Nonvolatile Read or Write	I_{CC}	(Note 4)		0.25	0.6	mA
V_{CC} Standby Supply Current	I_{CCQ}	(Note 5)		10	30	µA
V_{DD} Standby Supply Current	I_{DDQ}	(Note 6)		450	850	µA
I/O Capacitance (SDA, SCL, LD, S0, S1, A0)	$C_{I/O}$	Guaranteed by design		5	10	pF
End-to-End Resistance (VRH to VRL)	R_{TOTAL}			16		kΩ
R_{TOTAL} Tolerance		T_A= +25°C°	-20		+20	%

INPUT ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -45°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Resistance (GHH, GHM, GLM, GLL)				75		kΩ
Input Resistance Tolerance		T_A= +25°C	-20		+20	%
Power-On Recall Voltage	V_{POR}	(Note 7)	1.6		2.6	V
Power-Up Time	t_D	(Note 8)		25		ms

OUTPUT ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, VRL = +2.0V, GLL = +0.2V, GLM = +4.8V, GHM = +10.2V, VRH = +13.0V, GHH = +14.8V, T_A = -45°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GM1–GM14 DAC Resolution			10			Bits
V_{COM} DAC Resolution			8			Bits
V_{COM} Integral Nonlinearity Error	INL	T_A= +25°C (Note 9)	-0.5		+0.5	LSB
V_{COM} Differential Nonlinearity Error	DNL	T_A= +25°C (Note 10)	-0.5		+0.5	LSB
GM1–GM14 Integral Nonlinearity Error	INL	T_A= +25°C (Note 9)	-1.0		+1.0	LSB
GM1–GM14 Differential Nonlinearity Error	DNL	T_A= +25°C (Note 10)	-0.35		+0.35	LSB
Output Voltage Range (V_{COM})			2.0		V_{DD} - 2.0	V
Output Voltage Range (GM1–G14)			0.2		V_{DD} - 0.2	V
V_{COM} Output Accuracy		T_A= +25°C	-20		+20	mV
GM1–GM14 Offset		GM outputs = V_{DD}/2, T_A= +25°C		37		mV
GM1–GM14 Output Accuracy		GM outputs = V_{DD}/2, T_A= +25°C	-35		+35	mV
Voltage Gain (GM1–GM14)			0.995			V/V
Load Regulation (V_{COM}, GM1–GM14)				1.0		mV/mA
Short-Circuit Current (V_{COM})		To V_{DD} or GND	250			mA
S0/S1 to LD Setup Time	t_{SU}	Figure 2		37.5		ns
S0/S1 to LD Hold Time	t_{HD}	Figure 2		37.5		ns
V_{COM} Settling Time from LD Low to High (S0/S1 Meet t_{SU})	t_{SET-V}	Settling to 0.1% of final V_{COM} level (Figure 1) (Note 11)		2.0		µs
GM1–GM14 Settling Time from LD Low to High	t_{SET-G}	4t_{AU} settled with I_{LOAD}= ±20mA (Figure 2) (Notes 11, 12, 13)			5.0	µs
S0, S1 to GM1–GM14 Output 10% Settled	t_{SEL}	10% settling (Figure 3), LD = V_{CC} (asynchronous) (Notes 11, 13)			600	ns

I²C ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -45°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$. See Figure 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 14)	0		400	kHz
Bus-Free Time between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 15)	$20 + 0.1C_B$		300	ns
SDA and SCL Fall Time	t_F	(Note 15)	$20 + 0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 15)			400	pF
EEPROM Write Time	t_W	(Note 16)			20	ms
Pulse-Width Suppression Time at SDA and SCL Inputs	t_{IN}	(Note 17)			50	ns
A0 Setup Time	$t_{SU:A}$	Before START	0.6			µs
A0 Hold Time	$t_{HD:A}$	After STOP	0.6			µs
SDA and SCL Input Buffer Hysteresis			$0.05 \times V_{CC}$			V
Input Capacitance on A0, SDA, or SCL	C_I			5	10	pF
Low-Level Output Voltage (SDA)	V_{OL}	4mA sink current			0.4	V
SCL Falling Edge to SDA Output Data Valid	t_{AA}	SCL falling through $0.3 \times V_{CC}$ to SDA exit $0.3 \times V_{CC}$ to $0.7 \times V_{CC}$ window			900	ns
Output Data Hold	t_{DH}	SCL falling through $0.3 \times V_{CC}$ until SDA in $0.3 \times V_{CC}$ to $0.7 \times V_{CC}$ window	0			ns

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
EEPROM Write Cycles		T_A = +85°C (Guaranteed by design)	50,000		Writes
		T_A = +25°C (Guaranteed by design)	200,000		

Note 1: All voltages are referenced to ground. Currents entering the IC are specified positive and currents exiting the IC are negative.

Note 2: If V_{CC} is less than +2.7V or is left unconnected, the DS3514 pulls the I²C bus to V_{CC}, preventing communication with other devices on the I²C bus.

Note 3: I_{DD} supply current is specified with V_{DD} = 15.0V and no load on V_{COM} or GM1–GM14 outputs.

Note 4: I_{CC} is specified with the following conditions: SCL = 400kHz, SDA = V_{CC} = 5.5V, and V_{COM} and GM1–GM14 floating.

Note 5: I_{CCQ} is specified with the following conditions: SCL = SDA = V_{CC} = 5.5V, and V_{COM} and GM1–GM14 floating.

Note 6: I_{DDQ} is specified with the following conditions: SCL = SDA = V_{CC} = 5.5V and V_{COM} and GM1–GM14 floating.

Note 7: This is the minimum V_{CC} voltage that causes EEPROM to be recalled.

Note 8: This is the time from $V_{CC} > V_{POR}$ and $V_{DD} > V_{DD(MIN)}$ until the device is powered up.

Note 9: Integral nonlinearity is the deviation of a measured value from the expected values at each particular setting. Expected value is calculated by connecting a straight line from the measured minimum setting to the measured maximum setting. INL = $[V(RW)_i - (V(RW)_0]$/LSB(measured) - i, for i = 0...N (N = 255 for V_{COM}, 1023 for GM1–GM14).

Note 10: Differential nonlinearity is the deviation of the step-size change between two LSB settings from the expected step size. The expected LSB step size is the slope of the straight line from measured minimum position to measured maximum position. DNL = $[V(RW)_{i+1} - (V(RW)_i]$/LSB(measured) - 1, for i = 0...(N - 1) (N = 255 for V_{COM}, 1023 for GM1–GM14).

Note 11: Specified with the V_{COM} and gamma bias currents set to 100% (CR.5 = 1, CR.4 = 0).

Note 12: EEPROM data is assumed already settled at input of Latch B. LD transitions after EEPROM byte has been selected.

Note 13: Rising transition from 5V to 10V; falling transition from 10V to 5V.

Note 14: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I²C standard-mode timing.

Note 15: C_B—total capacitance of one bus line in picofarads.

Note 16: EEPROM write time begins after a STOP condition occurs.

Note 17: Pulses narrower than max are suppressed.

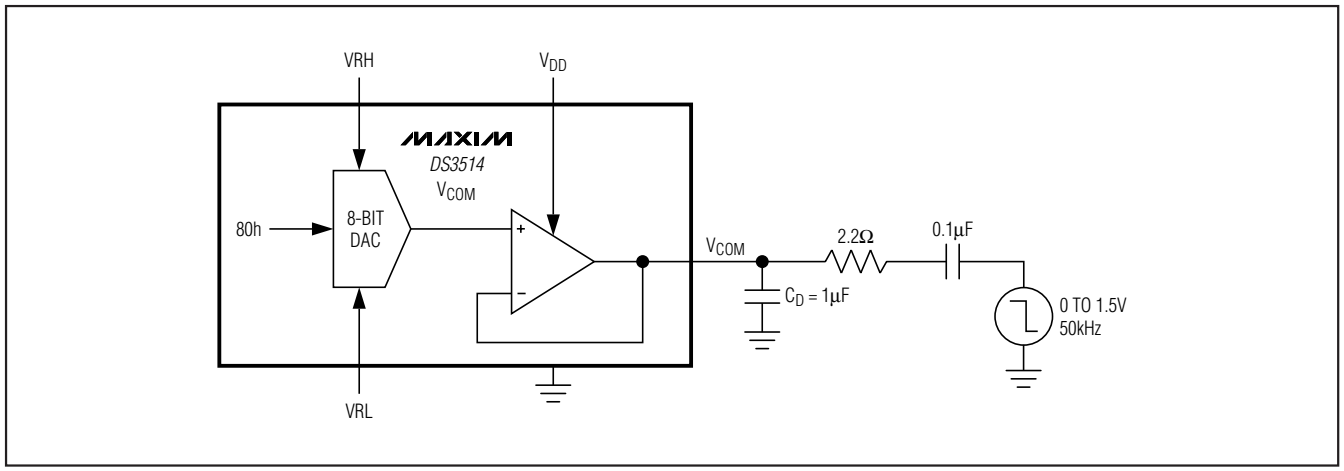


Figure 1. V_{COM} Settling Timing Diagram

I²C Gamma and VCOM Buffer with EEPROM

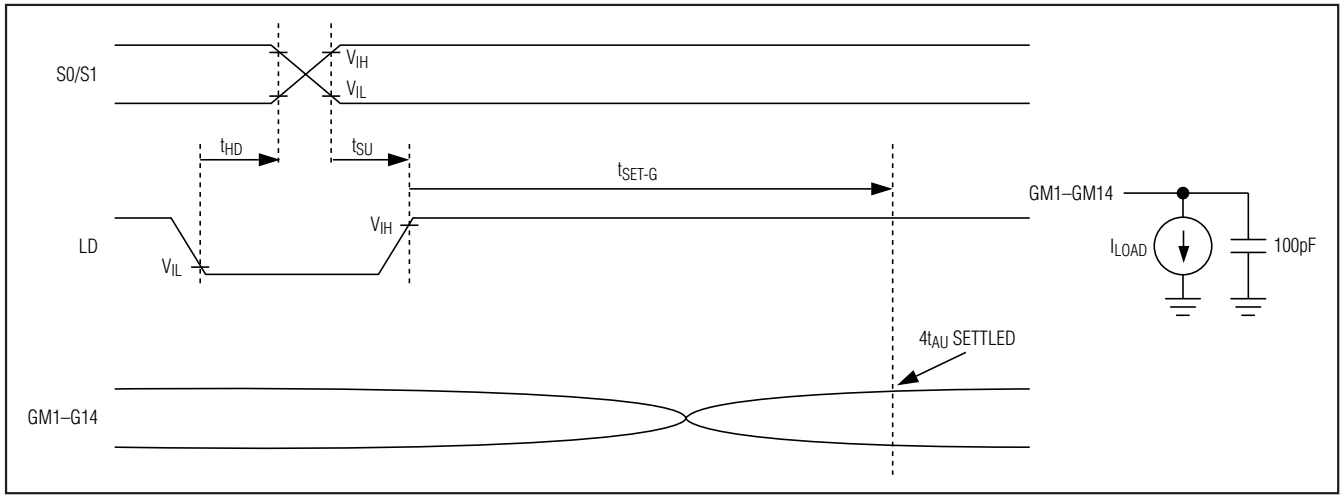


Figure 2. GM1–GM14 Settling Timing Diagram

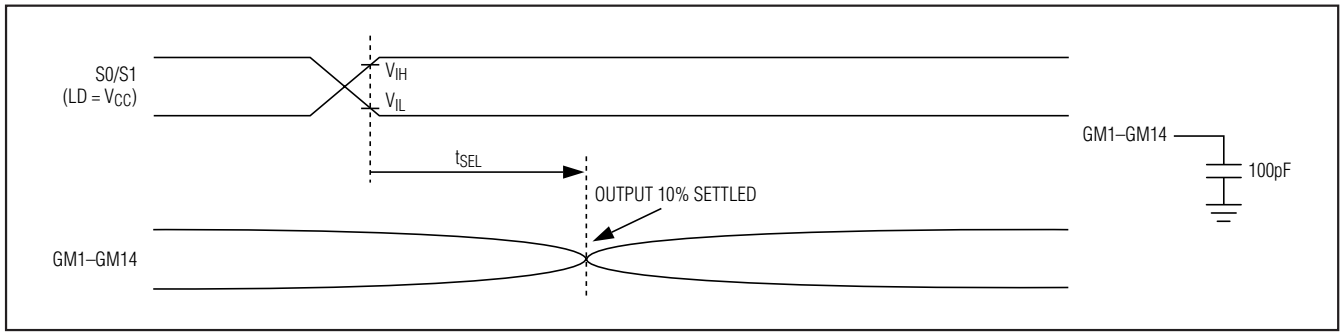
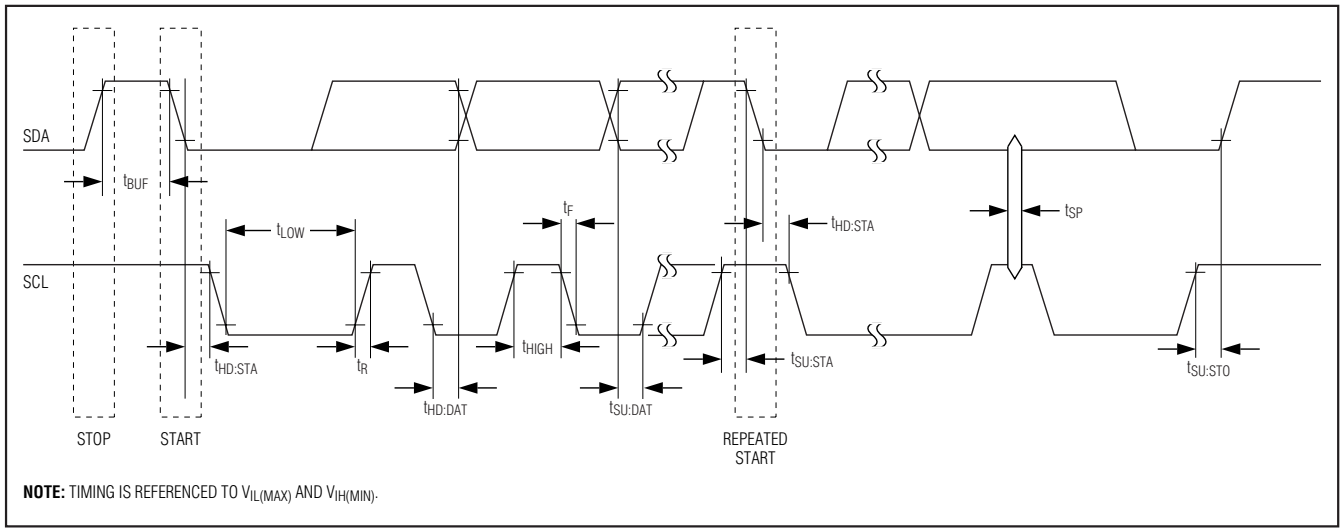


Figure 3. Input Pin to Output Change Timing Diagram



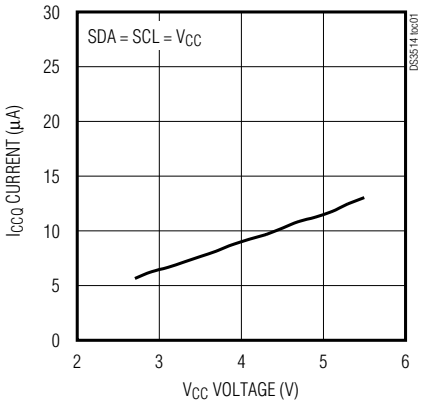
NOTE: TIMING IS REFERENCED TO $V_{IL(MAX)}$ AND $V_{IH(MIN)}$.

Figure 4. I²C Timing Diagram

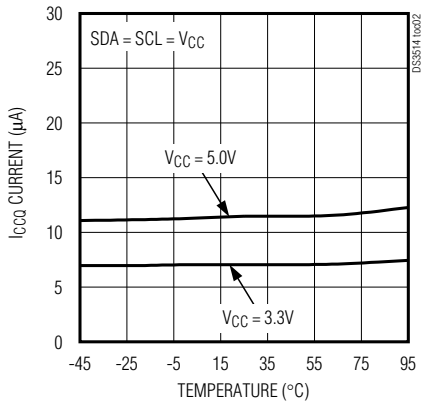
Typical Operating Characteristics

(V_{CC} = +5.0V, V_{DD} = +15V, T_A = +25°C, unless otherwise noted.)

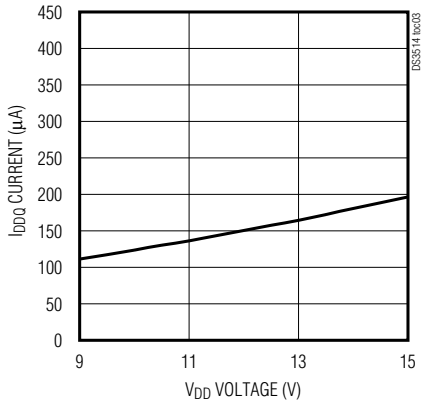
DIGITAL SUPPLY STANDBY CURRENT vs. V_{CC}



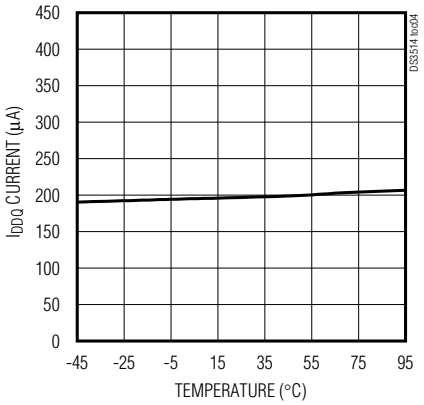
DIGITAL SUPPLY STANDBY CURRENT vs. TEMPERATURE



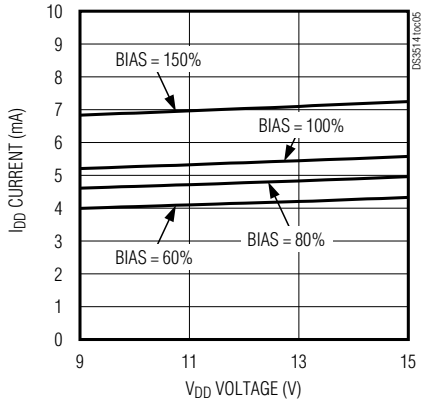
ANALOG SUPPLY STANDBY CURRENT vs. V_{DD}



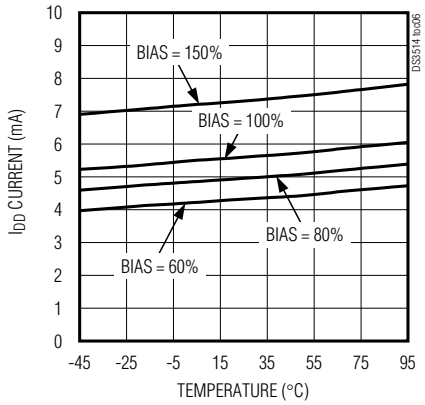
ANALOG SUPPLY STANDBY CURRENT vs. TEMPERATURE



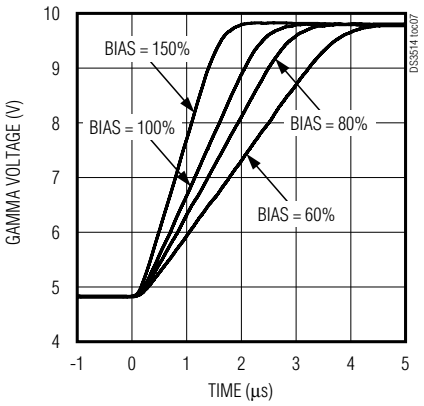
ANALOG SUPPLY CURRENT vs. V_{DD}



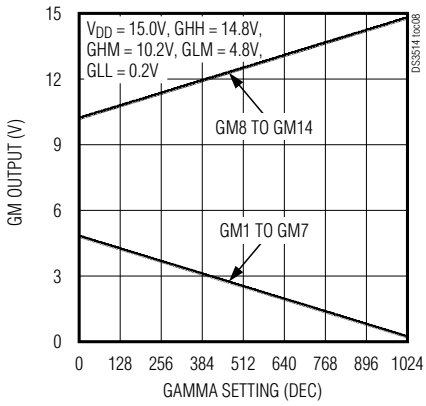
ANALOG SUPPLY CURRENT vs. TEMPERATURE



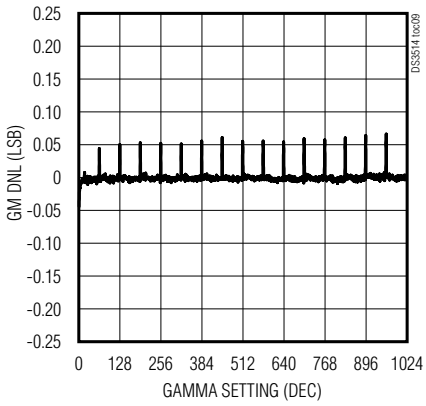
GAMMA SETTLING



GAMMA OUTPUT vs. SETTING



GM DNL

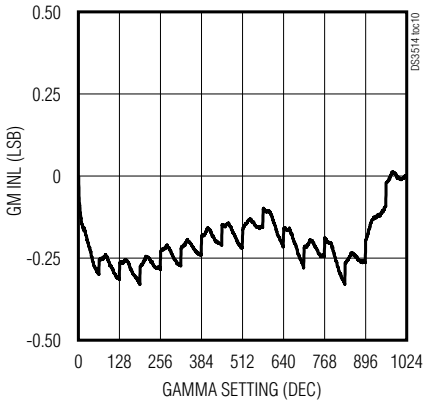


I²C Gamma and VCOM Buffer with EEPROM

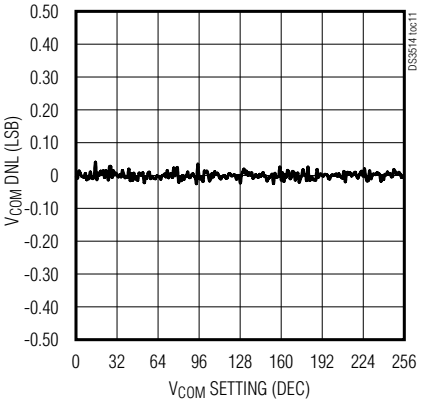
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, V_{DD} = +15V, T_A = +25°C, unless otherwise noted.)

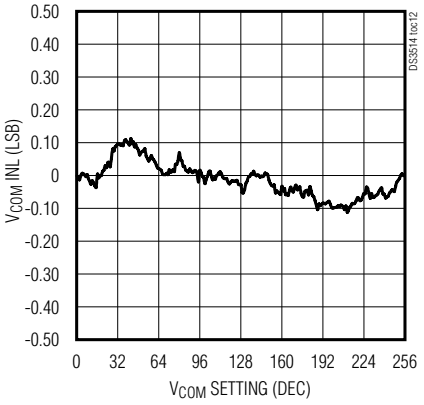
GM INL



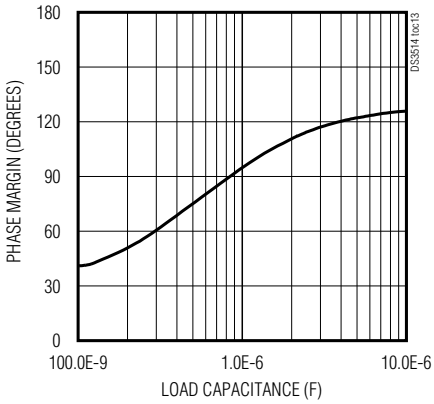
VCOM DNL



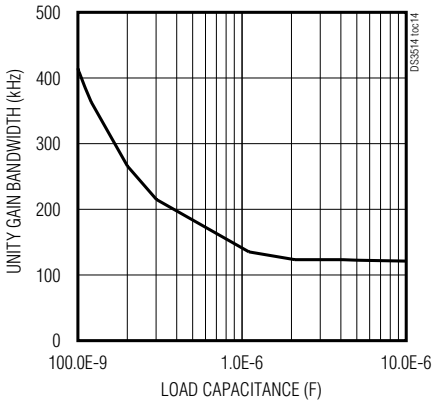
VCOM INL



VCOM PHASE MARGIN vs. LOAD CAPACITANCE



VCOM UNITY GAIN BANDWIDTH vs. LOAD CAPACITANCE

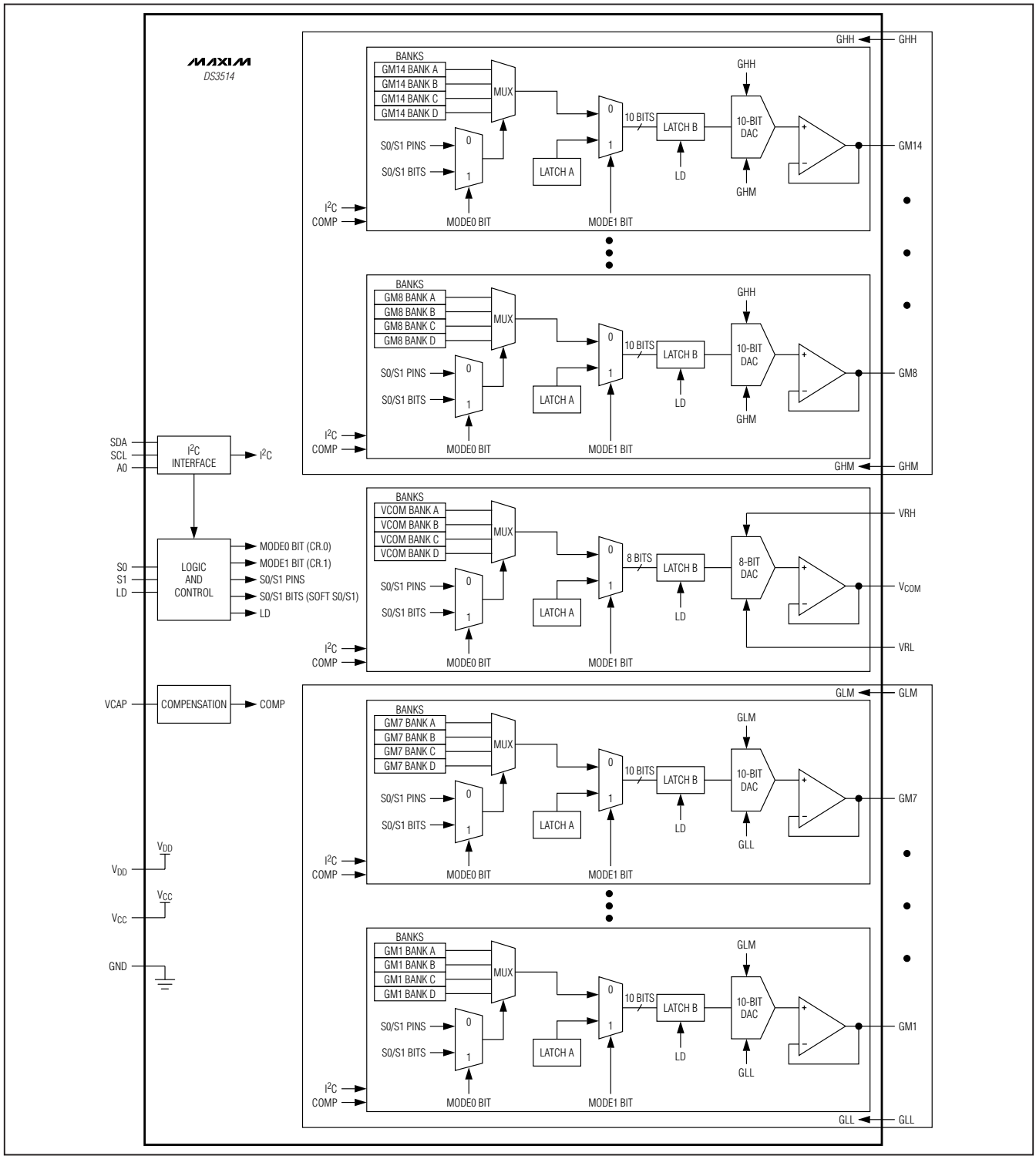


Pin Description

PIN	NAME	TYPE	FUNCTION
1–5, 9, 10, 46, 48	N.C.	—	No Connection
6, 23, 43	V_{DD}	Power	Analog Supply (9.0V to 15.5V)
7	VRH	Ref Input	High-Voltage Reference for V_{COM} DAC
8	VRL	Ref Input	Low-Voltage Reference for V_{COM} DAC
11, 18, 19, 21, 22, 42	GND	Power	Ground
12	S1	Input	Select Inputs. When the Control register [1,0] = 00, S0 and S1 are used to select DAC input data from EEPROM.
13	S0	Input	
14	LD	Input	Latch Data Input. When LD is low, Latch B retains existing data (acts as a latch). When LD is high, the input to Latch B data flows through to the output and updates the DACs asynchronously.
15	SDA	Input/Output	I²C Serial Data Input/Output
16	SCL	Input	I²C Serial Clock Input
17, 47	V_{CC}	Power	Digital Supply (2.7V to 5.5V)
20	VCAP	Input	Compensation Capacitor Input. Connect VCAP to GND through a 0.1µF capacitor.
24–30	GM1–GM7	Output	Low-Voltage Gamma Analog Outputs
31–37	GM8–GM14	Output	High-Voltage Gamma Analog Outputs
38	GLM	Ref Input	Reference for Low-Voltage Gamma DAC
39	GLL	Ref Input	Reference for Low-Voltage Gamma DAC
40	GHM	Ref Input	Reference for High-Voltage Gamma DAC
41	GHH	Ref Input	Reference for High-Voltage Gamma DAC
44	V_{COM}	Output	V_{COM} Analog Output. This output requires a 1µF capacitor to GND.
45	A0	Input	Address Input. This pin determines the DS3514's I²C slave address.
EP	GND	—	Ground. Exposed Pad. Connect to GND.

I²C Gamma and VCOM Buffer with EEPROM

Block Diagram



Detailed Description

The DS3514 operates in one of three modes that determine how the V_{COM} and gamma DACs are controlled/updated. The first two modes allow "banked" control of the 14 gamma channels and one V_{COM} channel. Depending on the mode, one of four banks (in EEPROM) can be selected using either the S0/S1 pins or using the SOFT S0/S1 bits in the Soft S0/S1 register. Once a bank is selected, the LD pin can then be used to simultaneously update each channel's DAC output. The third and final mode is not banked. It allows I²C control of each channel's Latch A register that is SRAM (volatile), allowing quick and unlimited updates. In this mode, the LD pin can also be used to simultaneously update each channel's DAC output. A detailed description of the three modes as well as additional features of the DS3514 follows.

Mode Selection

The DS3514 mode of operation is determined by two bits located in Control register (CR, register 48h), which is nonvolatile (NV) (EEPROM). In particular, the mode is determined by the MODE0 bit (CR.0) and the MODE1 bit (CR.1). Table 1 illustrates how the two control bits are used to select the operating mode. When shipped from the factory, the DS3514 is programmed with both MODE bits set to zero.

S0/S1 Pin-Controlled Bank-Updating Mode

As shown in the *Block Diagram*, each channel contains four words of EEPROM that are used to implement the "banking" functionality. Each bank contains unique DAC settings for each channel. When the DS3514 is configured in this operating mode, the desired bank is selected using the S0 and S1 pins as shown in Table 2 where 0 is ground and 1 is V_{CC}. For example, if S0 and S1 are both connected to ground, the first bank (Bank A) is selected. Once a bank is selected, the timing of the DAC update depends on the state of LD pin. When LD is high, Latch B functions as a flow-through latch, so the amplifier responds asynchronously to changes in the state of S0/S1 to meet the t_{SEL} specification. Conversely, when LD is low, Latch B functions as a latch, holding its previous data. A low-to-high transition on LD allows the Latch B input data to flow through and update the DACs with the EEPROM bank selected by S0/S1. A high-to-low transition on LD latches the selected DAC data into Latch B.

SOFT S0/S1 Bit-Controlled Bank-Updating Mode

This mode also features banked operation with the only difference being how the desired bank is selected. In particular, the bank is selected using the SOFT S0 (bit 0) and SOFT S1 (bit 1) bits contained in the Soft S0/S1 register (40h). The S0 and S1 pins are ignored in this mode. Table 2 illustrates the relationship between the bit settings and the selected bank. For example, if SOFT S0 and SOFT S1 are written to zero, the first bank (Bank A) is selected. Once a bank is selected, the timing of the DAC update depends on the state of the LD pin. When LD is high, Latch B functions as a flow-through latch, so the amplifier responds asynchronously to changes in the state of the SOFT S0/S1 bits. These are changed by an I²C write. Conversely, when LD is low, Latch B functions as a latch, holding its previous data. A low-to-high transition on LD allows the Latch B input data to flow through and update the DACs with the EEPROM bank selected by the SOFT S0/S1 bits. A high-to-low transition on LD latches the selected DAC data into Latch B.

Because the Soft S0/S1 register is SRAM, subsequent power ups result in the SOFT S0 and SOFT S1 bits being cleared to 0 and, hence, powering up to Bank A.

I²C Individual Channel-Control Mode

In this mode the I²C master writes directly to individual channel Latch A registers to update a single DAC (i.e., not banked). The Latch A registers are SRAM and not EEPROM. This allows an unlimited number of write cycles as well as quicker write times since t_W only applies to EEPROM writes. As shown in the *Memory*

Table 1. Operating Modes

MODE1 BIT (CR.1)	MODE0 BIT (CR.0)	MODE
0	0	S0/S1 Pin-Controlled Bank Updating (Factory Default)
0	1	S0/S1 Bit-Controlled Bank Updating
1	X	I²C Individual Channel Control

Table 2. Bank Selection Table

BIT OR PIN		VCOM CHANNEL	GAMMA CHANNELS
S1	S0		
0	0	V_{COM} Bank A	GM1–GM14 Bank A
0	1	V_{COM} Bank B	GM1–GM14 Bank B
1	0	V_{COM} Bank C	GM1–GM14 Bank C
1	1	V_{COM} Bank D	GM1–GM14 Bank D

I²C Gamma and VCOM Buffer with EEPROM

Map, the Latch A registers for each channel are accessed through memory addresses 00–1Ch. Then, like the other modes, the LD pin determines when the DACs are updated. If the LD signal is high, Latch B is flow-through and the DAC is updated immediately. If LD is low, Latch B is loaded from Latch A after a low-to-high transition on the LD pin. This latter method allows the timing of the DAC update to be controlled by an external signal pulse.

VCOM/Gamma Channel Outputs

As illustrated in the *Block Diagram*, the gamma channel outputs are equivalent to a 10-bit digital potentiometer (DAC) with a buffered output. The V_{COM} channel is equivalent to an 8-bit digital potentiometer (DAC) with a buffered output. The V_{COM} channel's digital potentiometer is composed of 255 equal resistive elements. The relationship between output voltage and DAC setting is illustrated in Table 3a. Unlike the gamma channels, the V_{COM} channel is capable of outputting a range of voltages including both references (VRH and VRL). Each of the gamma channel digital potentiometers, on the other hand, are composed of 1024 equal resistive elements. The extra resistive element prohibits one of the rails from being reached. In particular, gamma channel outputs GM1–GM7 can span from (and including) GLL to 1 LSB away from GLM. Likewise, gamma channel outputs GM8–GM14 span from (and including) GHM to 1 LSB away from GHH. The relationship between output voltage and DAC setting for the gamma channels are also illustrated in Table 3b.

Table 3a. VCOM DAC Voltage/Data Relationship for Selected Codes

SETTING (HEX)	VCOM OUTPUT VOLTAGE
00h	VRL
01h	VRL + (1/255) x (VRH - VRL)
02h	VRL + (2/255) x (VRH - VRL)
03h	VRL + (3/255) x (VRH - VRL)
0Fh	VRL + (15/255) x (VRH - VRL)
3Fh	VRL + (63/255) x (VRH - VRL)
7Fh	VRL + (127/255) x (VRH - VRL)
FDh	VRL + (253/255) x (VRH - VRL)
FEh	VRL + (254/255) x (VRH - VRL)
FFh	VRH

Standby Mode

Standby mode (not to be confused with the three DS3514 operating modes) can be used to minimize current consumption. Standby mode is entered by setting the STANDBY bit, which is the MSB of register 41h. The V_{COM} and gamma outputs are placed in a high-impedance state. Current drawn from the V_{DD} supply in this state is specified as I_{DDQ}.

The DS3514 continues to respond to I²C commands, and thus draws some current from V_{CC} when I²C activity is occurring. When the I²C interface is inactive, current drawn from the V_{CC} supply is specified as I_{CCQ}.

Thermal Shutdown

As a safety feature, the DS3514 goes into a thermal shutdown state if the junction temperature ever reaches

Table 3b. Gamma DAC Voltage/Data Relationship for Selected Codes

SETTING (HEX)	GM1–GM7 OUTPUT VOLTAGE	GM8–GM14 OUTPUT VOLTAGE
000h	GLM + (0 + 1) x ((GLL - GLM)/1024)	GHM + (0 + 1) x ((GHH - GHM)/1024)
001h	GLM + (1 + 1) x ((GLL - GLM)/1024)	GHM + (1 + 1) x ((GHH - GHM)/1024)
002h	GLM + (2 + 1) x ((GLL - GLM)/1024)	GHM + (2 + 1) x ((GHH - GHM)/1024)
003h	GLM + (3 + 1) x ((GLL - GLM)/1024)	GHM + (3 + 1) x ((GHH - GHM)/1024)
00Fh	GLM + (15 + 1) x ((GLL - GLM)/1024)	GHM + (15 + 1) x ((GHH - GHM)/1024)
03Fh	GLM + (63 + 1) x ((GLL - GLM)/1024)	GHM + (63 + 1) x ((GHH - GHM)/1024)
07Fh	GLM + (127 + 1) x ((GLL - GLM)/1024)	GHM + (127 + 1) x ((GHH - GHM)/1024)
0FFh	GLM + (255 + 1) x ((GLL - GLM)/1024)	GHM + (255 + 1) x ((GHH - GHM)/1024)
3FDh	GLM + (1021 + 1) x ((GLL - GLM)/1024)	GHM + (1021 + 1) x ((GHH - GHM)/1024)
3FEh	GLM + (1022 + 1) x ((GLL - GLM)/1024)	GHM + (1022 + 1) x ((GHH - GHM)/1024)
3FFh	GLL	GHH

or exceeds +150°C. In this state, the V_{COM} buffer is disabled (output goes high impedance) until the junction temperature falls below +150°C.

Slave Address Byte and Address Pin

The slave address byte consists of a 7-bit slave address plus a R/$\overline{W}$ bit (see Figure 5). The DS3514's slave address is determined by the state of the A0 pin. This pin allows up to two devices to reside on the same I²C bus. Connecting A0 to GND results in a 0 in the corresponding bit position in the slave address. Conversely, connecting A0 to V_{CC} results in a 1 in the corresponding bit position. For example, the DS3514's slave address byte is C0h when A0 is grounded. I²C communication is described in detail in the *I²C Serial Interface Description* section.

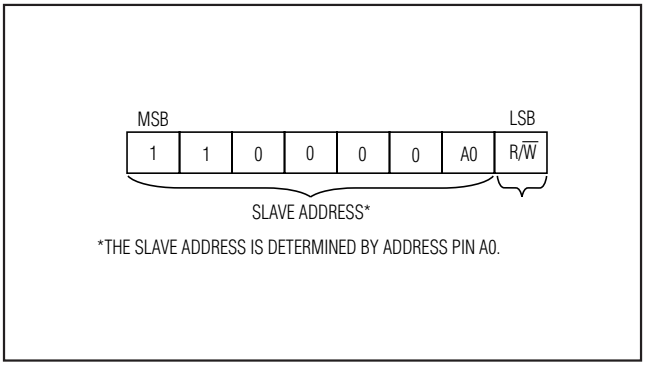


Figure 5. DS3514 Slave Address Byte

Memory Organization

Memory Description

The list of registers/memory contained in the DS3514 is shown in the *Memory Map* section. Also shown for each of the registers is the memory type, accessibility, as well as the power-up default values for volatile locations and factory-programmed defaults for the nonvolatile locations. Additional information regarding reading and writing the memory is located in the *I²C Serial Interface Description* section.

Memory Map

NAME	ADDRESS		DESCRIPTION	TYPE MEMORY OR COMMAND	I²C ACCESS
	(HEX)	(DEC)			
Latch A for V_{COM} Ch	0h	0	8-Bit I²C Data for V_{COM} DAC	Volatile	R/W
Latch A for GM1 Ch	2h, 3h	2, 3	10-Bit I²C Data for GM1 DAC	Volatile	R/W
Latch A for GM2 Ch	4h, 5h	4, 5	10-Bit I²C Data for GM2 DAC	Volatile	R/W
Latch A for GM3 Ch	6h, 7h	6, 7	10-Bit I²C Data for GM3 DAC	Volatile	R/W
Latch A for GM4 Ch	8h, 9h	8, 9	10-Bit I²C Data for GM4 DAC	Volatile	R/W
Latch A for GM5 Ch	Ah, Bh	10, 11	10-Bit I²C Data for GM5 DAC	Volatile	R/W
Latch A for GM6 Ch	Ch, Dh	12, 13	10-Bit I²C Data for GM6 DAC	Volatile	R/W
Latch A for GM7 Ch	Eh, Fh	14, 15	10-Bit I²C Data for GM7 DAC	Volatile	R/W
Latch A for GM8 Ch	10h, 11h	16, 17	10-Bit I²C Data for GM8 DAC	Volatile	R/W
Latch A for GM9 Ch	12h, 13h	18, 19	10-Bit I²C Data for GM9 DAC	Volatile	R/W
Latch A for GM10 Ch	14h, 15h	20, 21	10-Bit I²C Data for GM10 DAC	Volatile	R/W
Latch A for GM11 Ch	16h, 17h	22, 23	10-Bit I²C Data for GM11 DAC	Volatile	R/W
Latch A for GM12 Ch	18h, 19h	24, 25	10-Bit I²C Data for GM12 DAC	Volatile	R/W

I²C Gamma and VCOM Buffer with EEPROM

Memory Map (continued)

NAME	ADDRESS		DESCRIPTION	TYPE MEMORY OR COMMAND	I²C ACCESS
	(HEX)	(DEC)			
Latch A for GM13 Ch	1Ah, 1Bh	26, 27	10-Bit I²C Data for GM13 DAC	Volatile	R/W
Latch A for GM14 Ch	1Ch, 1Dh	28, 29	10-Bit I²C Data for GM14 DAC	Volatile	R/W
Reserved	1Eh–3Fh	30–63	—	—	—
Soft S1/S0	40h	64	Software Bank Select Byte (Bits 1:0)	Volatile	R/W
Standby	41h	65	Shutdown Byte	Volatile	R/W
Reserved	42h–47h	66–71	—	—	—
Control	48h	72	Control Register (see Table 1)	NV	R/W
Reserved	49h	73	—	—	—
Status Bits	4Ah	74	Status Bits	Status	R
Reserved	4Bh–4Fh	75–79	—	—	—
VCOM1–VCOM4	50h, 52h, 54h, 56h	80, 82, 84, 86	V_{COM} EEPROM Data (Four 8-Bit Words)	NV	R/W
GM1 GDAT1–GDAT4	58h–5Fh	88–95	GM1 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM2 GDAT1–GDAT4	60h–67h	96–103	GM2 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM3 GDAT1–GDAT4	68h–6Fh	104–111	GM3 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM4 GDAT1–GDAT4	70h–77h	112–119	GM4 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM5 GDAT1–GDAT4	78h–7Fh	120–127	GM5 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM6 GDAT1–GDAT4	80h–87h	128–135	GM6 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM7 GDAT1–GDAT4	88h–8Fh	136–143	GM7 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM8 GDAT1–GDAT4	90h–97h	144–151	GM8 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM9 GDAT1–GDAT4	98h–9Fh	152–159	GM9 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM10 GDAT1–GDAT4	A0h–A7h	160–167	GM10 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM11 GDAT1–GDAT4	A8h–AFh	168–175	GM11 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM12 GDAT1–GDAT4	B0h–B7h	176–183	GM12 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM13 GDAT1–GDAT4	B8h–BFh	184–191	GM13 EEPROM Data (Four 10-Bit Words)	NV	R/W
GM14 GDAT1–GDAT4	C0h–C7h	192–198	GM14 EEPROM Data (Four 10-Bit Words)	NV	R/W
Reserved	C8h–FFh	200–255	—	—	—

Detailed Register Descriptions

Soft S0/S1 Register 40h: SOFT S1/S0 Bits

FACTORY DEFAULT 00h

MEMORY TYPE Volatile

	BIT 7						SOFT S1	SOFT S0 BIT 0
40h	x	x	x	x	x	x		

Bits 7:2	Reserved
Bits 1:0	These bits are used when in SOFT S0/S1 Bit-Controlled Bank-Updating mode (MODE1 = 0, MODE0 = 1) SOFT S1, SOFT S0: 00 = Selects V_{COM} and GM1–GM14 Bank A 01 = Selects V_{COM} and GM1–GM14 Bank B 10 = Selects V_{COM} and GM1–GM14 Bank C 11 = Selects V_{COM} and GM1–GM14 Bank D

Standby Register 41h: Standby Mode Enable

FACTORY DEFAULT 00h

MEMORY TYPE Volatile

	STANDBY BIT 7							x BIT 0
41h		x	x	x	x	x	x	

Bit 7	STANDBY: 0 = Standby mode disabled 1 = Standby mode enabled
Bits 6:1	Reserved

Control Register 48h: Control Register (CR)

FACTORY DEFAULT 20h

MEMORY TYPE NV

48h	x	x	BIAS1	BIAS0	x	x	MODE1	MODE0
	BIT 7							BIT 0

Bits 7:6	Reserved
Bits 5:4	V_{COM} and Gamma Bias Current Control Bits (BIAS[1:0]): 00 = 60% 01 = 80% 10 = 100% (default) 11 = 150%
Bits 3:2	Reserved
Bits 1:0	DS3514 Mode (MODE[1:0]): 00 = S0/S1 pins are used to select the desired bank (A–D) (default). 01 = SOFT S0/S1 (bits) are used to select the desired bank (A–D). 1X = Latch A is used to control the DACs.

Status Bits Register 4Ah: Real-Time Indicator of Logic State on LD, S1, and S0 Pins

FACTORY DEFAULT —

MEMORY TYPE Read Only

4Ah	LD	x	x	x	x	x	S1	S0
	BIT 7							BIT 0

GDATx Register: EEPROM Data for the Gamma Channels

This is an example of how the bits are arranged for a typical GDATx memory location. GDATx has 10 bits that are arranged in two consecutive bytes. The following example shows the arrangement for GM1 GDAT1 (58h–59h). This arrangement is applicable for all the EEPROM data for all gamma channels.

FACTORY DEFAULT 8000h

MEMORY TYPE NV

58h	GDAT[9]	GDAT[8]	GDAT[7]	GDAT[6]	GDAT[5]	GDAT[4]	GDAT[3]	GDAT[2]
59h	GDAT[1]	GDAT[0]	x	x	x	x	x	x
	BIT 7							BIT 0

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. (See Figure 4 and the *I²C Electrical Characteristics* for additional information.)

Master device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave devices: Slave devices send and receive data at the master's request.

Bus idle or not busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition.

STOP condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

Repeated START condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition.

Bit write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

Bit read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An Acknowledge (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a 0 during the 9th bit. A device performs a NACK by transmitting a 1 during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or indicates that the device is not receiving data.

Byte write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit-write definition and the acknowledgment is read using the bit-read definition.

Byte read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave will return control of SDA to the master.

Slave address byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS3514's slave address is determined by the state of the A0 address pin as shown in Figure 5. An address pin connected to GND results in a 0 in the corresponding bit position in the slave address. Conversely, an address pin connected to V_{CC} results in a 1 in the corresponding bit position.

When the R/$\overline{W}$ bit is 0 (such as in C0h), the master is indicating it will write data to the slave. If R/$\overline{W}$ is set to a 1 (C1h in this case), the master is indicating that it wants to read from the slave.

If an incorrect (nonmatching) slave address is written, the DS3514 assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory address: During an I²C write operation to the DS3514, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Gamma and VCOM Buffer with EEPROM

I²C Communication

Writing a single byte to a slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgment during all byte-write operations.

When writing to the DS3514 (and if LD = 1), the DAC adjusts to the new setting once it has acknowledged the new data that is being written, and the EEPROM (used to make the setting nonvolatile) is written following the STOP condition at the end of the write command.

Writing multiple bytes to a slave: To write multiple bytes to a slave in one transaction, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The DS3514 can write 1 to 8 bytes (one page or row) in a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). The first page begins at address 00h and subsequent pages begin at multiples of 8 (08h, 10h, 18h, etc). Attempts to write to additional pages of memory without sending a STOP condition between pages results in the address counter wrapping around to the beginning of the present row. To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM write time to elapse. Then the master can generate a new START condition and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge polling: Any time a EEPROM byte is written, the DS3514 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the byte to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS3514, which allows communication to continue as soon as the DS3514 is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

EEPROM write cycles: The DS3514's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature (hot) as well as at room temperature.

Reading a single byte from a slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, because requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

Manipulating the address counter for reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. Recall that the master must NACK the last byte to inform the slave that no additional bytes will be read.

See Figure 6 for I²C communication examples.

Reading multiple bytes from a slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and generates a STOP condition.

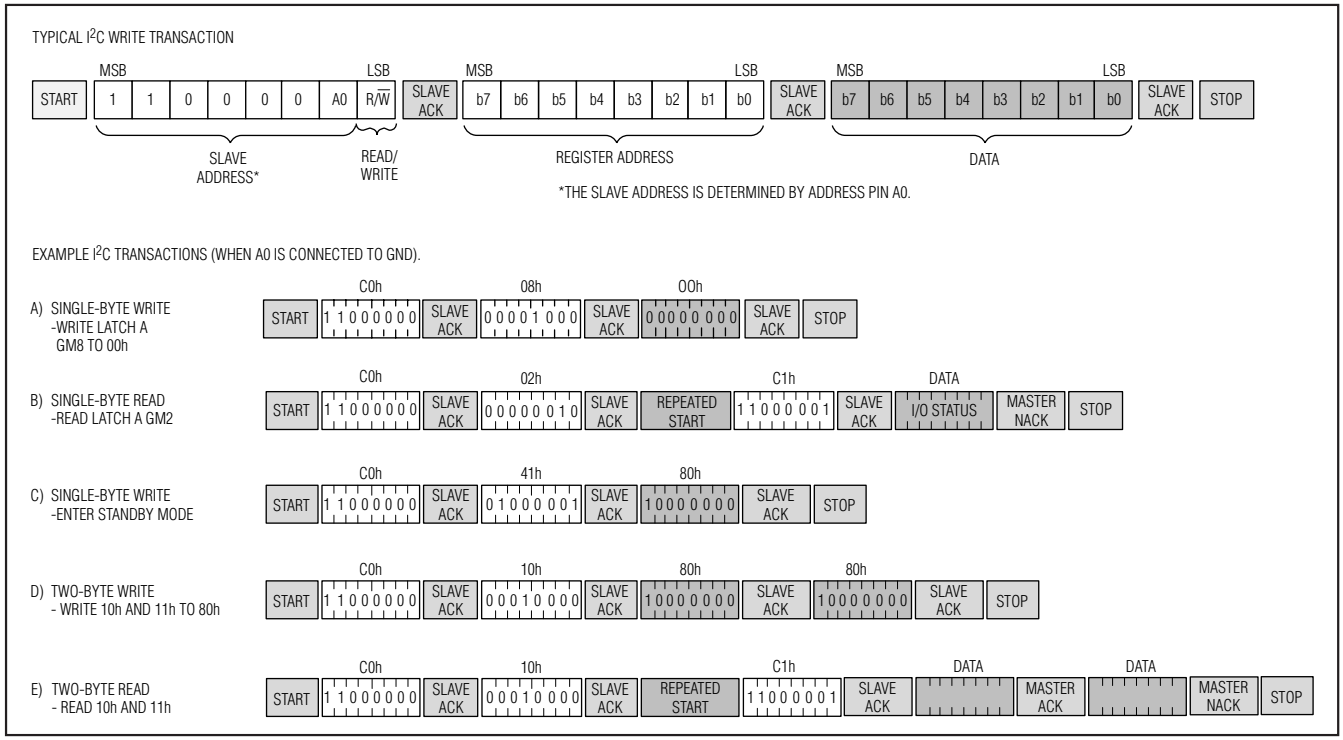


Figure 6. I²C Communication Examples

Applications Information

Power-Supply Decoupling

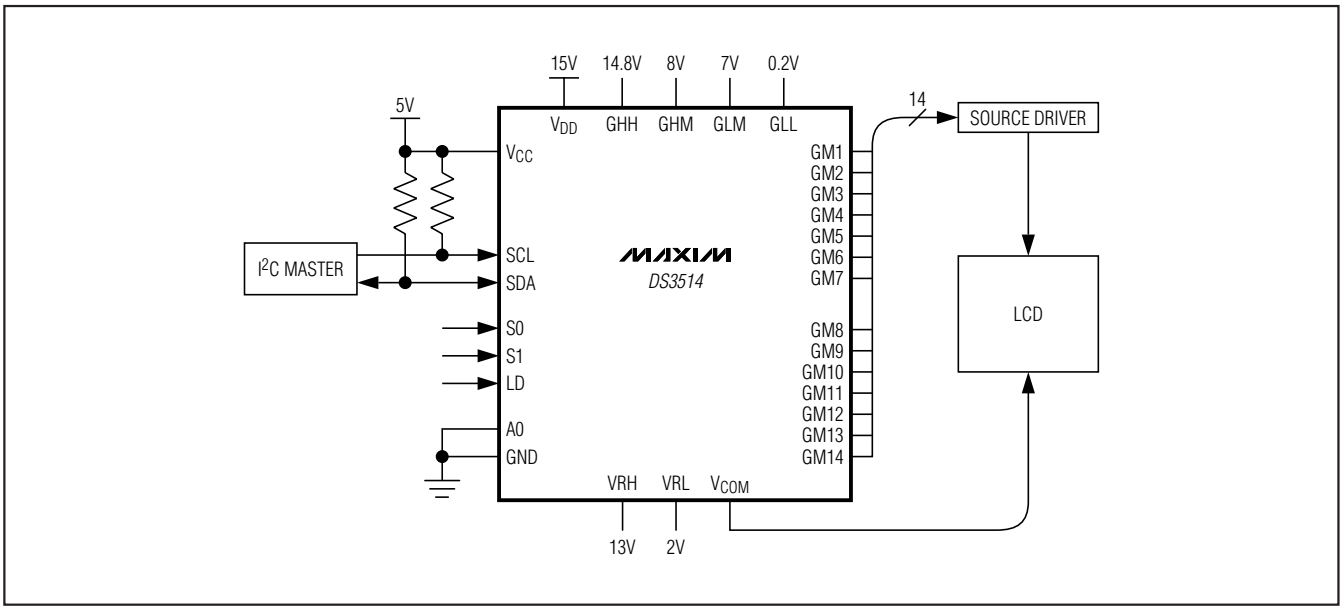
To achieve the best results when using the DS3514, decouple all the power-supply pins (V_{CC} and V_{DD}) with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

SDA and SCL Pullup Resistors

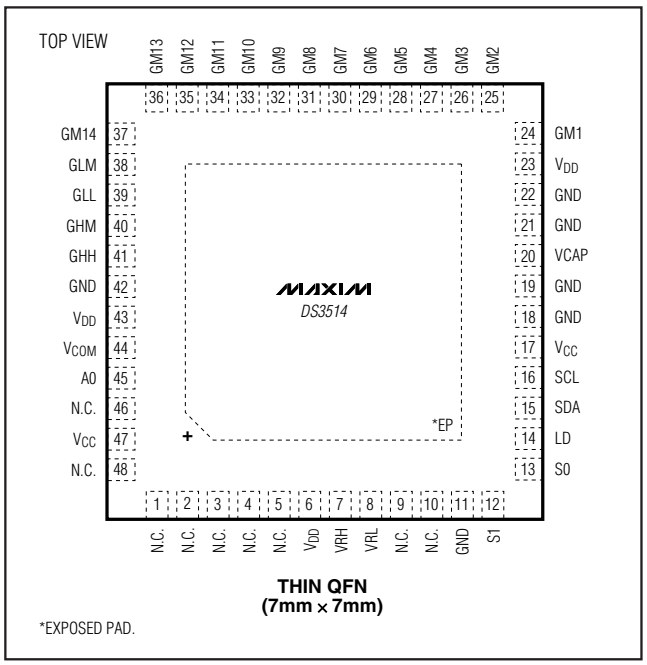
SDA is an I/O with an open-collector output that requires a pullup resistor to realize high-logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I²C Electrical Characteristics* are within specification. A typical value for the pullup resistors is 4.7kΩ.

I²C Gamma and VCOM Buffer with EEPROM

Typical Operating Circuit



Pin Configuration



THIN QFN
(7mm × 7mm)

*EXPOSED PAD.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN-EP	T4877M+6	21-0144

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/08	Initial release.	—
1	10/08	Changed the maximum V_{CC} supply current (I_{CC}) specification from 0.5mA to 0.6mA.	2