

# NE592

## Video Amplifier

The NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

### Features

- 120 MHz Unity Gain Bandwidth
- Adjustable Gains from 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required
- Wave Shaping with Minimal External Components
- MIL-STD Processing Available
- Pb-Free Packages are Available

### Applications

- Floppy Disk Head Amplifier
- Video Amplifier
- Pulse Amplifier in Communications
- Magnetic Memory
- Video Recorder Systems

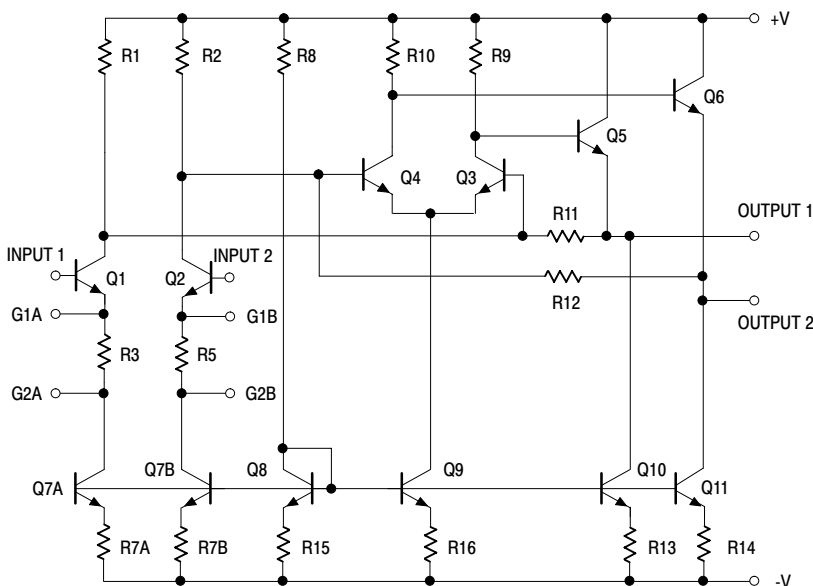


Figure 1. Block Diagram



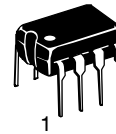
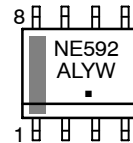
ON Semiconductor®

<http://onsemi.com>

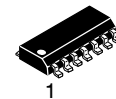
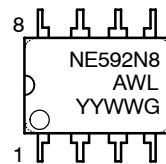
### MARKING DIAGRAMS



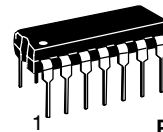
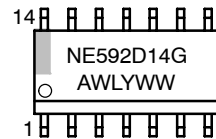
SOIC-8  
D SUFFIX  
CASE 751



PDIP-8  
N SUFFIX  
CASE 626



SOIC-14  
D SUFFIX  
CASE 751A



PDIP-14  
N SUFFIX  
CASE 646



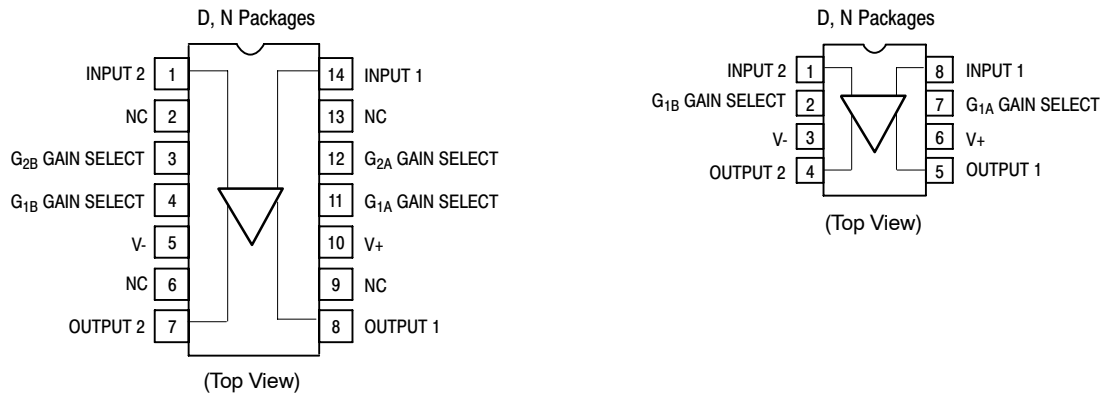
A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
■ or G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

# NE592

## PIN CONNECTIONS



### MAXIMUM RATINGS ( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	$\pm 8.0$	V
Differential Input Voltage	$V_{IN}$	$\pm 5.0$	V
Common-Mode Input Voltage	$V_{CM}$	$\pm 6.0$	V
Output Current	$I_{OUT}$	10	mA
Operating Ambient Temperature Range	$T_A$	0 to +70	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	65 to +150	$^\circ\text{C}$
Maximum Power Dissipation, $T_A = 25^\circ\text{C}$ (Still Air) (Note 1)	$P_{D\ MAX}$	D-14 Package D-8 Package N-14 Package N-8 Package	0.98 0.79 1.44J1.17 W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	D-14 Package D-8 Package N-14 Package N-8 Package	145 182 100 130 $^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Derate above  $25^\circ\text{C}$  at the following rates:  
 D-14 package at  $6.9\ \text{mW}/^\circ\text{C}$   
 D-8 package at  $5.5\ \text{mW}/^\circ\text{C}$   
 N-14 package at  $10\ \text{mW}/^\circ\text{C}$   
 N-8 package at  $7.7\ \text{mW}/^\circ\text{C}$ .

# NE592

**DC ELECTRICAL CHARACTERISTICS** ( $V_{SS} = \pm 6.0$  V,  $V_{CM} = 0$ , typicals at  $T_A = +25^\circ\text{C}$ , min and max at  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ , unless otherwise noted. Recommended operating supply voltages  $V_S = \pm 6.0$  V.)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain Gain 1 (Note 2) Gain 2 (Notes 3 and 4)	$R_L = 2.0$ k $\Omega$ , $V_{OUT} = 3.0$ V <sub>P-P</sub>	$A_{VOL}$	250 80	400 100	600 120	V/V
Input Resistance Gain 1 (Note 2) Gain 2 (Notes 3 and 4)	– $T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	$R_{IN}$	– 10 8.0	4.0 30 –	– – –	k $\Omega$
Input Capacitance	Gain 2 (Note 4)	$C_{IN}$	–	2.0	–	pF
Input Offset Current	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	$I_{OS}$	– –	0.4 –	5.0 6.0	$\mu\text{A}$
Input Bias Current	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	$I_{BIAS}$	– –	9.0 –	30 40	$\mu\text{A}$
Input Noise Voltage	BW 1.0 kHz to 10 MHz	$V_{NOISE}$	–	12	–	$\mu\text{V}_{RMS}$
Input Voltage Range	–	$V_{IN}$	$\pm 1.0$	–	–	V
Common-Mode Rejection Ratio Gain 2 (Note 4)	$V_{CM} \pm 1.0$ V, $f < 100$ kHz, $T_A = 25^\circ\text{C}$ $V_{CM} \pm 1.0$ V, $f < 100$ kHz, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $V_{CM} \pm 1.0$ V, $f < 5.0$ MHz	CMRR	60 50 –	86 – 60	– – –	dB
Supply Voltage Rejection Ratio Gain 2 (Note 4)	$\Delta V_S = \pm 0.5$ V	PSRR	50	70	–	dB
Output Offset Voltage Gain 1 Gain 2 (Note 4) Gain 3 (Note 5) Gain 3 (Note 5)	$R_L = \infty$ $R_L = \infty$ $R_L = \infty$ , $T_A = 25^\circ\text{C}$ $R_L = \infty$ , $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	$V_{OS}$	– – – –	– – 0.35 –	1.5 1.5 0.75 1.0	V
Output Common-Mode Voltage	$R_L = \infty$ , $T_A = 25^\circ\text{C}$	$V_{CM}$	2.4	2.9	3.4	V
Output Voltage Swing Differential	$R_L = 2.0$ k $\Omega$ , $T_A = 25^\circ\text{C}$ $R_L = 2.0$ k $\Omega$ , $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	$V_{OUT}$	3.0 2.8	4.0 –	– –	V
Output Resistance	–	$R_{OUT}$	–	20	–	$\Omega$
Power Supply Current	$R_L = \infty$ , $T_A = 25^\circ\text{C}$ $R_L = \infty$ , $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	$I_{CC}$	– –	18 –	24 27	mA

**AC ELECTRICAL CHARACTERISTICS** ( $T_A = +25^\circ\text{C}$ ,  $V_{SS} = \pm 6.0$  V,  $V_{CM} = 0$ , unless otherwise noted. Recommended operating supply voltages  $V_S = \pm 6.0$  V.)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
Bandwidth Gain 1 (Note 2) Gain 2 (Notes 3 and 4)	–	BW	– –	40 90	– –	MHz
Rise Time Gain 1 (Note 2) Gain 2 (Notes 3 and 4)	$V_{OUT} = 1.0$ V <sub>P-P</sub>	$t_R$	– –	10.5 4.5	12 –	ns
Propagation Delay Gain 1 (Note 2) Gain 2 (Notes 3 and 4)	$V_{OUT} = 1.0$ V <sub>P-P</sub>	$t_{PD}$	– –	7.5 6.0	10 –	ns

- Gain select Pins  $G_{1A}$  and  $G_{1B}$  connected together.
- Gain select Pins  $G_{2A}$  and  $G_{2B}$  connected together.
- Applies to 14-pin version only.
- All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

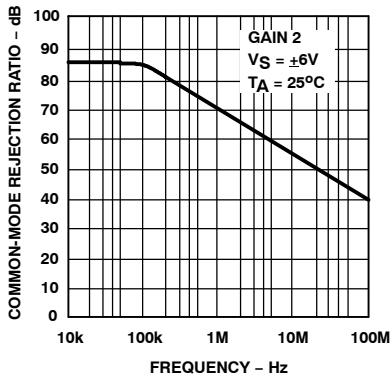


Figure 2. Common-Mode Rejection Ratio as a Function of Frequency

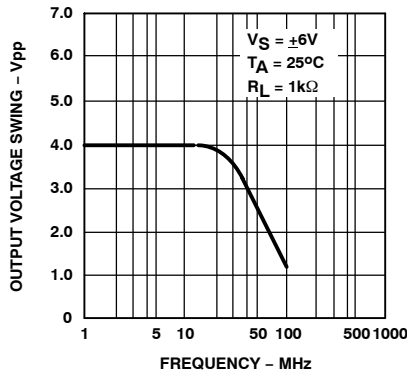


Figure 3. Output Voltage Swing as a Function of Frequency

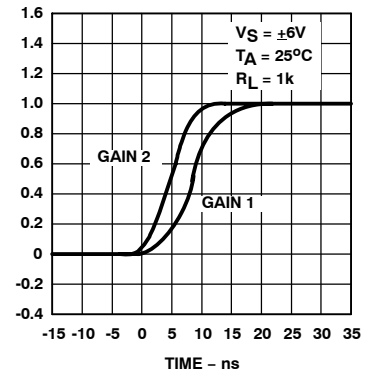


Figure 4. Pulse Response

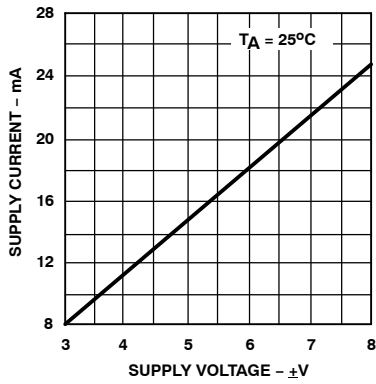


Figure 5. Supply Current as a Function of Temperature

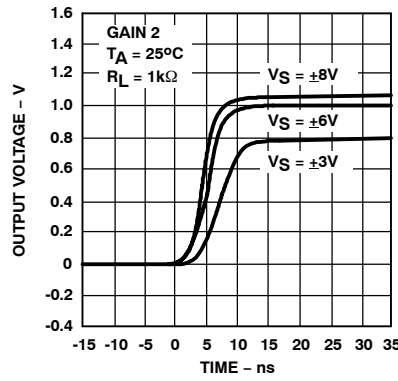


Figure 6. Pulse Response as a Function of Supply Voltage

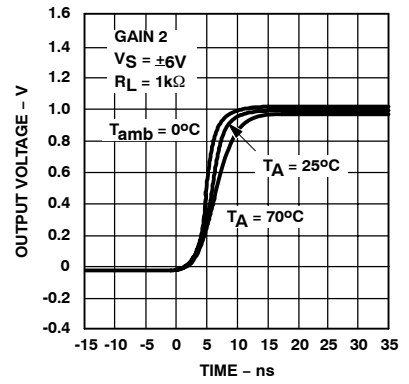


Figure 7. Pulse Response as a Function of Temperature

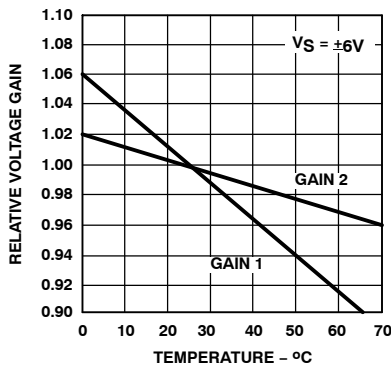


Figure 8. Voltage Gain as a Function of Temperature

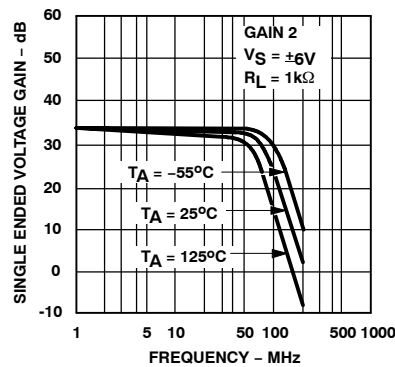


Figure 9. Gain vs. Frequency as a Function of Temperature

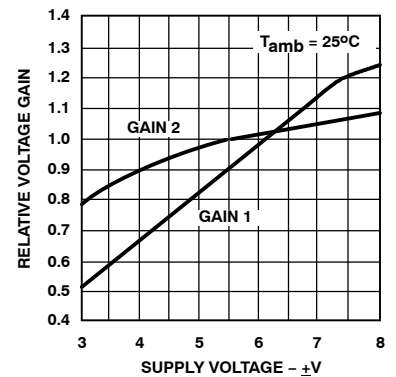


Figure 10. Voltage Gain as a Function of Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

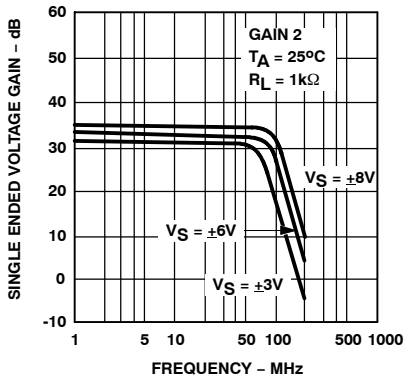


Figure 11. Gain vs. Frequency as a Function of Supply Voltage

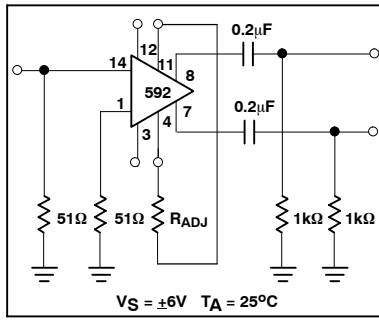


Figure 12. Voltage Gain Adjust Circuit

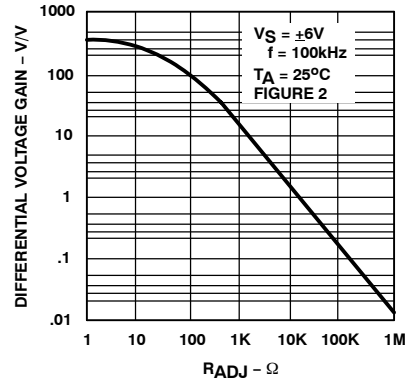


Figure 13. Voltage Gain as a Function of RADJ (Figure 2)

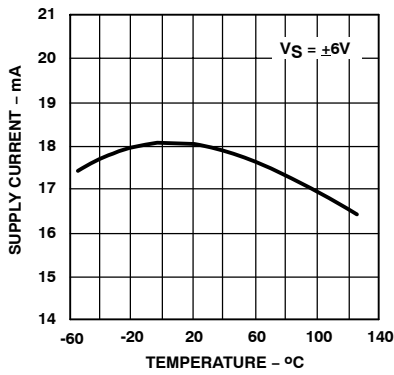


Figure 14. Supply Current as a Function of Temperature

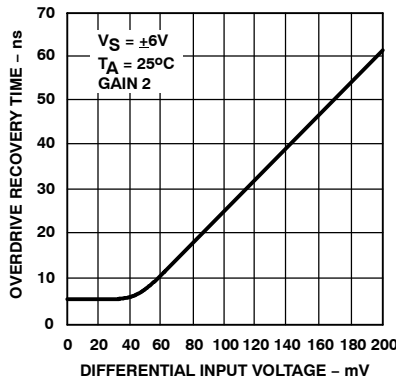


Figure 15. Differential Overdrive Recovery Time

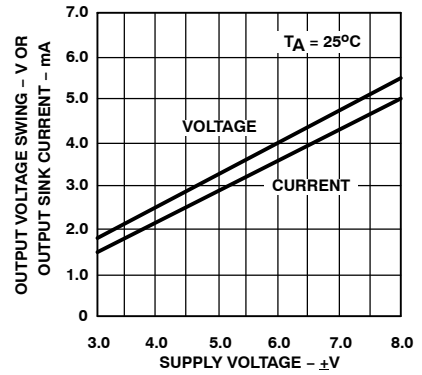


Figure 16. Output Voltage and Current Swing as a Function of Supply Voltage

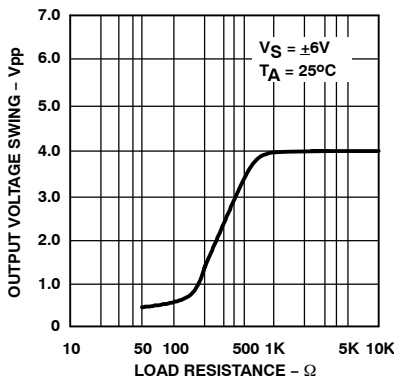


Figure 17. Output Voltage Swing as a Function of Load Resistance

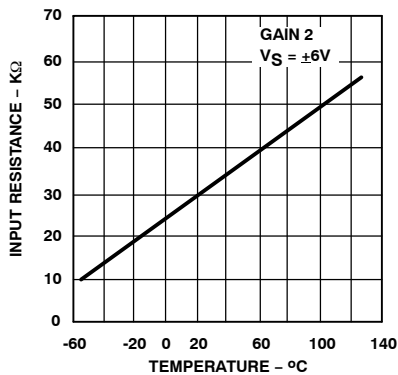


Figure 18. Input Resistance as a Function of Temperature

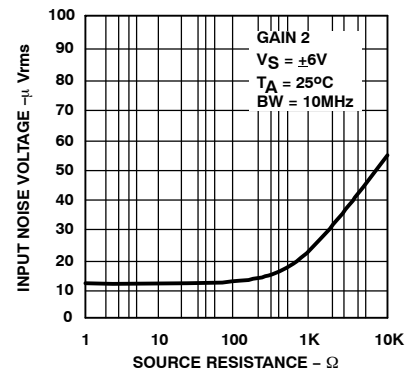


Figure 19. Input Noise Voltage as a Function of Source Resistance

TYPICAL PERFORMANCE CHARACTERISTICS

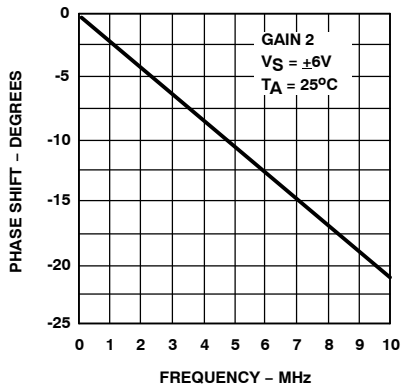


Figure 20. Phase Shift as a Function of Frequency

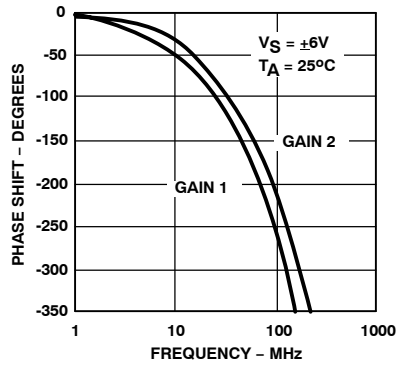


Figure 21. Phase Shift as a Function of Frequency

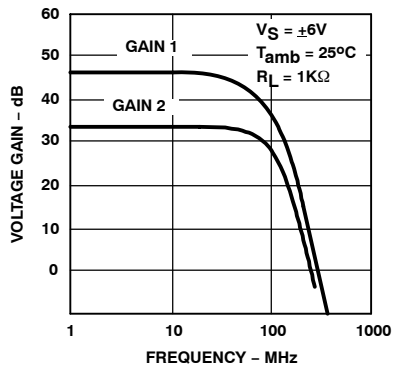


Figure 22. Voltage Gain as a Function of Frequency

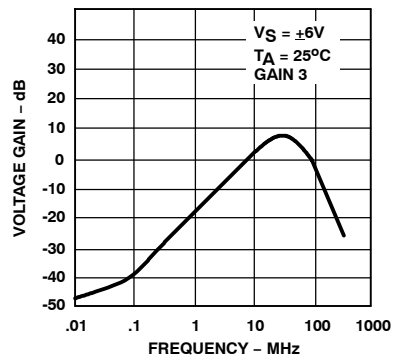


Figure 23. Voltage Gain as a Function of Frequency

TEST CIRCUITS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

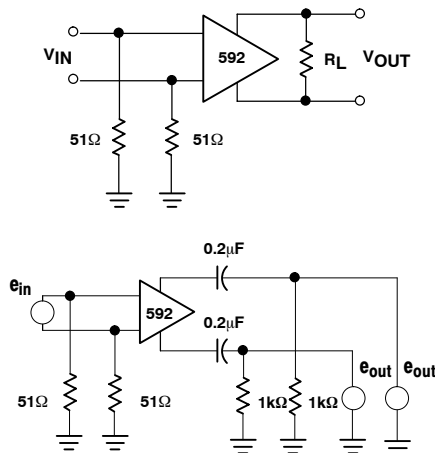


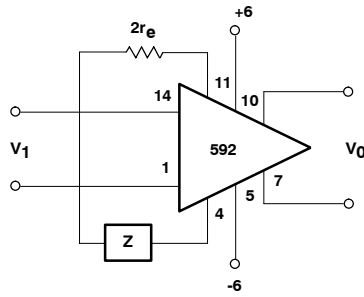
Figure 24. Test Circuits

# NE592

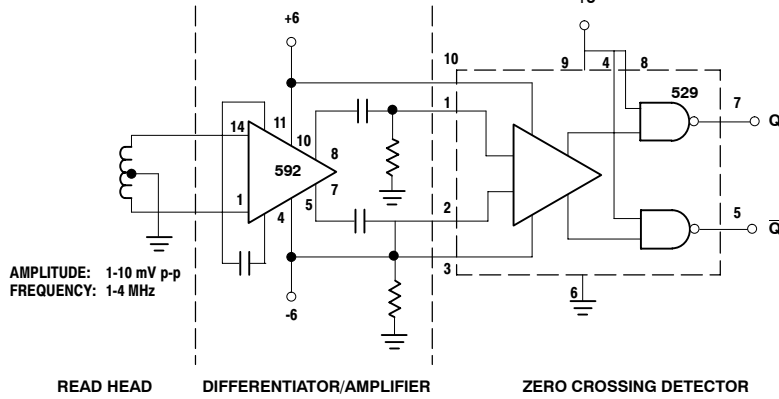
NOTE:

$$\frac{V_0(s)}{v_1(s)} \approx \frac{1.4 \cdot 10^4}{Z(s) + 2r_e}$$

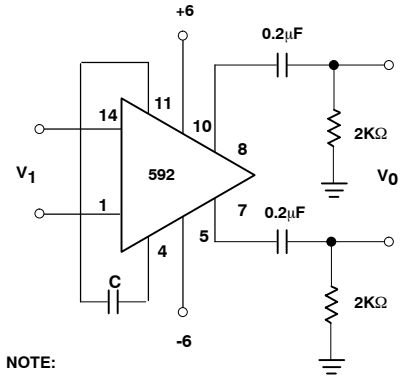
$$\approx \frac{1.4 \cdot 10^4}{Z(s) + 32}$$



Basic Configuration



Disc/Tape Phase-Modulated Readback Systems



NOTE:

For frequency  $F_1 \ll 1/2 \pi (32) C$

$$V_0 \approx 1.4 \times 10^4 C \frac{dV_1}{dt}$$

Differentiation with High Common-Mode Noise Rejection

Figure 25. Typical Applications

Z NETWORK	FILTER TYPE	$V_0(s)$ TRANSFER $V_1(s)$ FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L} \left[ \frac{1}{s + R/L} \right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R} \left[ \frac{s}{s + 1/RC} \right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L} \left[ \frac{s}{s^2 + R/Ls + 1/LC} \right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R} \left[ \frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC} \right]$

NOTES:

In the networks above, the R value used is assumed to include  $2r_e$ , or approximately  $32\Omega$ .

$S = j\Omega$

$\Omega = 2\pi f$

Figure 26. Filter Networks

# NE592

## ORDERING INFORMATION

Device	Temperature Range	Package	Shipping†
NE592D8	0 to +70°C	SOIC-8	98 Units/Rail
NE592D8G		SOIC-8 (Pb-Free)	
NE592D8R2		SOIC-8	2500 / Tape & Reel
NE592D8R2G		SOIC-8 (Pb-Free)	
NE592N8		PDIP-8	50 Units/Rail
NE592N8G		PDIP-8 (Pb-Free)	
NE592D14		SOIC-14	55 Units/Rail
NE592D14G		SOIC-14 (Pb-Free)	
NE592D14R2		SOIC-14	2500 / Tape & Reel
NE592D14R2G		SOIC-14 (Pb-Free)	
NE592N14		PDIP-14	25 Units/Rail
NE592N14G		PDIP-14 (Pb-Free)	

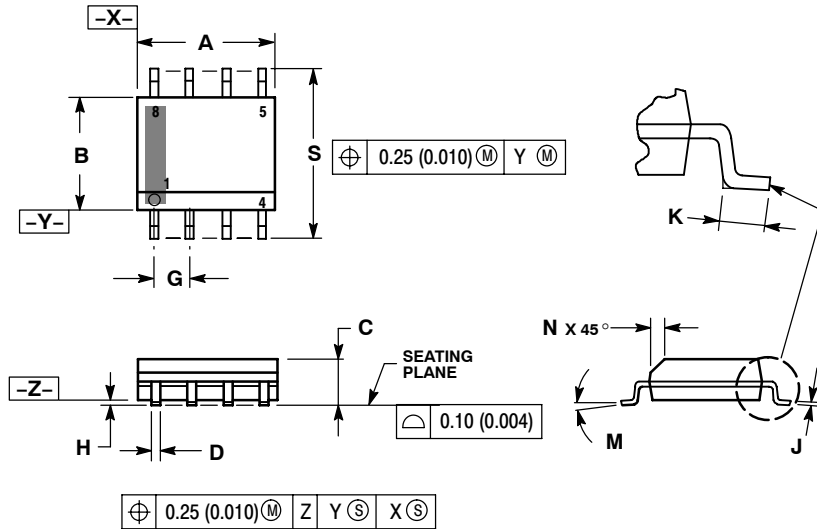
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



# NE592

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AH

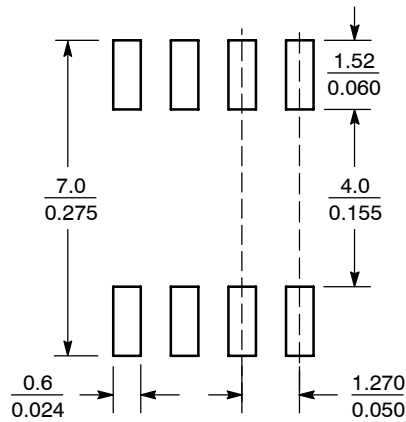


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



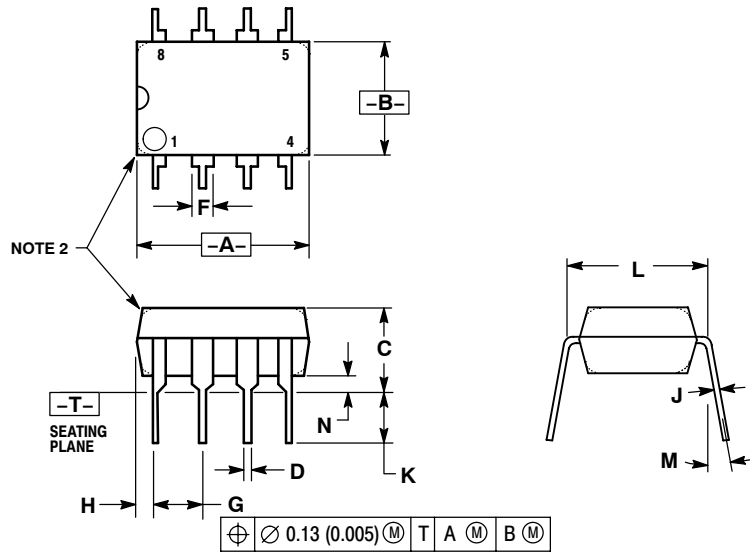
SCALE 6:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NE592

## PACKAGE DIMENSIONS

PDIP-8  
N SUFFIX  
CASE 626-05  
ISSUE L



NOTES:

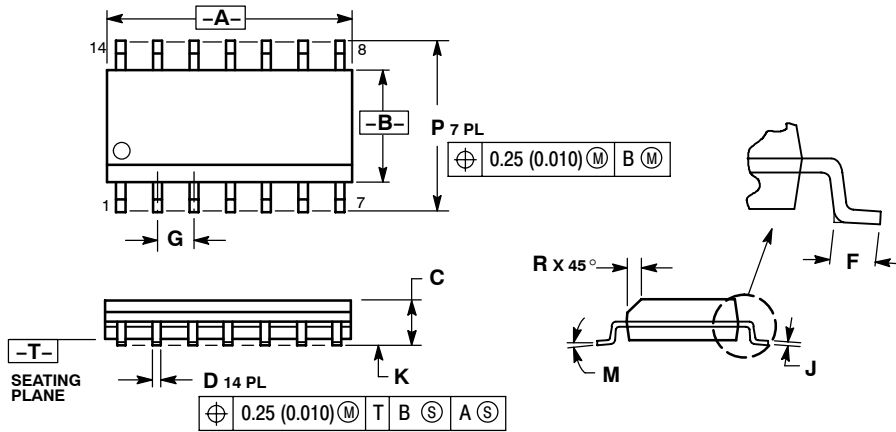
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

# NE592

## PACKAGE DIMENSIONS

SOIC-14  
CASE 751A-03  
ISSUE H

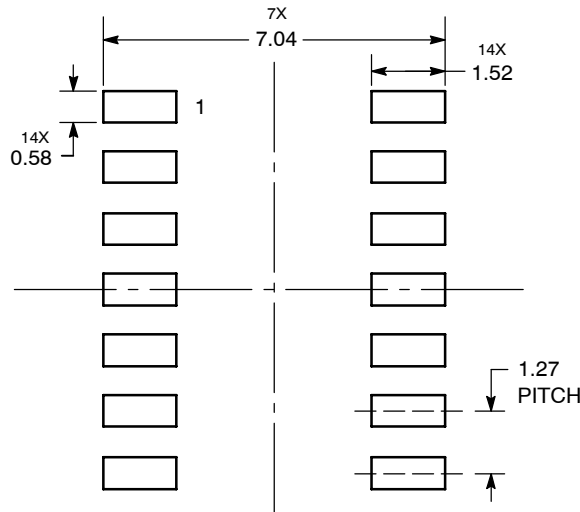


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

**SOLDERING FOOTPRINT\***



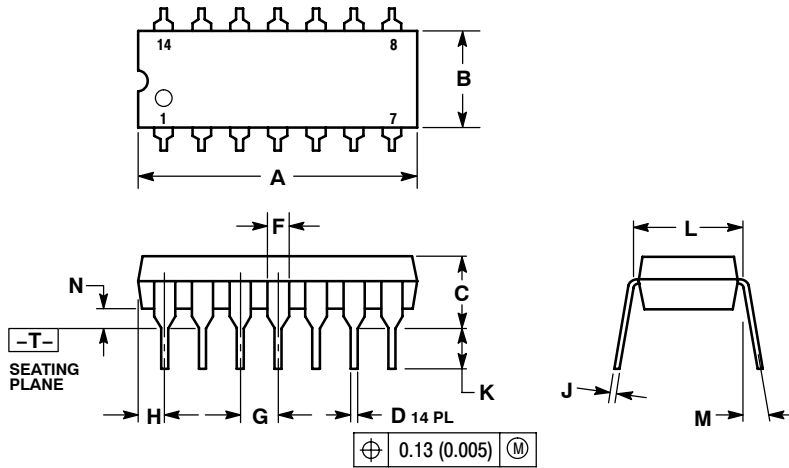
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NE592

## PACKAGE DIMENSIONS

**PDIP-14**  
CASE 646-06  
ISSUE P



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

**NE592/D**