Differential Video Amplifier with Common Mode Sync Encoder and Serial Digital Interface

The ISL59311 is a high bandwidth triple differential amplifier with integrated encoding of video sync signals. The inputs are suitable for handling high speed video or other communications signals in either single-ended or differential form, and the common-mode input range extends all the way to the negative rail enabling ground-referenced signaling in single supply applications. The high bandwidth enables differential signaling onto standard twisted-pair or coax with very low harmonic distortion, while internal feedback ensures balanced gain and phase at the outputs reducing radiated EMI and harmonics.

Embedded logic encodes standard video horizontal and vertical sync signals onto the common mode of the twisted pair(s), transmitting this additional information without the requirement for additional buffers or transmission lines. The ISL59311 enables significant system cost savings when compared with discrete line driver alternatives.

The digital block of the chip is a data transceiver which is intended to drive one twisted pair line. The maximum baudrate for this block is 50Mbps.

The ISL59311 is available in a 32 Ld QFN package and is specified for operation over the -40°C to +85°C temperature range.

Applications

- Twisted-pair drivers
- Differential line drivers
- VGA over twisted-pair
- Transmission of analog signals in a noisy environment

Ordering Information

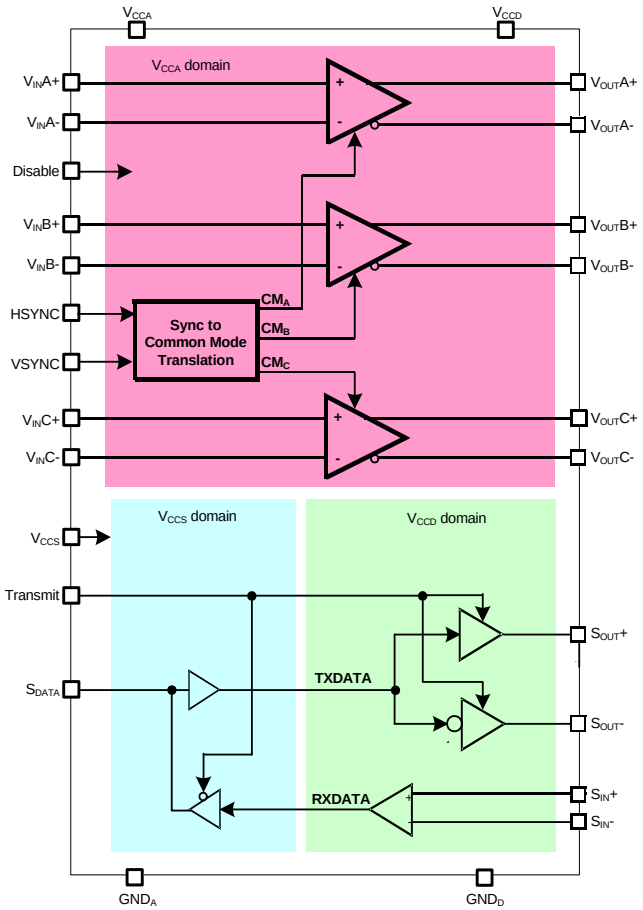
PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL59311IRZ	59311 IRZ	-	32 Ld QFN	L32.5x6A
ISL59311IRZ-T13	59311 IRZ	13”	32 Ld QFN	L32.5x6A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

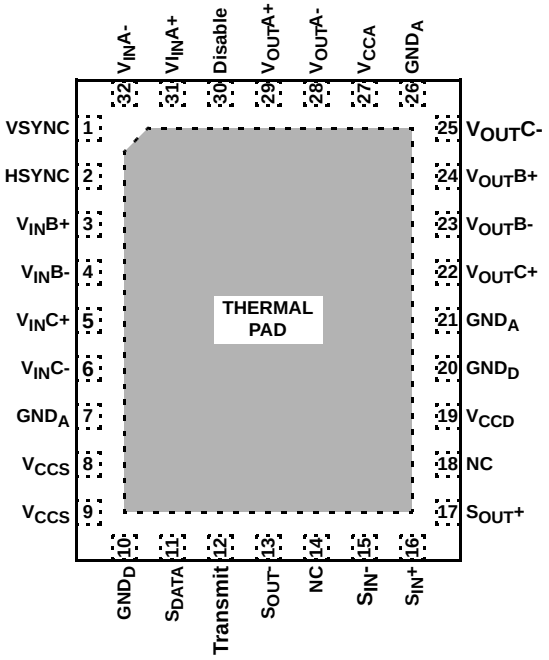
- Fully differential inputs, outputs, and feedback
- 650MHz -3dB bandwidth
- 1500V/µs slew rate
- -70dB distortion at 20MHz
- Single 5V operation
- 50mA minimum output current
- Low power: 57mA total supply current
- Pb-free plus anneal available (RoHS compliant)

Block Diagram

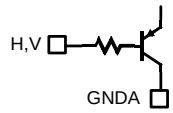
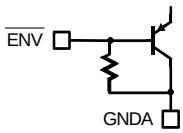
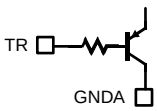


Pinout

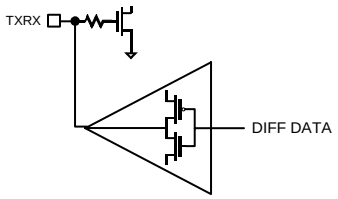
ISL59311
(32 LD QFN)



Pin Descriptions

PIN NAME	DESCRIPTIONS	EQUIVALENT CIRCUIT
$V_{IN}A\pm$, $V_{IN}B\pm$, $V_{IN}C\pm$	Differential video inputs	
$V_{OUT}A\pm$, $V_{OUT}B\pm$, $V_{OUT}C\pm$	Differential video outputs to transmission line	
HSYNC, VSYNC	Horizontal and Vertical Sync inputs to be encoded	
Disable	Disable video amplifiers signal. Logic low enables the video amplifiers. Logic high disables the video amplifiers, reducing V_{CCA} power consumption. The Serial Digital Interface is always enabled regardless of the state of the Disable pin.	
Transmit	Transmit/$\overline{\text{receive}}$ logic input. Logic high: Transmits data from the S_{DATA} pin data down the transmission line. Logic low: Data received from the transmission line is output on the S_{DATA} pin.	
$S_{OUT}\pm$	Differential serial data outputs to transmission line	
$S_{IN}\pm$	Differential serial data inputs from transmission line	

Pin Descriptions (Continued)

PIN NAME	DESCRIPTIONS	EQUIVALENT CIRCUIT
S_{DATA}	Digital data input/output. When Transmit is high, this is an input, receiving the serial data to be transmitted over the $S_{OUT}\pm$ pins. When Transmit is low, this is an output, representing the data received on the $S_{IN}\pm$ pins.	
V_{CCS}	Power supply for S_{DATA} I/O pin - sets input thresholds and output swing. Typically set to 3.3V or 5V.	
V_{CCD}	V_{CC} for line interface section (5V)	
GND_D	Digital ground for the Serial Digital Interface	
V_{CCA}	V_{CC} for the video amplifiers (5V)	
GND_A	Analog ground for the video amplifiers	
NC	No Connection. **Do not connect these pins to anything. Leave these pins floating!**	

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_{CCA}, V_{CCD}) . . . . . +6.5V
Maximum Output Continuous Current . . . . . ±70mA
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +125°C
Ambient Operating Temperature . . . . . -40°C to +85°C

Input/Output Voltages
All signal (non-supply) pins . . . . . -0.6V to V_{CCA} + 0.6V
ESD Classification
Human Body Model 3000V
Machine Model 250V
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

$V_{CCA} = V_{CCD} = V_{CCS}$ = +5V, $GND_A = GND_D$ = 0V, T_A = +25°C, V_{IN} = 0V, R_L = 200Ω, unless otherwise specified.

DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
Video Amplifier Electrical Characteristics					
Output Voltage Range		1		V_{CC} - 1	V
Output Impedance, Disabled			10		MΩ
AC PERFORMANCE					
Bandwidth, -3dB	A_V = 2, V_{OUT} = 200mV		650		MHz
	V_{OUT} = 2V		600		MHz
Differential Slew Rate,	$V_{OUT} = 2V_{P-P}$		1500		V/µs
Settling Time (0.1%, $2V_{P-P}$)			20		ns
Gain Bandwidth Product			1300		MHz
2nd Harmonic Distortion	20MHz, R_L = 200Ω		-70		dBc
3rd Harmonic Distortion	20MHz, R_L = 200Ω		-70		dBc
Hostile Crosstalk			75		dB
Differential Phase @100MHz			0.01		°
Differential Gain @100MHz			0.01		%
INPUT CHARACTERISTICS					
Input Referred Offset Voltage		-10	±1	10	mV
Input Bias Current		2	6	12	µA
Differential Input Impedance			10		MΩ
Differential Input Range			±0.75		V
Common Mode Input Voltage Range		-0.3		V_{CCA} - 2.6	V
Input Referred Noise			15		nV/√Hz
CMRR	V_{CM} = 0V to 2V	60	75		dB
OUTPUT CHARACTERISTICS					
Output Peak Current		±40	±60		mA
Output Voltage Range		1		V_{CC} - 1	V
DC PERFORMANCE					
Voltage Gain		1.90	1.95	2.00	V/V

Electrical Specifications $V_{CCA} = V_{CCD} = V_{CCS} = +5V$, $GND_A = GND_D = 0V$, $T_A = +25°C$, $V_{IN} = 0V$, $R_L = 200\Omega$, unless otherwise specified. **(Continued)**

DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
PSRR	Rejection of V_{CCA}	60	75		dB
Digital Transceiver Block Electrical Characteristics					
TRANSMITTER DC CHARACTERSTICS					
$S_{OUT}\pm$ Differential Output Voltage	No load		V_{CCD}		V
	$R_L = 100\Omega$ (Figure 1A)	3.0	3.3		V
Change in Magnitude of Driver Differential $S_{OUT}\pm$ for Complementary Output States	$R_L = 100\Omega$ (Figure 1A) $\lvert(S_{OUT}+) - (S_{OUT}-)\rvert$		.08	0.2	V
$S_{OUT}\pm$ Common-Mode Voltage (deviation from $V_{CCD}/2$)	$R_L = 100\Omega$ (Figure 1A)	-0.1	±0.06	+0.1	V
$S_{OUT}\pm$ Short Circuit Current	Driving high, output tied to GND		95	110	mA
	Driving low, output tied to V_{CCD}		95	110	mA
$S_{OUT}\pm$ Leakage Current	S_{OUT} (Transmit = GND)		±2	±100	nA
TRANSMITTER SWITCHING CHARACTERISTICS					
Maximum Data Rate	$R_L = 100\Omega$, (Figure 1A)	50			Mbps
Differential Propagation Delay	t_{PLH} (Figure 2, $R_{DIFF} = 100\Omega$)		6	10	ns
	t_{PHL} (Figure 2, $R_{DIFF} = 100\Omega$)		6	10	ns
Differential Output Skew	$\lvert t_{PLH} - t_{PHL}\rvert$ (Figure 2, $R_{DIFF} = 100\Omega$)		2	4	ns
Output Enable Time	t_{PZH}: Driver Enable to Output High (Figure 3, I_{SINK} = 1mA, I_{SOURCE} = off)		4	20	ns
	t_{PZL}: Driver Enable to Output Low (Figure 3, I_{SINK} = off, I_{SOURCE} = 1mA)		6	20	ns
Output Disable Time	t_{PHZ}: Output High to Output Disabled (Figure 3, I_{SINK} = 25mA, I_{SOURCE} = off)		28	35	ns
	t_{PLZ}: Output Low to Output Disabled (Figure 3, I_{SINK} = off, I_{SOURCE} = 25mA)		28	35	ns
Disabled Output Leakage			±2	±100	nA
RECEIVER DC CHARACTERISTICS					
$S_{IN}\pm$ Input Hysteresis	V_{CM} = 2.5V	2	30	50	mV
$S_{IN}\pm$ Input Range		GND - 0.5		V_{CC} + 0.5	V
$S_{IN}\pm$ Input Resistance; Each Input to GND		2.5	3.0	3.5	kΩ
RECEIVER SWITCHING CHARACTERISTICS					
Maximum Data Rate	Driven with 100mV differential signal (Figure 4, Note 4)	50			Mbps
Receiver Input to Output Propagation Delay	T_{PLH} (Figure 4)		4.7	8	ns
	T_{PHL} (Figure 4)		5.5	8	ns
Receiver Skew	$\lvert t_{PLH} - t_{PHL}\rvert$ (Figure 4)		0.8	2	ns
t_{RISE}/t_{FALL}	100kΩ II10pF load		2		ns
Receiver Enable to Output High			15	20	ns
Receiver Enable to Output Low			35	42	ns
Receiver High to Hi-Z			15	25	ns

Electrical Specifications $V_{CCA} = V_{CCD} = V_{CCS} = +5V$, $GND_A = GND_D = 0V$, $T_A = +25°C$, $V_{IN} = 0V$, $R_L = 200\Omega$, unless otherwise specified. **(Continued)**

DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
Receiver Low to Hi-Z			10	20	ns
System Logic Inputs DC Characteristics					
VSYNC, HSYNC, TRANSMIT, AND DISABLE INPUT CHARACTERISTICS					
Input High Voltage	V_{IH}	2			V
Input Low Voltage	V_{IL}			0.8	V
VSYNC, HSYNC, Transmit Input Current	I_{IN}		±1	±5	µA
Disable Pin Pull-down Resistance to GNDA	$R_{Disable}$		500		kΩ
S_{DATA} INPUT CHARACTERISTICS (Transmit = V_{CCD})					
Input High Voltage	V_{IH}	0.7 V_{CCS}			V
Input Low Voltage	V_{IL}			0.3 V_{CCS}	V
Input Current	I_{IN}		±0.001	±1	µA
S_{DATA} OUTPUT CHARACTERISTICS (Transmit = GND)					
High Output Level	Sourcing 4mA to GND	4.5	4.7		V
Low Output Level	Sinking 4mA from V_{CCS}		0.3	0.4	V
Short Circuit Output Current	Driving high, output tied to GND		20		mA
	Driving low, output tied to V_{CCS}		40		mA
Power Supply Characteristics					
V_{CCA} Operating Range		4.5		5.5	V
V_{CCA} Supply Current **(all 3 channels)**	Operating (Disable = GND)		50	60	mA
	Disabled (Disable = V_{CCA})		2.3	3	mA
V_{CCD} Operating Range		4.5		5.5	V
V_{CCD} Supply Current			7	12	mA
V_{CCS} Input Impedance	V_{CCS} = 5V (Note 2)	4	5	6	kΩ

NOTES:

1. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
2. V_{CCS} current is equal to the V_{CCS} voltage applied divided by the V_{CCS} Input Impedance. Some additional current is consumed when S_{DATA} is driving high into the external load.
3. Applies to peak current. See “Typical Performance Curves” for more information.
4. Guaranteed by characterization but not tested.

Test Circuits and Waveforms

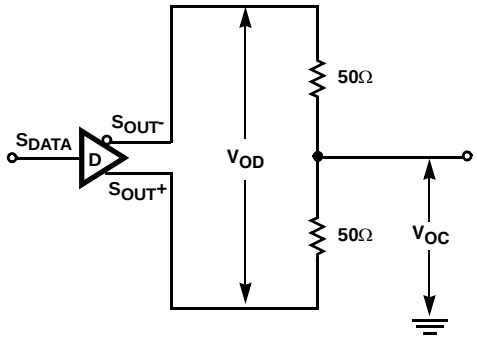


FIGURE 1A. V_{OD} AND V_{OC}

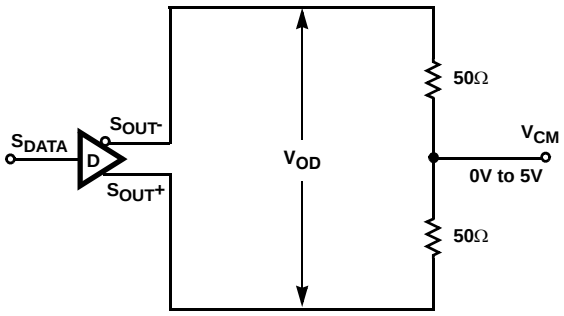


FIGURE 1B. V_{OD} WITH COMMON MODE LOAD

FIGURE 1. DC DRIVER TEST CIRCUITS

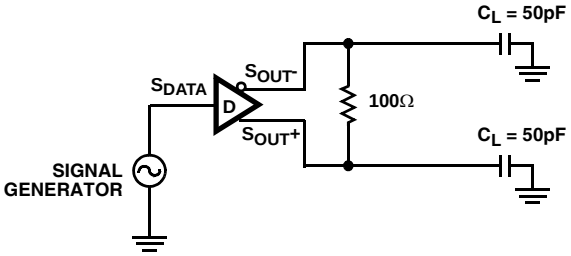


FIGURE 2A. TEST CIRCUIT

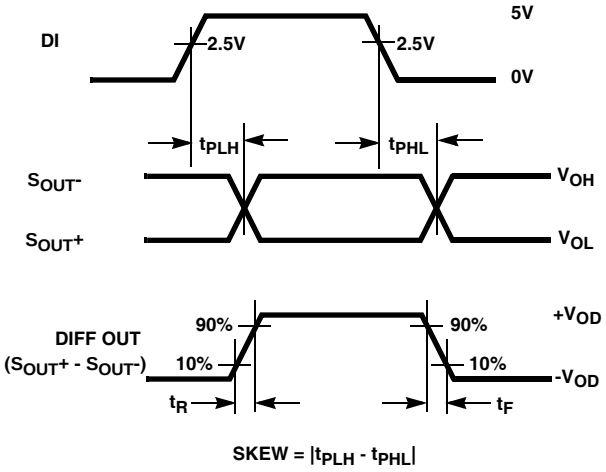


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES

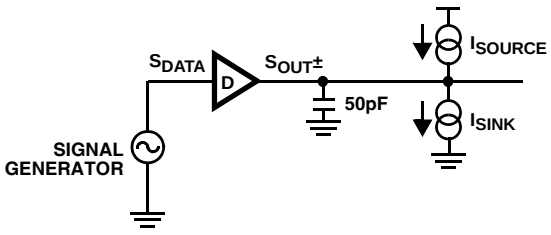


FIGURE 3A. TEST CIRCUIT

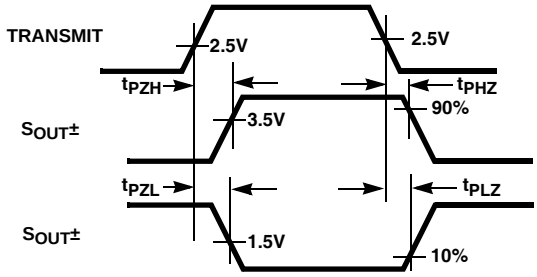


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER DATA RATE

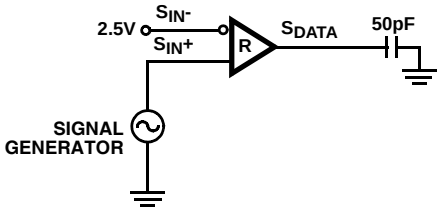


FIGURE 4A. TEST CIRCUIT

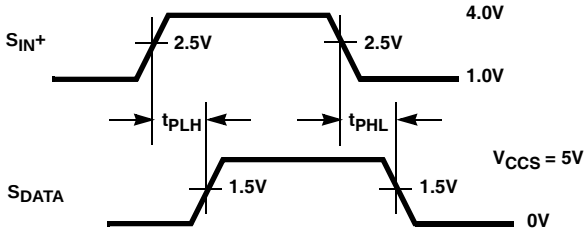


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. RECEIVER PROPAGATION DELAY AND DATA RATE

Typical Performance Curves

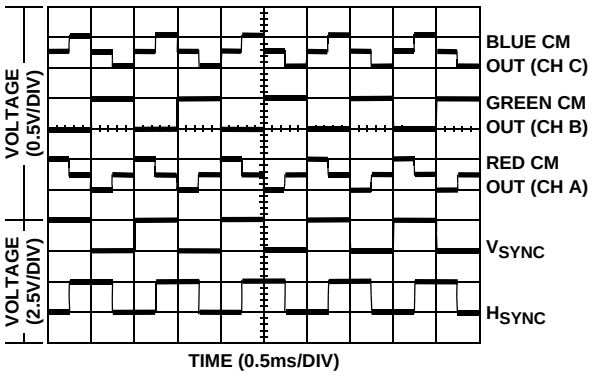


FIGURE 5. COMMON MODE OUTPUT

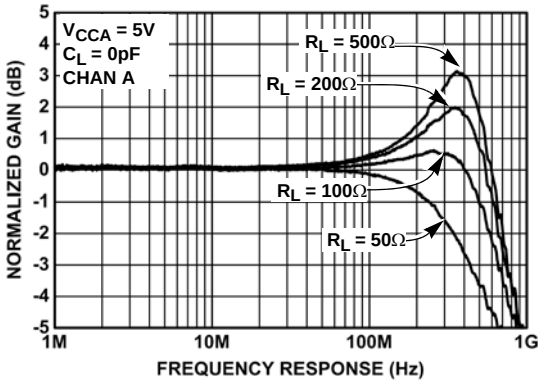


FIGURE 6. DIFFERENTIAL FREQUENCY RESPONSE FOR VARIOUS R_L - DIFF (CHANNEL A)

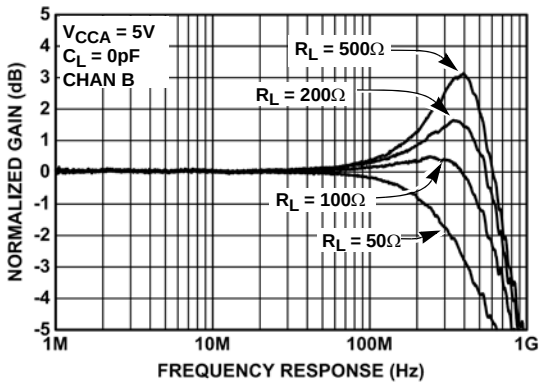


FIGURE 7. DIFFERENTIAL FREQUENCY RESPONSE FOR VARIOUS R_L - DIFF (CHANNEL B)

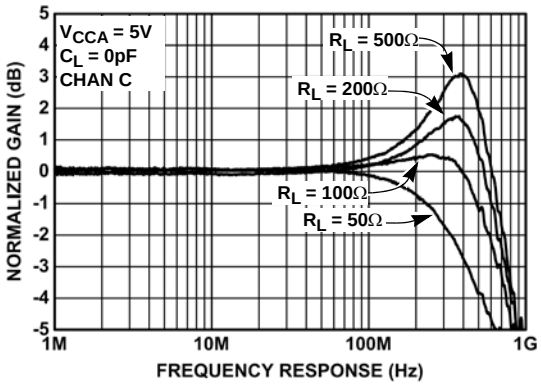


FIGURE 8. DIFFERENTIAL FREQUENCY RESPONSE FOR VARIOUS R_L - DIFF (CHANNEL C)

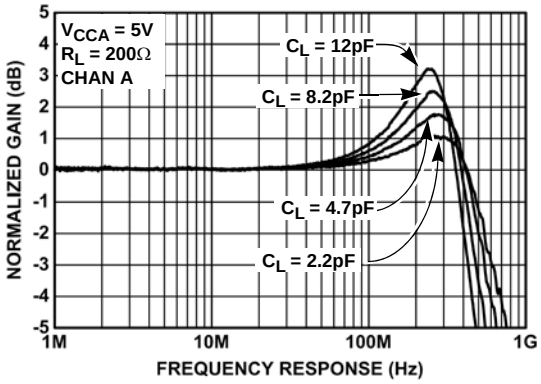


FIGURE 9. DIFFERENTIAL FREQUENCY RESPONSE FOR VARIOUS C_L - DIFF (CHANNEL A)

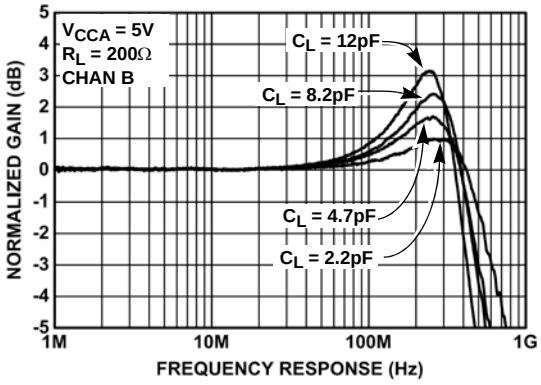


FIGURE 10. DIFFERENTIAL FREQUENCY RESPONSE FOR VARIOUS C_L - DIFF (CHANNEL B)

Typical Performance Curves (Continued)

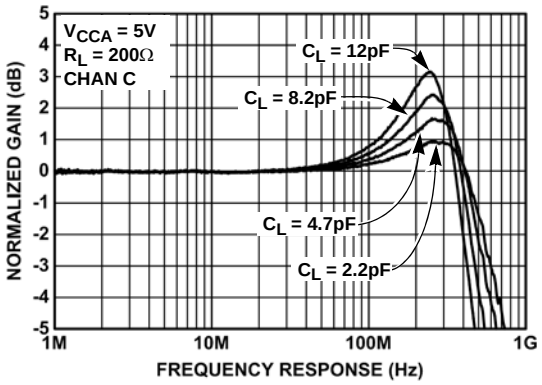


FIGURE 11. DIFFERENTIAL FREQUENCY RESPONSE FOR VARIOUS C_L - DIFF (CHANNEL C)

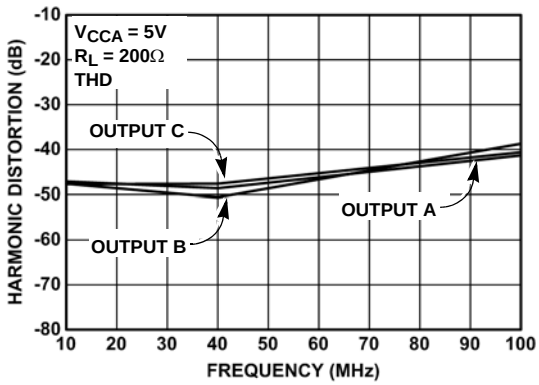


FIGURE 12. TOTAL HARMONIC DISTORTION

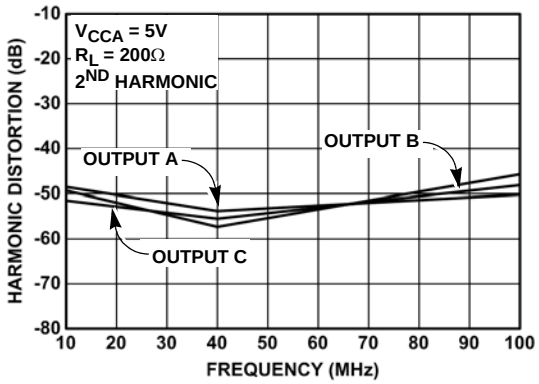


FIGURE 13. 2^{ND} HARMONIC DISTORTION

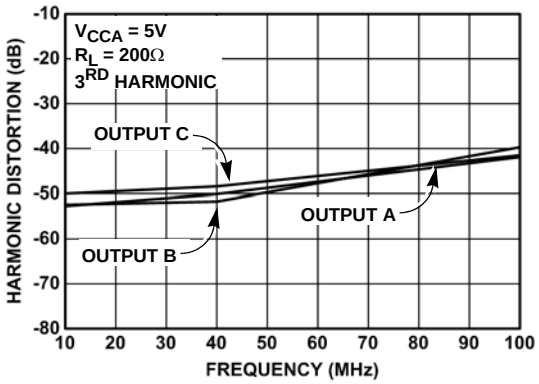


FIGURE 14. 3^{RD} HARMONIC DISTORTION

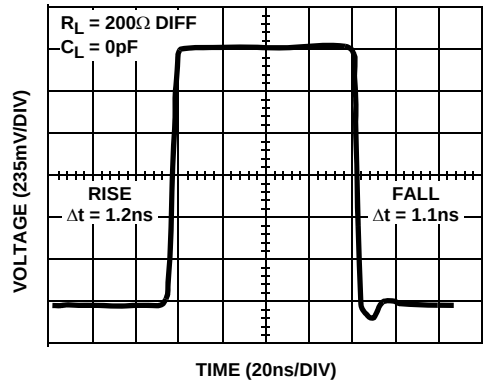


FIGURE 15. DIFFERENTIAL LARGE SIGNAL TRANSIENT RESPONSE

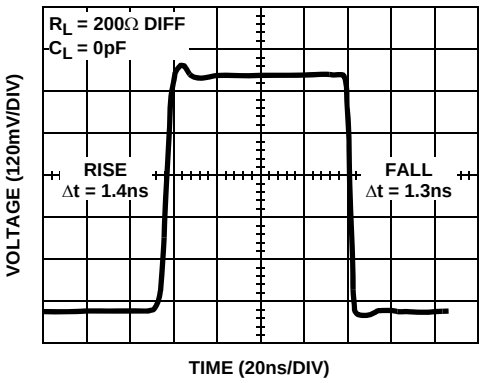


FIGURE 16. DIFFERENTIAL SMALL SIGNAL TRANSIENT RESPONSE

Typical Performance Curves (Continued)

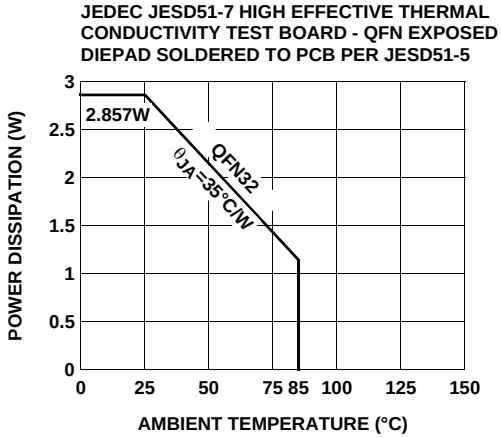


FIGURE 17. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

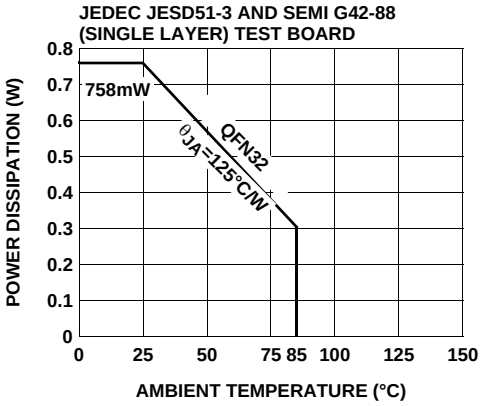


FIGURE 18. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Operational Description and Application Information

Introduction

The ISL59311 is designed to differentially drive composite RGB video signals onto twisted pair lines, while simultaneously encoding horizontal and vertical sync signals as common mode output. The entire video signal plus sync can therefore be transmitted on 3 twisted pairs of wire. When utilizing CAT5 cable, the 4th available twisted pair can be used for transmission of audio, data or control information. The distribution of composite video over standard CAT5 cable enables enormous cost and labor savings compared with traditional coaxial cable, when considering both the relative low price and ease of pulling CAT5 cable.

The digital block of the chip is a data transceiver which is intended to drive one twisted pair line. The maximum baudrate for this block is 50Mbps.

Functional Description

The ISL59311 provides three fully differential high-speed amplifiers, suitable for driving high-resolution composite video signals onto twisted pair or standard coaxial cable. The input common-mode range extends to the negative rail, allowing simple ground-referenced input termination to be used with a single supply. The amplifiers provide a fixed gain of +2 to compensate for standard video cable termination schemes. Horizontal and Vertical sync signals (H_{SYNC} and V_{SYNC}) are passed to an internal Logic Encoding Block to encode the sync information as three discrete signals of different voltage levels. Generally, in differential amplifiers an external V_{REF} pin is used to control the common mode level of the differential output; in the case of the ISL59311 the V_{REF} of each of the three internal amplifier channels receives a signal from the Logic Encoding Block with encoded H_{SYNC} and V_{SYNC} information. The final output consists of three fully differential video signals, with sync encoded on the common mode of each of the three RGB differential signals. H_{SYNC} and V_{SYNC} can easily be separated from the differential output signals, decoded and transmitted along with the RGB video signals to the video monitor.

Sync Transmission

The ISL59311 encodes H_{SYNC} and V_{SYNC} signals on the common mode output of the differential video signals; Red, Green and Blue respectively. Data Sheet Table 1 shows the common mode levels for the different SYNC input combinations. Note that the sum of the common mode voltages results in a fixed average DC level with no AC content. This dramatically reduces EMI radiation into any common mode signal along the twisted pairs of CAT5 cable.

Extract Common Mode Sync and Decode H_{SYNC} and V_{SYNC}

H_{SYNC} and V_{SYNC} can be regenerated from the Common Mode sync output voltages. The relationships between H_{SYNC}, V_{SYNC} and the 3 common mode levels are given by Table 1. The common mode levels are easily separated from the differential outputs of the ISL59311 using this simple resistor network at the cable receiver input of each differential channel; see Figure 20.

TABLE 1. SYNC SIGNAL ENCODING

HSYNC	VSYNC	COMMON MODE A (RED)	COMMON MODE B (GREEN)	COMMON MODE C (BLUE)
Low	High	3.0	2.0	2.5
Low	Low	2.5	3.0	2.0
High	Low	2.0	3.0	2.5
High	High	2.5	2.0	3.0

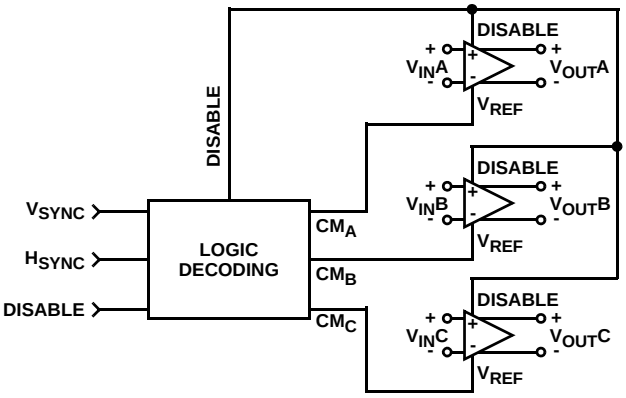


FIGURE 19. VIDEO DRIVER BLOCK DIAGRAM

Twisted Pair Termination

The schematic in Figure 20 illustrates a termination scheme for 50Ω series termination and a 100Ω twisted pair cable. Note RCM is the common mode termination to allow measurement of V_{CM} and should not be too small since it loads the ISL59311; a little over a 100Ω is recommended for RCM.

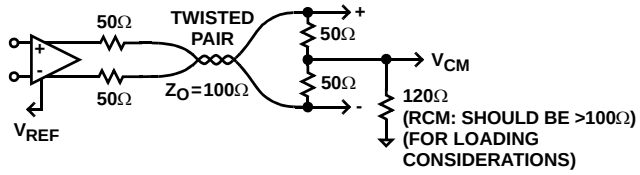


FIGURE 20. TWISTED PAIR TERMINATION

Video Transmission

The ISL59311 is a twisted pair differential line driver directed at the transmission of Video Signals through cables up to 100 feet; however, as signal losses increase with transmission line length the ISL59311 will need additional support to equalize video signals along longer twisted pair transmission lines. A full solution to accomplish this is the SXGA Video Transmission System presented in the ISL59311 Data Sheet. Note the inclusion of the EL9111 for signal equalization of up to 1000ft of CAT5 cable and common mode extraction; see Data Sheet for additional information on the EL9111.

Long Distance Video Transmission

The SXGA Video Transmission System makes it possible to transmit Red, Green and Blue (RGB) video plus sync up to 1000ft through CAT5 cable. The input to the SXGA Video Transmission System is the output of a video source transmitting RGB video signals plus sync. The signals are received initially by the ISL59311; which converts the single ended input RGB signals to three fully differential waveforms with sync encoded on the discrete common modes of each color channel and then drives the signals through a length of CAT5 cable. The signal is received by the EL9111, which can provide 6-pole equalization for both high and low frequency signal transmission line losses. Then the EL9111 converts the differential RGB video signals back into single ended format while extracting the common mode component for decoding. The single ended RGB signal is taken directly from the output of the EL9111 and is ready for the output device. The EL9111 Common Mode Decoder Circuit receives the common mode signals and decodes them and transmits H_{SYNC} and V_{SYNC} to the output device.

Disabling the Amplifiers with the Disable Pin

The Disable pin must be a logic low for normal operation of the video amplifiers. When Disable is taken high, the amplifiers are disabled, reducing supply V_{CCA} supply current. (The Disable pin has no effect on the Serial Digital Transceiver - it is always enabled as long as power is applied to V_{CCD}.)

Serial Digital Transceiver Operation

The digital transceiver is a half-duplex design, either receiving data on the S_{IN} pins and sending it out on the S_{DATA} pin, or transmitting data from the S_{DATA} pin out on some the 2 S_{OUT} pins. The digital transceiver operates in a high speed (up to 50MBaud) differential mode. The S_{DATA} pin is the half-duplex logic-level transmit and receive data pin. S_{DATA} is an output when Transmit = low (receive mode) and an input when Transmit = high (transmit mode). This can be made to work with existing designs that use independent transmit and receive pins by connecting S_{DATA} directly to the transmit pin and through a resistor to the receive pin. Figure 21 shows an example of how to interface the ISL59311 with an RS485 transceiver.

V_{CCD} is the power source for the digital line interface drivers and receivers.

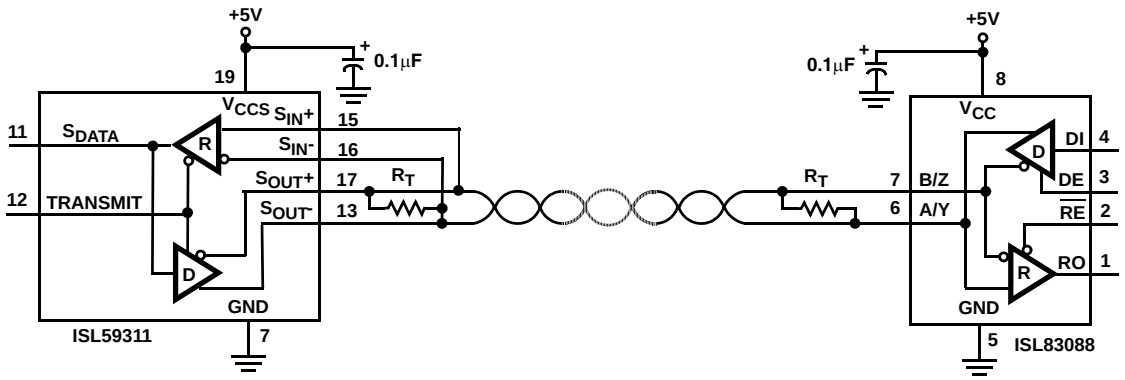
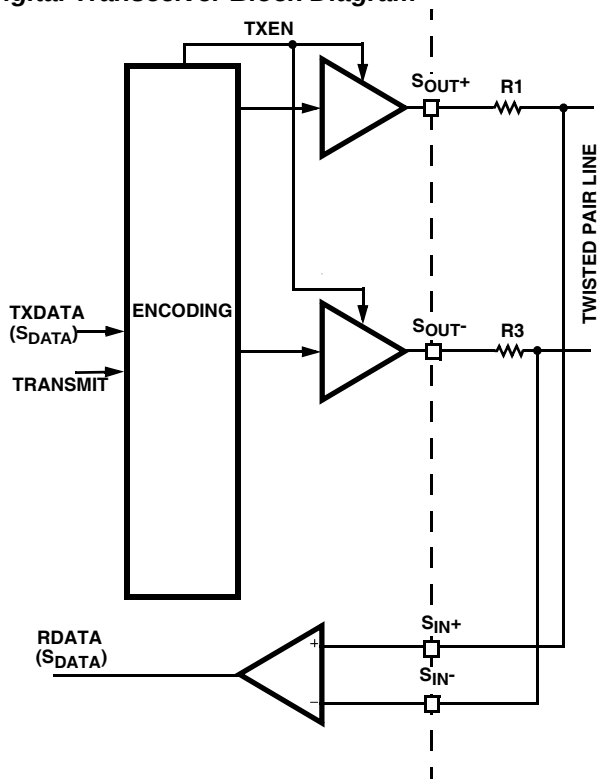


FIGURE 21. RS-485 SERIAL INTERFACE CONNECTION DIAGRAM

Digital Transceiver Block Diagram



Proper Layout Technique

A critical concern with any PCB layout is the establishment of a “healthy” ground plane. It is imperative to provide ground planes terminated close to inputs to minimize input capacitance. Additionally, the ground plane can be selectively removed from inputs to prevent load and supply currents from flowing near the input nodes.

In general the following guidelines apply to all PCB layout:

- Keep all traces as short as possible.
- Keep power supply bypass components as close to the chip as possible - extremely close.
- Create a healthy ground with low impedance and continuous ground pathways available to all grounded components board-wide.
- In high frequency applications on multi-level boards try to keep one level of board with continuous ground plane and minimum via cutouts - providing it is affordable.
- Provide extremely short loops from power pin to ground.
- If it is affordable, a ferrite bead is always of benefit to isolate device from Power Supply noise and the rest of the circuit from the noise of the device.

Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the ISL59311 drive capability is ultimately limited by the rise in die temperature brought about by internal power dissipation. For reliable operation die temperature must be kept below T_{JMAX} (+125°C). It is necessary to calculate the power dissipation for a given application prior to selecting package type. Power dissipation may be calculated:

$$PD = (V_S \times I_S) \times \sum_{1}^{4}(C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f)$$

where:

- V_S is the total power supply to the ISL59311 (= V_{CCD})
- V_{OUT} is the swing on the output (V_H - V_L)
- C_L is the load capacitance
- C_{INT} is the internal load capacitance (80pF max)
- I_S is the quiescent supply current
- f is frequency

Having obtained the application's power dissipation, the maximum junction temperature can be calculated:

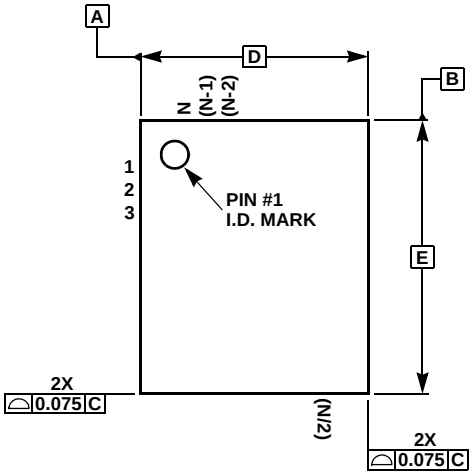
$$T_{JMAX} = T_{MAX} + \Theta_{JA} \times PD$$

where:

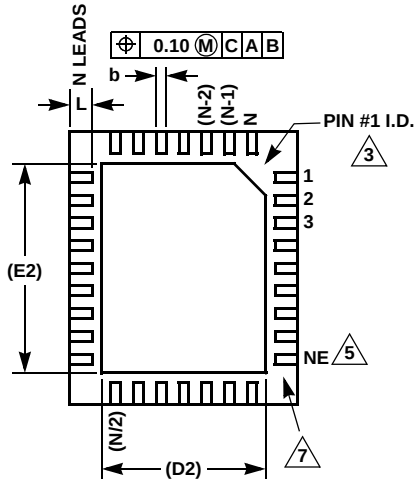
- T_{JMAX} is the maximum junction temperature (+125°C)
- T_{MAX} is the maximum ambient operating temperature
- PD is the power dissipation calculated above

θ_{JA} is the thermal resistance, junction to ambient, of the application (package + PCB combination). Refer to the Package Power Dissipation curves. See Technical Bulletin 389 (http://www.intersil.com/data/tb/TB389.pdf) for additional QFN PCB layout information.

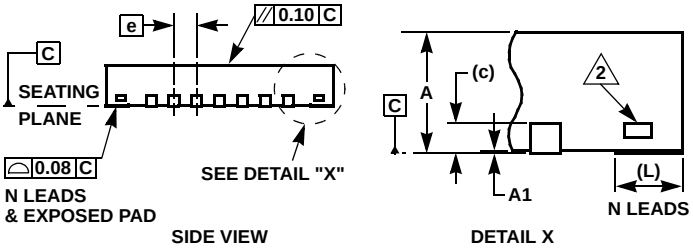
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



TOP VIEW



BOTTOM VIEW



SIDE VIEW DETAIL X

L32.5x6A (One of 10 Packages in MDP0046)

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	0.00	0.02	0.05	-
D		5.00 BSC		-
D2		2.48 REF		-
E		6.00 BSC		-
E2		3.40 REF		-
L	0.45	0.50	0.55	-
b	0.20	0.22	0.24	-
c		0.20 REF		-
e		0.50 BSC		-
N		32 REF		4
ND		7 REF		6
NE		9 REF		5

Rev 0 9/05

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.