

# SC16C2550

Dual UART with 16 bytes of transmit and receive FIFOs and infrared (IrDA) encoder/decoder

Rev. 03 — 19 June 2003

Product data

## 1. Description

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The SC16C2550 is a 2 channel Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data and vice versa. The UART can handle serial data rates up to 5 Mbits/s.

The SC16C2550 is pin compatible with the ST16C2550. It will power-up to be functionally equivalent to the 16C2450. The SC16C2550 provides enhanced UART functions with 16-byte FIFOs, modem control interface, DMA mode data transfer. The DMA mode data transfer is controlled by the FIFO trigger levels and the TXRDY and RXRDY signals. On-board status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by software to meet specific user requirements. An internal loop-back capability allows on-board diagnostics. Independent programmable baud rate generators are provided to select transmit and receive baud rates.

The SC16C2550 operates at 5 V, 3.3 V and 2.5 V and the Industrial temperature range, and is available in plastic PLCC44, LQFP48 and DIP40 packages.

## 2. Features

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- 2 channel UART
- 5 V, 3.3 V and 2.5 V operation
- Industrial temperature range
- Pin and functionally compatible to 16C2450 and software compatible with INS8250, SC16C550
- Up to 5 Mbits/s data rate at 5 V and 3.3 V, and 3 Mbits/s at 2.5 V
- 16 byte transmit FIFO to reduce the bandwidth requirement of the external CPU
- 16 byte receive FIFO with error flags to reduce the bandwidth requirement of the external CPU
- Independent transmit and receive UART control
- Four selectable Receive FIFO interrupt trigger levels
- Automatic software/hardware flow control
- Programmable Xon/Xoff characters
- Software selectable Baud Rate Generator
- Sleep mode
- Standard asynchronous error and framing bits (Start, Stop, and Parity Overrun Break)
- Transmit, Receive, Line Status, and Data Set interrupts independently controlled



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- Fully programmable character formatting:
  - ◆ 5-, 6-, 7-, or 8-bit characters
  - ◆ Even-, Odd-, or No-Parity formats
  - ◆ 1-, 1½-, or 2-stop bit
  - ◆ Baud generation (DC to 1.5 Mbit/s)
- False start-bit detection
- Complete status reporting capabilities
- 3-State output TTL drive capabilities for bi-directional data bus and control bus
- Line Break generation and detection
- Internal diagnostic capabilities:
  - ◆ Loop-back controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ( $\overline{\text{CTS}}$ ,  $\overline{\text{RTS}}$ ,  $\overline{\text{DSR}}$ ,  $\overline{\text{DTR}}$ ,  $\overline{\text{RI}}$ ,  $\overline{\text{DCD}}$ ).

### 3. Ordering information

Table 1: Ordering information

| Type number   | Package |  |          |
|---------------|---------|--|----------|
|               | Name    | Description  | Version  |
| SC16C2550IN40 | DIP40   | plastic dual in-line package; 40 leads (600 mil)                     | SOT129-1 |
| SC16C2550IA44 | PLCC44  | plastic leaded chip carrier; 44 leads                                | SOT187-2 |
| SC16C2550IB48 | LQFP48  | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |

### 4. Block diagram

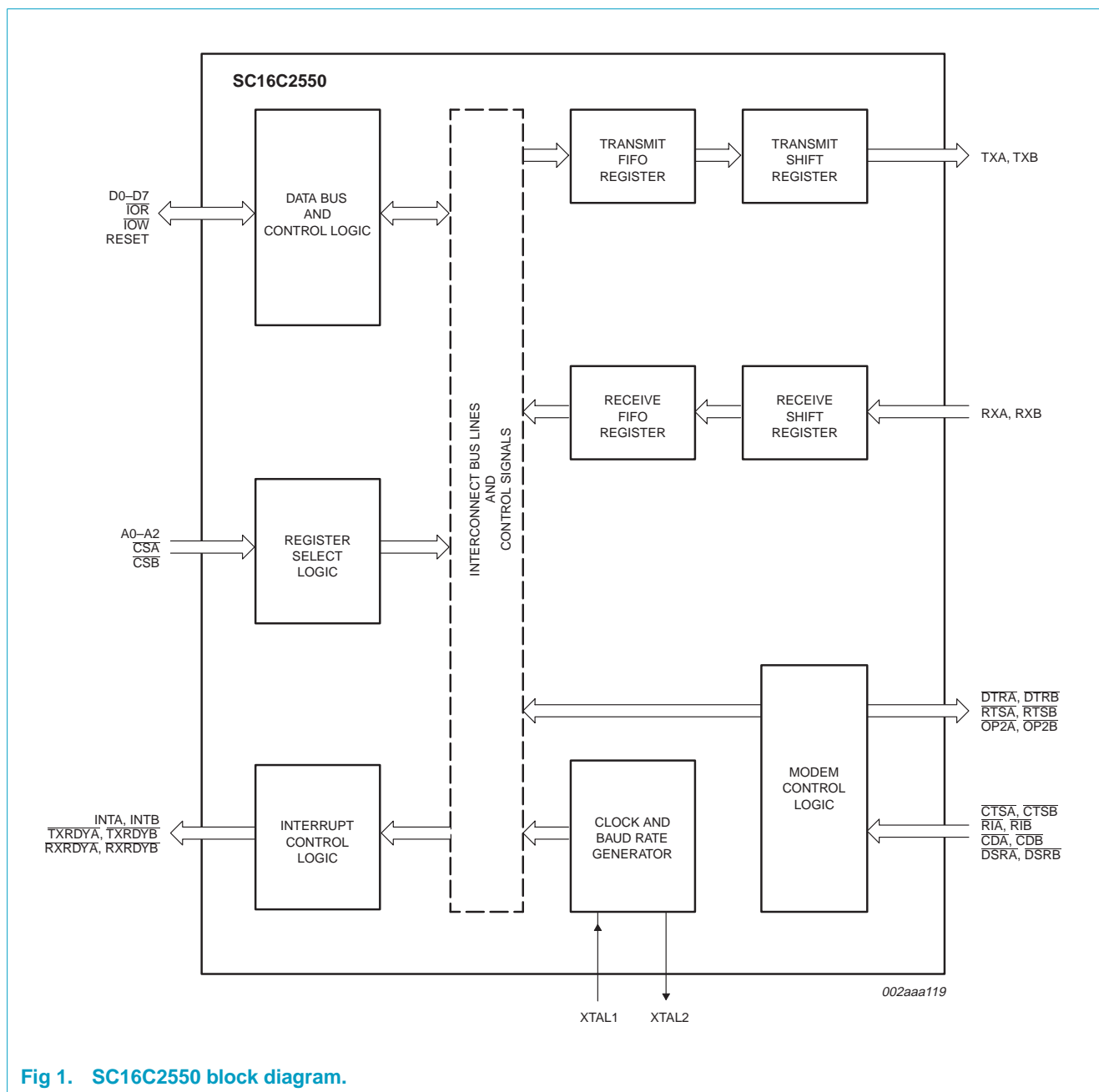
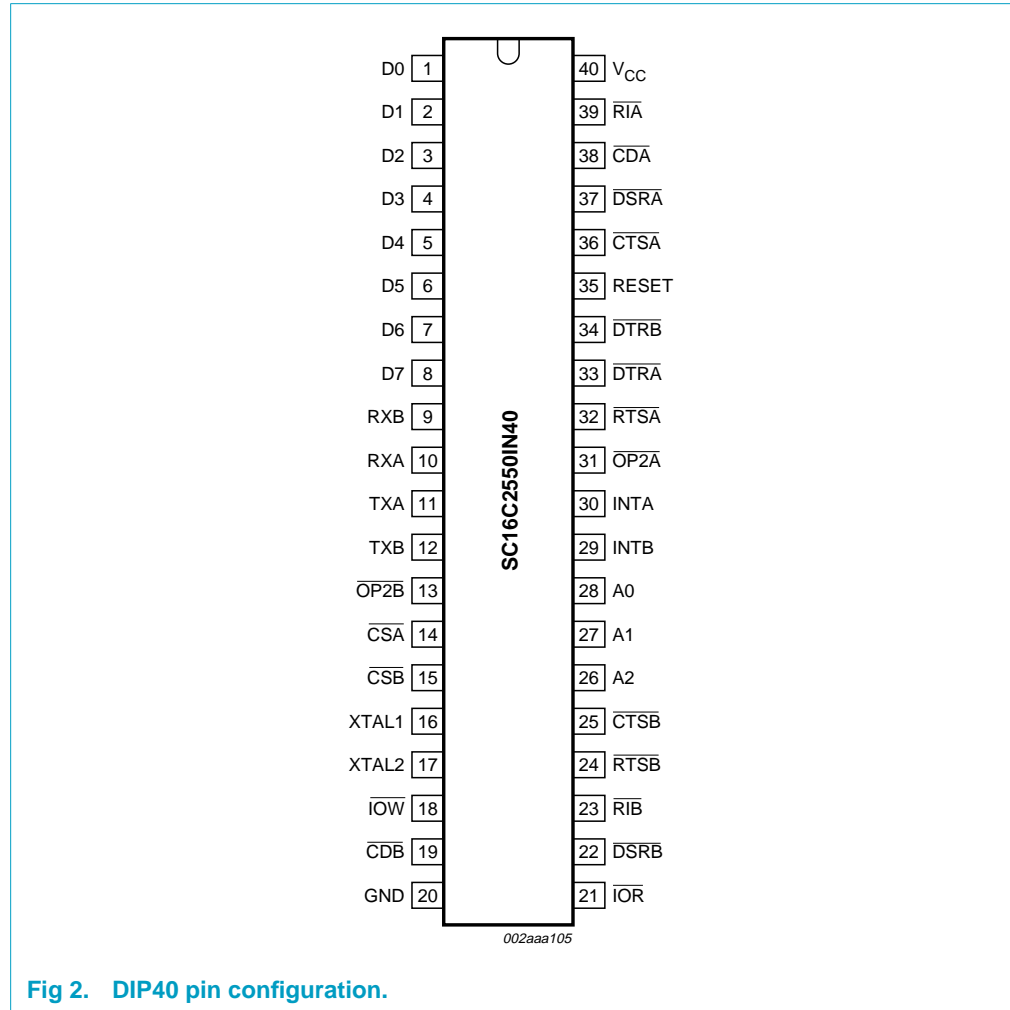


Fig 1. SC16C2550 block diagram.

## 5. Pinning information

### 5.1 Pinning



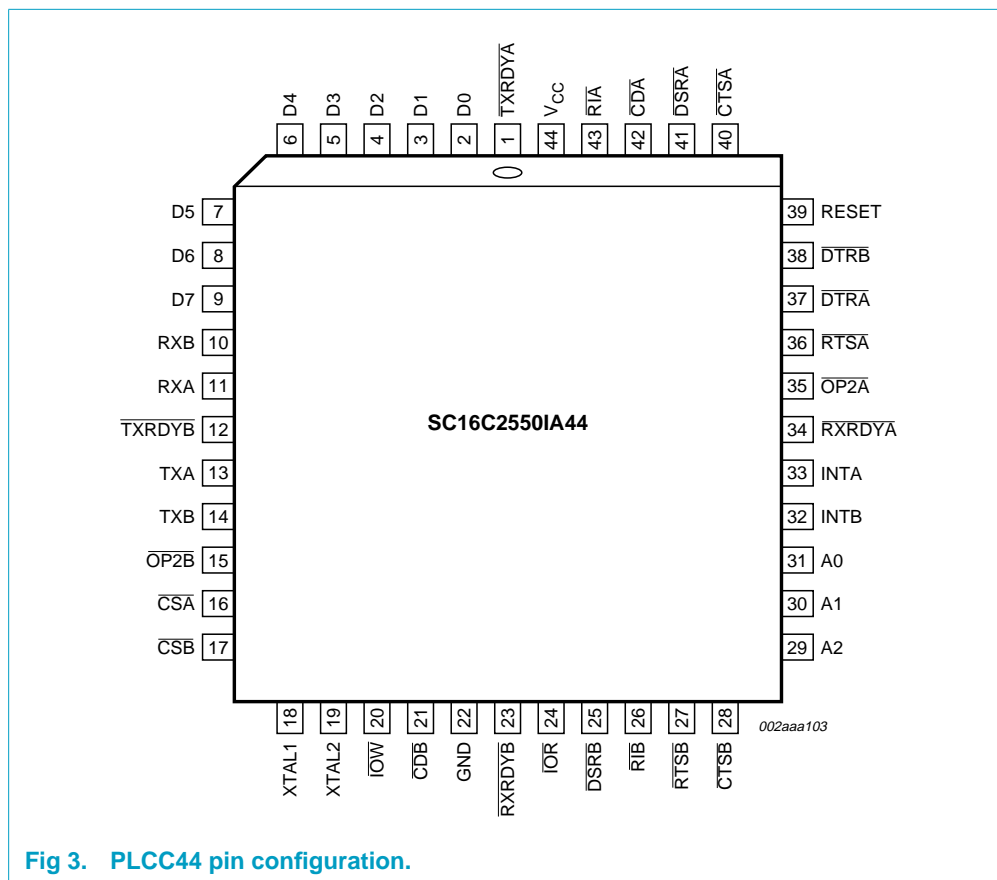


Fig 3. PLCC44 pin configuration.

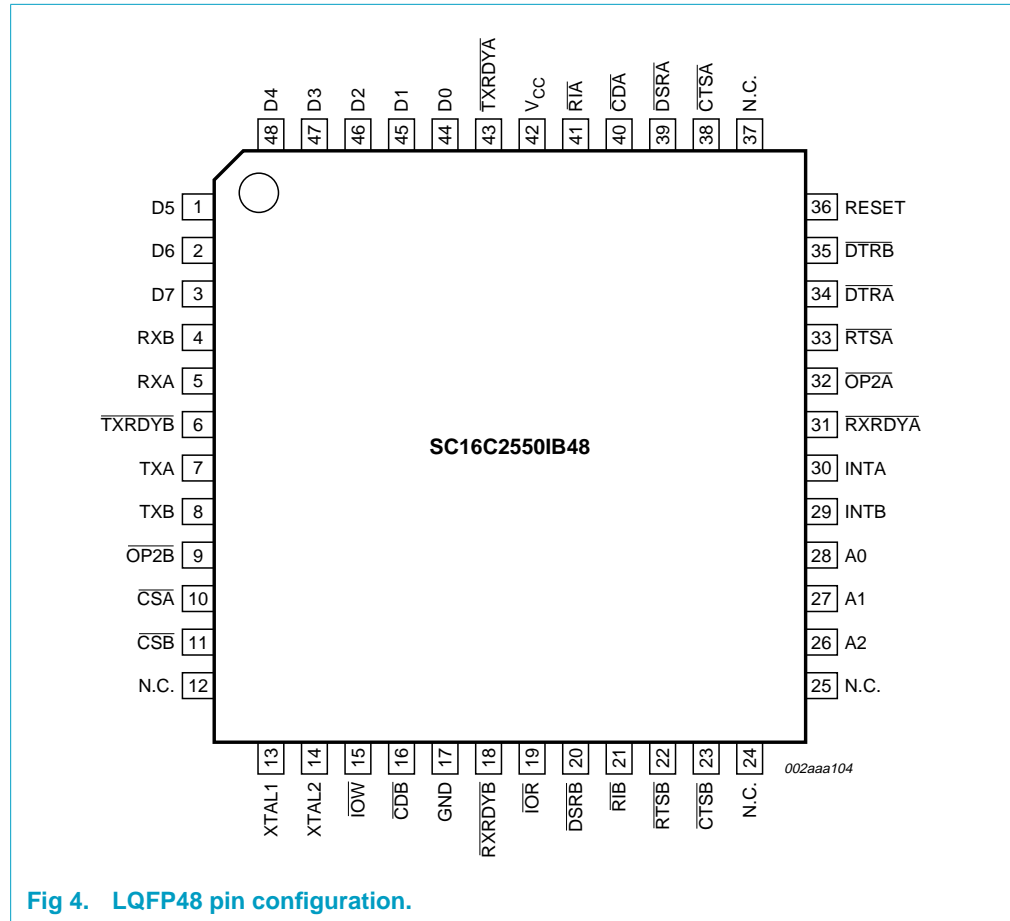


Fig 4. LQFP48 pin configuration.

### 5.2 Pin description

Table 2: Pin description

| Symbol                              | Pin    |        |            | Type | Description  |
|-------------------------------------|--------|--------|------------|------|--|
|                                     | DIP40  | PLCC44 | LQFP48     |      |  |
| A0                                  | 28     | 31     | 28         | I    | <b>Address 0 select bit.</b> Internal register address selection.  |
| A1                                  | 27     | 30     | 27         | I    | <b>Address 1 select bit.</b> Internal register address selection.  |
| A2                                  | 26     | 29     | 26         | I    | <b>Address 2 select bit.</b> Internal register address selection.  |
| $\overline{CSA}$ , $\overline{CSB}$ | 14, 15 | 16, 17 | 10, 11     | I    | <b>Chip Select A, B (Active-LOW).</b> This function is associated with individual channels, A through B. These pins enable data transfers between the user CPU and the SC16C2550 for the channel(s) addressed. Individual UART sections (A, B) are addressed by providing a logic 0 on the respective $\overline{CSA}$ , $\overline{CSB}$ pin. |
| D0-D7                               | 1-8    | 2-9    | 44-48, 1-3 | I/O  | <b>Data bus (bi-directional).</b> These pins are the 8-bit, 3-State data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.  |
| GND                                 | 20     | 22     | 17         | I    | <b>Signal and power ground.</b>  |

Table 2: Pin description...continued

| Symbol   | Pin    |        |        | Type | Description   |
|--|--------|--------|--------|------|---|
|  | DIP40  | PLCC44 | LQFP48 |      |   |
| INTA,<br>INTB  | 30, 29 | 33, 32 | 30, 29 | O    | <b>Interrupt A, B (3-State).</b> This function is associated with individual channel interrupts, INTA, INTB. INTA, INTB are enabled when MCR bit 3 is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and is active when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected.   |
| $\overline{\text{IOR}}$                                    | 21     | 24     | 19     | I    | <b>Read strobe (Active-LOW strobe).</b> A logic 0 transition on this pin will load the contents of an internal register defined by address bits A0-A2 onto the SC16C2550 data bus (D0-D7) for access by external CPU.   |
| $\overline{\text{IOW}}$                                    | 18     | 20     | 15     | I    | <b>Write strobe (Active-LOW strobe).</b> A logic 0 transition on this pin will transfer the contents of the data bus (D0-D7) from the external CPU to an internal register that is defined by address bits A0-A2.   |
| $\overline{\text{OP2A}}$ ,<br>$\overline{\text{OP2B}}$     | 31, 13 | 35, 15 | 32, 9  | O    | <b>Output 2 (user-defined).</b> This function is associated with individual channels, A through B. The state at these pin(s) are defined by the user and through MCR register bit 3. INTA, INTB are set to the active mode and $\overline{\text{OP2}}$ to logic 0 when MCR[3] is set to a logic 1. INTA, INTB are set to the 3-State mode and $\overline{\text{OP2}}$ to a logic 1 when MCR[3] is set to a logic 0. See bit 3, Modem Control Register (MCR[3]). Since these bits control both the INTA, INTB operation and $\overline{\text{OP2}}$ outputs, only one function should be used at one time, INT or $\overline{\text{OP2}}$ .  |
| RESET  | 35     | 39     | 36     | I    | <b>Reset (Active-HIGH).</b> A logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See <a href="#">Section 7.11 "SC16C2550 external reset condition"</a> for initialization details.)   |
| $\overline{\text{RXRDYA}}$ ,<br>$\overline{\text{RXRDYB}}$ | -      | 34, 23 | 31, 18 | O    | <b>Receive Ready A, B (Active-LOW).</b> This function is associated with PLCC44 and LQFP48 packages only. This function provides the RX FIFO/RHR status for individual receive channels (A-B). $\overline{\text{RXRDYn}}$ is primarily intended for monitoring DMA mode 1 transfers for the receive data FIFOs. A logic 0 indicates there is a receive data to read/upload, i.e., receive ready status with one or more RX characters available in the FIFO/RHR. This pin is a logic 1 when the FIFO/RHR is empty or when the programmed trigger level has not been reached. This signal can also be used for single mode transfers (DMA mode 0).   |
| $\overline{\text{TXRDYA}}$ ,<br>$\overline{\text{TXRDYB}}$ | -      | 1, 12  | 43, 6  | O    | <b>Transmit Ready A, B (Active-LOW).</b> This function is associated with PLCC44 and LQFP48 packages only. These outputs provide the TX FIFO/THR status for individual transmit channels (A-B). $\overline{\text{TXRDYn}}$ is primarily intended for monitoring DMA mode 1 transfers for the transmit data FIFOs. An individual channel's $\overline{\text{TXRDYA}}$ , $\overline{\text{TXRDYB}}$ buffer ready status is indicated by logic 0, i.e., at least one location is empty and available in the FIFO or THR. This pin goes to a logic 1 (DMA mode 1) when there are no more empty locations in the FIFO or THR. This signal can also be used for single mode transfers (DMA mode 0). |
| V <sub>CC</sub>  | 40     | 44     | 42     | I    | <b>Power supply input.</b>  |
| XTAL1  | 16     | 18     | 13     | I    | <b>Crystal or external clock input.</b> Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit. This configuration requires an external 1 M $\Omega$ resistor between the XTAL1 and XTAL2 pins. Alternatively, an external clock can be connected to this pin to provide custom data rates. (See <a href="#">Section 6.8 "Programmable baud rate generator"</a> .) See <a href="#">Figure 5</a> .   |

Table 2: Pin description...continued

| Symbol                                   | Pin    |        |        | Type | Description   |
|--|--------|--------|--------|------|---|
|  | DIP40  | PLCC44 | LQFP48 |      |   |
| XTAL2                                    | 17     | 19     | 14     | O    | <b>Output of the crystal oscillator or buffered clock.</b> (See also XTAL1.) Crystal oscillator output or buffered clock output. Should be left open if an external clock is connected to XTAL1. For extended frequency operation, this pin should be tied to $V_{CC}$ via a 2 k $\Omega$ resistor.   |
| $\overline{CDA}$ ,<br>$\overline{CDB}$   | 38, 19 | 42, 21 | 40, 16 | I    | <b>Carrier Detect (Active-LOW).</b> These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.  |
| $\overline{CTSA}$ ,<br>$\overline{CTSB}$ | 36, 25 | 40, 28 | 38, 23 | I    | <b>Clear to Send (Active-LOW).</b> These inputs are associated with individual UART channels, A through B. A logic 0 on the $\overline{CTS}$ pin indicates the modem or data set is ready to accept transmit data from the SC16C2550. Status can be tested by reading MSR[4]. This pin has no effect on the UART's transmit or receive operation.   |
| $\overline{DSRA}$ ,<br>$\overline{DSRB}$ | 37, 22 | 41, 25 | 39, 20 | I    | <b>Data Set Ready (Active-LOW).</b> These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation.   |
| $\overline{DTRA}$ ,<br>$\overline{DTRB}$ | 33, 34 | 37, 38 | 34, 35 | O    | <b>Data Terminal REady (Active-LOW).</b> These outputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates that the SC16C2550 is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR[0] will set the $\overline{DTR}$ output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR[0], or after a reset. This pin has no effect on the UART's transmit or receive operation. |
| $\overline{RIA}$ , $\overline{RIB}$      | 39, 23 | 43, 26 | 41, 21 | I    | <b>Ring Indicator (Active-LOW).</b> These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.   |
| $\overline{RTSA}$ ,<br>$\overline{RTSB}$ | 32, 24 | 36, 27 | 33, 22 | O    | <b>Request to Send (Active-LOW).</b> These outputs are associated with individual UART channels, A through B. A logic 0 on the $\overline{RTS}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset this pin will be set to a logic 1. This pin has no effect on the UART's transmit or receive operation.   |
| RXA, RXB                                 | 10, 9  | 11, 10 | 5, 4   | I    | <b>Receive data A, B.</b> These inputs are associated with individual serial channel data to the SC16C2550 receive input circuits, A-B. The RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the RX input pin is disabled and TX data is connected to the UART RX input, internally.   |
| TXA, TXB                                 | 11, 12 | 13, 14 | 7, 8   | O    | <b>Transmit data A, B.</b> These outputs are associated with individual serial transmit channel data from the SC16C2550. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the TX output pin is disabled and TX data is internally connected to the UART RX input.  |



## 6. Functional description

The SC16C2550 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex, especially when manufactured on a single integrated silicon chip. The SC16C2550 represents such an integration with greatly enhanced features. The SC16C2550 is fabricated with an advanced CMOS process.

The SC16C2550 is an upward solution that provides a dual UART capability with 16 bytes of transmit and receive FIFO memory, instead of none in the 16C2450. The SC16C2550 is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C2550 by the transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C2450 without a receive FIFO, will require unloading of the RHR in 93 microseconds (this example uses a character length of 11 bits, including start/stop bits at 115.2 kbits/s). This means the external CPU will have to service the receive FIFO less than every 100 microseconds. However, with the 16 byte FIFO in the SC16C2550, the data buffer will not require unloading/loading for 1.53 ms. This increases the service interval, giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the four selectable receive FIFO trigger interrupt levels is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C2550 is capable of operation up to 5 Mbits/s with a 80 MHz clock. With a crystal or external clock input of 7.3728 MHz, the user can select data rates up to 460.8 kbits/s.

The rich feature set of the SC16C2550 is available through internal registers. Selectable receive FIFO trigger levels, selectable TX and RX baud rates, and modem interface controls are all standard features. Following a power-on reset or an external reset, the SC16C2550 is software compatible with the previous generation, ST16C2450.

### 6.1 UART A-B functions

The UART provides the user with the capability to bi-directionally transfer information between an external CPU, the SC16C2550 package, and an external serial device. A logic 0 on chip select pins  $\overline{\text{CSA}}$  and/or  $\overline{\text{CSB}}$  allows the user to configure, send data, and/or receive data via UART channels A-B. Individual channel select functions are shown in [Table 3](#).

Table 3: Serial port selection

| Chip Select  | Function       |
|--|----------------|
| $\overline{\text{CSA}}\text{-}\overline{\text{CSB}} = 1$ | none           |
| $\overline{\text{CSA}} = 0$                              | UART channel A |
| $\overline{\text{CSB}} = 0$                              | UART channel B |

## 6.2 Internal registers

The SC16C2550 provides two sets of internal registers (A and B) consisting of 12 registers each for monitoring and controlling the functions of each channel of the UART. These registers are shown in Table 4. The UART registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible scratchpad register (SPR).

Table 4: Internal registers decoding

| A2   | A1 | A0 | READ mode                 | WRITE mode                |
|--|----|----|---------------------------|---------------------------|
| <b>General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LSR, SPR)<sup>[1]</sup></b> |    |    |                           |                           |
| 0  | 0  | 0  | Receive Holding Register  | Transmit Holding Register |
| 0  | 0  | 1  |                           | Interrupt Enable Register |
| 0  | 1  | 0  | Interrupt Status Register | FIFO Control Register     |
| 0  | 1  | 1  |                           | Line Control Register     |
| 1  | 0  | 0  |                           | Modem Control Register    |
| 1  | 0  | 1  | Line Status Register      | n/a                       |
| 1  | 1  | 0  | Modem Status Register     | n/a                       |
| 1  | 1  | 1  | Scratchpad Register       | Scratchpad Register       |
| <b>Baud rate register set (DLL/DLM)<sup>[2]</sup></b>                                |    |    |                           |                           |
| 0  | 0  | 0  | LSB of Divisor Latch      | LSB of Divisor Latch      |
| 0  | 0  | 1  | MSB of Divisor Latch      | MSB of Divisor Latch      |
| <b>Enhanced register set (EFR, Xon/off 1-2)<sup>[3]</sup></b>                        |    |    |                           |                           |
| 0  | 1  | 0  | Enhanced Feature Register | Enhanced Feature Register |
| 1  | 0  | 0  | Xon1 word                 | Xon1 word                 |
| 1  | 0  | 1  | Xon2 word                 | Xon2 word                 |
| 1  | 1  | 0  | Xoff1 word                | Xoff1 word                |
| 1  | 1  | 1  | Xoff2 word                | Xoff2 word                |

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

[3] Enhanced Feature Register, Xon1, 2 and Xoff1, 2 are accessible only when the LCR is set to 'BF(HEX)'.

### 6.3 FIFO operation

The 16 byte transmit and receive data FIFOs are enabled by the FIFO Control Register (FCR) bit 0. The user can set the receive trigger level via FCR bits 6-7, but not the transmit trigger level. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

**Table 5: Flow control mechanism**

| Selected trigger level (characters) | INT pin activation | Negate $\overline{\text{RTS}}$ or send Xoff | Assert $\overline{\text{RTS}}$ or send Xon |
|-------------------------------------|--------------------|---|--|
| 1                                   | 1                  | 4   | 1  |
| 4                                   | 4                  | 8   | 4  |
| 8                                   | 8                  | 12  | 8  |
| 14                                  | 14                 | 14  | 10   |

### 6.4 Hardware flow control

When automatic hardware flow control is enabled, the SC16C2550 monitors the  $\overline{\text{CTS}}$  pin for a remote buffer overflow indication and controls the  $\overline{\text{RTS}}$  pin for local buffer overflows. Automatic hardware flow control is selected by setting EFR[6] (RTS) and EFR[7] (CTS) to a logic 1. If  $\overline{\text{CTS}}$  transitions from a logic 0 to a logic 1 indicating a flow control request, ISR[5] will be set to a logic 1 (if enabled via IER[6,7]), and the SC16C2550 will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the  $\overline{\text{CTS}}$  input returns to a logic 0, indicating more data may be sent.

With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The  $\overline{\text{RTS}}$  pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the next trigger level. However, the  $\overline{\text{RTS}}$  pin will return to a logic 0 after the data buffer (FIFO) is unloaded to the next trigger level below the programmed trigger. However, under the above described conditions, the SC16C2550 will continue to accept data until the receive FIFO is full.

### 6.5 Software flow control

When software flow control is enabled, the SC16C2550 compares one or two sequential receive data characters with the programmed Xon/Xoff or Xoff1,2 character value(s). If received character(s) match the programmed values, the SC16C2550 will halt transmission (TX) as soon as the current character(s) has completed transmission. When a match occurs, the receive ready (if enabled via Xoff IER[5]) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. Following a suspension due to a match of the Xoff characters' values, the SC16C2550 will monitor the receive data stream for a match to the Xon1,2 character value(s). If a match is found, the SC16C2550 will resume operation and clear the flags (ISR[4]).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset, the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected,

the SC16C2550 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overflowing and flow control needs to be executed, the SC16C2550 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The SC16C2550 sends the Xoff1,2 characters as soon as received data passes the programmed trigger level. To clear this condition, the SC16C2550 will transmit the programmed Xon1,2 characters as soon as receive data drops below the programmed trigger level.

## 6.6 Special feature software flow control

A special feature is provided to detect an 8-bit character when EFR[5] is set. When 8-bit character is detected, it will be placed on the user-accessible data stack along with normal incoming RX data. This condition is selected in conjunction with EFR[0-3]. Note that software flow control should be turned off when using this special mode by setting EFR[0-3] to a logic 0.

The SC16C2550 compares each incoming receive character with Xoff2 data. If a match exists, the received data will be transferred to the FIFO, and ISR[4] will be set to indicate detection of a special character. Although the Internal Register Table (Table 7) shows each X-Register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register bits LCR[0-1] define the number of character bits, i.e., either 5 bits, 6 bits, 7 bits or 8 bits. The word length selected by LCR[0-1] also determine the number of bits that will be used for the special character comparison. Bit 0 in the X-registers corresponds with the LSB bit for the receive character.

## 6.7 Hardware/software and time-out interrupts

The interrupts are enabled by IER[0-3]. Care must be taken when handling these interrupts. Following a reset, if Interrupt Enable Register (IER) bit 1 = 1, the SC16C2550 will issue a Transmit Holding Register interrupt. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. It could be noted that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/RTS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER[3]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C2550 FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the

receive holding register (RHR) is read. The actual time-out value is 4 character time, including data information length, start bit, parity bit, and the size of stop bit, i.e., 1×, 1.5×, or 2× bit times.

## 6.8 Programmable baud rate generator

The SC16C2550 supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s. The SC16C2550 can support a standard data rate of 921.6 kbit/s.

A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of operating with a frequency of up to 80 MHz. To obtain maximum data rate, it is necessary to use full rail swing on the clock input. The SC16C2550 can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal is connected externally between the XTAL1 and XTAL2 pins. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 6).

The generator divides the input 16× clock by any divisor from 1 to  $2^{16} - 1$ . The SC16C2550 divides the basic external clock by 16. The basic 16× clock provides table rates to support standard and custom applications using the same system design. The rate table is configured via the DLL and DLM internal register functions. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 6 shows the selectable baud rate table available when using a 1.8432 MHz external clock input.

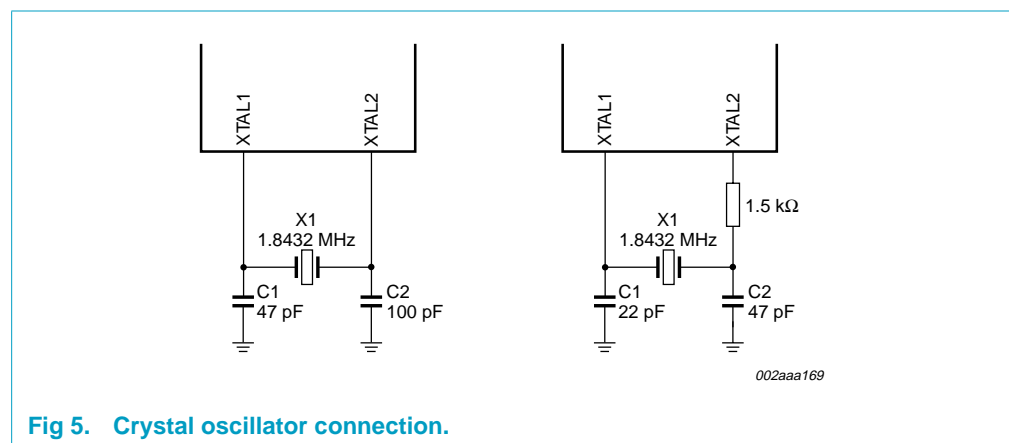


Fig 5. Crystal oscillator connection.

Table 6: Baud rate generator programming table using a 1.8432 MHz clock

| Output baud rate | Output 16 × clock divisor (decimal) | Output 16 × clock divisor (HEX) | DLM program value (HEX) | DLL program value (HEX) |
|------------------|-------------------------------------|---------------------------------|-------------------------|-------------------------|
| 50               | 2304                                | 900                             | 09                      | 00                      |
| 75               | 1536                                | 600                             | 06                      | 00                      |
| 110              | 1047                                | 417                             | 04                      | 17                      |
| 150              | 768                                 | 300                             | 03                      | 00                      |
| 300              | 384                                 | 180                             | 01                      | 80                      |
| 600              | 192                                 | C0                              | 00                      | C0                      |
| 1200             | 96                                  | 60                              | 00                      | 60                      |
| 2400             | 48                                  | 30                              | 00                      | 30                      |
| 3600             | 32                                  | 20                              | 00                      | 20                      |
| 4800             | 24                                  | 18                              | 00                      | 18                      |
| 7200             | 16                                  | 10                              | 00                      | 10                      |
| 9600             | 12                                  | 0C                              | 00                      | 0C                      |
| 19.2 k           | 6                                   | 06                              | 00                      | 06                      |
| 38.4 k           | 3                                   | 03                              | 00                      | 03                      |
| 57.6 k           | 2                                   | 02                              | 00                      | 02                      |
| 115.2 k          | 1                                   | 01                              | 00                      | 01                      |

## 6.9 DMA operation

The SC16C2550 FIFO trigger level provides additional flexibility to the user for block mode operation. LSR[5,6] provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). When the transmit and receive FIFOs are enabled and the DMA mode is de-activated (DMA Mode 0), the SC16C2550 activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode 1), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the receive trigger level and the transmit FIFO. In this mode, the SC16C2550 sets the TXRDY (or RXRDY) output pin when characters in the transmit FIFO is below 16, or the characters in the receive FIFOs are above the receive trigger level.

## 6.10 Loop-back mode

The internal loop-back capability allows on-board diagnostics. In the loop-back mode, the normal modem interface pins are disconnected and reconfigured for loop-back internally (see Figure 6). MCR[0-3] register bits are used for controlling loop-back diagnostic testing. In the loop-back mode, the transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally. The CTS, DSR, CD, and RI are disconnected from their normal modem control inputs pins, and instead are connected internally to RTS, DTR, MCR[3] (OP2) and MCR[2] (OP1). Loop-back test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel

data that is then made available at the user data interface D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational.

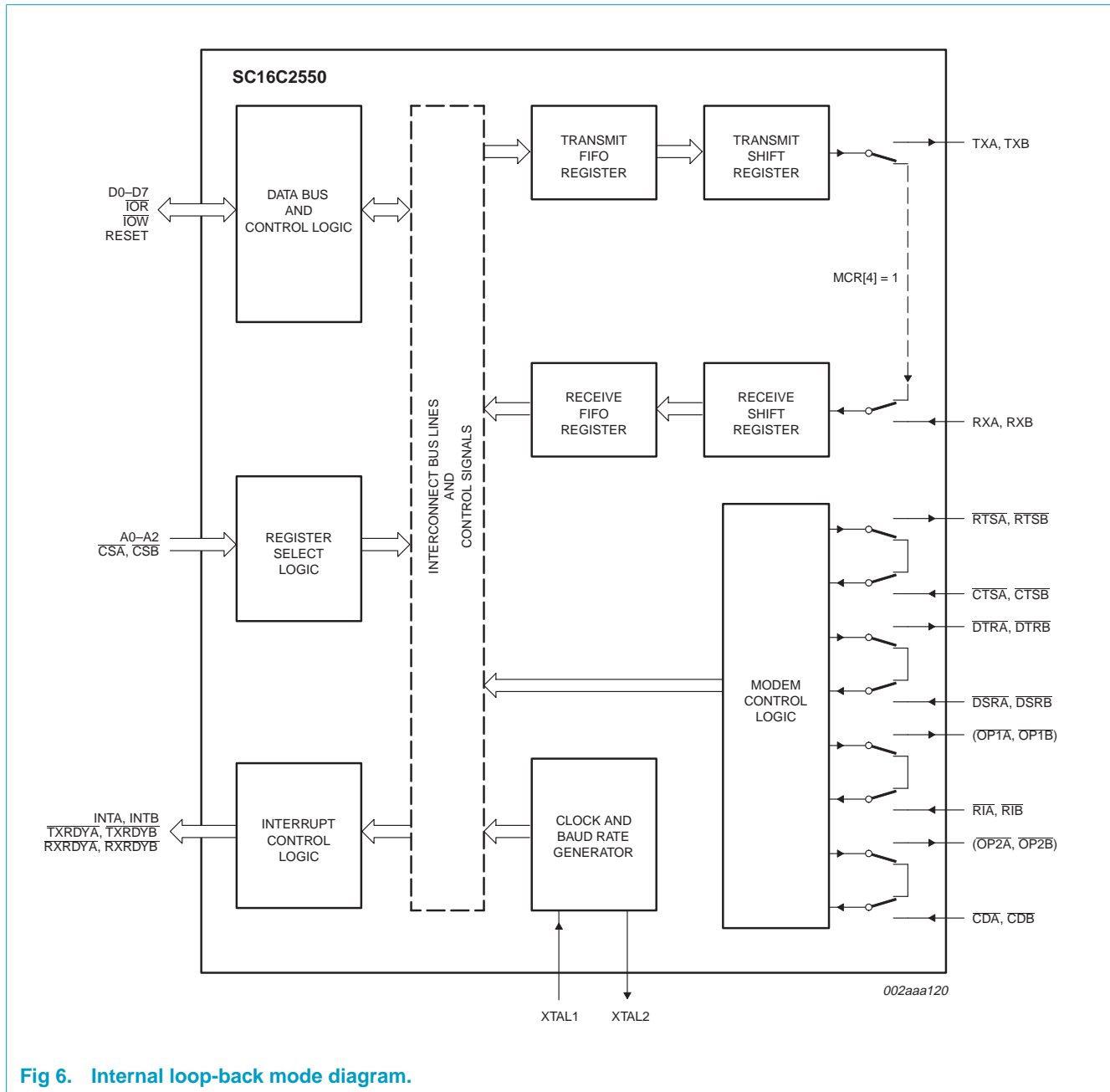


Fig 6. Internal loop-back mode diagram.



## 7. Register descriptions

**Table 7** details the assigned bit functions for the SC16C2550 internal registers. The assigned bit functions are more fully defined in [Section 7.1](#) through [Section 7.11](#).

**Table 7: SC16C2550 internal registers**

Shaded bits are only accessible when EFR[4] is set.

| A2   | A1 | A0 | Register | Default <sup>[1]</sup> | Bit 7                | Bit 6              | Bit 5                | Bit 4   | Bit 3                  | Bit 2                         | Bit 1                               | Bit 0                    |
|--|----|----|----------|------------------------|----------------------|--------------------|----------------------|---|------------------------|-------------------------------|-------------------------------------|--------------------------|
| <b>General Register Set<sup>[2]</sup></b>  |    |    |          |                        |                      |                    |                      |   |                        |                               |                                     |                          |
| 0  | 0  | 0  | RHR      | XX                     | bit 7                | bit 6              | bit 5                | bit 4   | bit 3                  | bit 2                         | bit 1                               | bit 0                    |
| 0  | 0  | 0  | THR      | XX                     | bit 7                | bit 6              | bit 5                | bit 4   | bit 3                  | bit 2                         | bit 1                               | bit 0                    |
| 0  | 0  | 1  | IER      | 00                     | CTS interrupt        | RTS interrupt      | Xoff interrupt       | Sleep mode                                    | modem status interrupt | receive line status interrupt | transmit holding register interrupt | receive holding register |
| 0  | 1  | 0  | FCR      | 00                     | RCVR trigger (MSB)   | RCVR trigger (LSB) | reserved 0           | reserved 0                                    | DMA mode select        | XMIT FIFO reset               | RCVR FIFO reset                     | FIFOs enable             |
| 0  | 1  | 0  | ISR      | 01                     | FIFOs enabled        | FIFOs enabled      | INT priority bit 4   | INT priority bit 3                            | INT priority bit 2     | INT priority bit 1            | INT priority bit 0                  | INT status               |
| 0  | 1  | 1  | LCR      | 00                     | divisor latch enable | set break          | set parity           | even parity                                   | parity enable          | stop bits                     | word length bit 1                   | word length bit 0        |
| 1  | 0  | 0  | MCR      | 00                     | 0                    | IR enable          | 0                    | loop back                                     | OP2/INT enable         | (OP1)                         | RTS                                 | DTR                      |
| 1  | 0  | 1  | LSR      | 60                     | FIFO data error      | THR and TSR empty  | THR empty            | break interrupt                               | framing error          | parity error                  | overrun error                       | receive data ready       |
| 1  | 1  | 0  | MSR      | X0                     | CD                   | RI                 | DSR                  | CTS   | $\Delta\overline{CD}$  | $\Delta\overline{RI}$         | $\Delta\overline{DSR}$              | $\Delta\overline{CTS}$   |
| 1  | 1  | 1  | SPR      | FF                     | bit 7                | bit 6              | bit 5                | bit 4   | bit 3                  | bit 2                         | bit 1                               | bit 0                    |
| <b>Special Register Set<sup>[3]</sup></b>  |    |    |          |                        |                      |                    |                      |   |                        |                               |                                     |                          |
| 0  | 0  | 0  | DLL      | XX                     | bit 7                | bit 6              | bit 5                | bit 4   | bit 3                  | bit 2                         | bit 1                               | bit 0                    |
| 0  | 0  | 1  | DLM      | XX                     | bit 15               | bit 14             | bit 13               | bit 12  | bit 11                 | bit 10                        | bit 9                               | bit 8                    |
| <b>Enhanced Register Set<sup>[4]</sup></b> |    |    |          |                        |                      |                    |                      |   |                        |                               |                                     |                          |
| 0  | 1  | 0  | EFR      | 00                     | Auto CTS             | Auto RTS           | Special char. select | Enable IER[4-7], ISR[4,5], FCR[4,5], MCR[5-7] | Cont-3 Tx, Rx Control  | Cont-2 Tx, Rx Control         | Cont-1 Tx, Rx Control               | Cont-0 Tx, Rx Control    |
| 1  | 0  | 0  | Xon-1    | 00                     | bit 7                | bit 6              | bit 5                | bit 4   | bit 3                  | bit 2                         | bit 1                               | bit 0                    |
| 1  | 0  | 1  | Xon-2    | 00                     | bit 15               | bit 14             | bit 13               | bit 12  | bit 11                 | bit 10                        | bit 9                               | bit 8                    |
| 1  | 1  | 0  | Xoff-1   | 00                     | bit 7                | bit 6              | bit 5                | bit 4   | bit 3                  | bit 2                         | bit 1                               | bit 0                    |
| 1  | 1  | 1  | Xoff-2   | 00                     | bit 15               | bit 14             | bit 13               | bit 12  | bit 11                 | bit 10                        | bit 9                               | bit 8                    |

[1] The value shown in represents the register's initialized HEX value; X = n/a.

[2] Accessible only when LCR[7] is logic 0.

[3] Baud rate registers accessible only when LCR[7] is logic 1.

[4] Enhanced Feature Register, Xon-1,2 and Xoff-1,2 are accessible only when LCR is set to 'BF<sub>Hex</sub>'.



## 7.1 Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the TSR and UART via the THR, providing that the THR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = at least one byte in FIFO/THR, logic 1 = FIFO/THR empty).

The serial receive section also contains an 8-bit Receive Holding Register (RHR) and a Receive Serial Shift Register (RSR). Receive data is removed from the SC16C2550 and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the  $16\times$  clock rate. After  $7\frac{1}{2}$  clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

## 7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INTA, INTB output pins.

**Table 8: Interrupt Enable Register bits description**

| Bit | Symbol | Description   |
|-----|--------|---|
| 7   | IER[7] | CTS interrupt.<br>Logic 0 = Disable the CTS interrupt (normal default condition).<br>Logic 1 = Enable the CTS interrupt. The SC16C2550 issues an interrupt when the CTS pin transitions from a logic 0 to a logic 1.  |
| 6   | IER[6] | RTS interrupt.<br>Logic 0 = Disable the RTS interrupt (normal default condition).<br>Logic 1 = Enable the RTS interrupt. The SC16C2550 issues an interrupt when the RTS pin transitions from a logic 0 to a logic 1.  |
| 5   | IER[5] | Xoff interrupt.<br>Logic 0 = Disable the software flow control, receive Xoff interrupt (normal default condition).<br>Logic 1 = Enable the software flow control, receive Xoff interrupt.   |
| 4   | IER[4] | Sleep mode.<br>Logic 0 = Disable sleep mode (normal default condition).<br>Logic 1 = Enable sleep mode.   |
| 3   | IER[3] | Modem Status Interrupt. This interrupt will be issued whenever there is a modem status change as reflected in MSR[0-3].<br>Logic 0 = Disable the modem status register interrupt (normal default condition).<br>Logic 1 = Enable the modem status register interrupt. |

**Table 8:** Interrupt Enable Register bits description...continued

| Bit | Symbol | Description  |
|-----|--------|--|
| 2   | IER[2] | <p>Receive Line Status interrupt. This interrupt will be issued whenever a receive data error condition exists as reflected in LSR[1-4].</p> <p>Logic 0 = Disable the receiver line status interrupt (normal default condition).</p> <p>Logic 1 = Enable the receiver line status interrupt.</p>   |
| 1   | IER[1] | <p>Transmit Holding Register interrupt. In the 16C450 mode, this interrupt will be issued whenever the THR is empty, and is associated with LSR[5]. In the FIFO modes, this interrupt will be issued whenever the FIFO is empty.</p> <p>Logic 0 = Disable the Transmit Holding Register Empty (TXRDY) interrupt (normal default condition).</p> <p>Logic 1 = Enable the TXRDY (ISR level 3) interrupt.</p>   |
| 0   | IER[0] | <p>Receive Holding Register. In the 16C450 mode, this interrupt will be issued when the RHR has data, or is cleared when the RHR is empty. In the FIFO mode, this interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level.</p> <p>Logic 0 = Disable the receiver ready (ISR level 2, RXRDY) interrupt (normal default condition).</p> <p>Logic 1 = Enable the RXRDY (ISR level 2) interrupt.</p> |

### 7.2.1 IER versus Transmit/Receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive RXRDY interrupt (Level 2 ISR interrupt) is issued to the external CPU when the receive FIFO has reached the programmed trigger level. It will be cleared when the receive FIFO drops below the programmed trigger level.
- Receive FIFO status will also be reflected in the user accessible ISR register when the receive FIFO trigger level is reached. Both the ISR register receive status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The receive data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register (RSR) to the receive FIFO. It is reset when the FIFO is empty.
- When the Transmit FIFO and interrupts are enabled, an interrupt is generated when the transmit FIFO is empty due to the unloading of the data by the TSR and UART for transmission via the transmission media. The interrupt is cleared either by reading the ISR register, or by loading the THR with new data characters.

### 7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[0-3] enables the SC16C2550 in the FIFO polled mode of operation. In this mode, interrupts are not generated and the user must poll the LSR register for TX and/or RX data status. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[1-4] will provide the type of receive errors, or a receive break, if encountered.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will show if any FIFO data errors occurred.

### 7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receive FIFO trigger levels, and select the DMA mode.

#### 7.3.1 DMA mode

**Mode 0 (FCR bit 3 = 0):** Set and enable the interrupt for each single transmit or receive operation, and is similar to the 16C450 mode. Transmit Ready ( $\overline{\text{TXRDY}}$ ) on PLCC44 and LQFP48 packages will go to a logic 0 whenever the FIFO (THR, if FIFO is not enabled) is empty. Receive Ready ( $\overline{\text{RXRDY}}$ ) on PLCC44 and LQFP48 packages will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.

**Mode 1 (FCR bit 3 = 1):** Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO is empty.  $\overline{\text{TXRDY}}$  on PLCC and LQFP48 packages remains a logic 0 as long as one empty FIFO location is available. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full.  $\overline{\text{RXRDY}}$  on PLCC44 and LQFP48 packages transitions LOW when the FIFO reaches the trigger level, and transitions HIGH when the FIFO empties.

## 7.3.2 FIFO mode

Table 9: FIFO Control Register bits description

| Bit | Symbol                              | Description  |
|-----|-------------------------------------|--|
| 7-6 | FCR[7]<br>(MSB),<br>FCR[6]<br>(LSB) | <p>RCVR trigger. These bits are used to set the trigger level for the receive FIFO interrupt.</p> <p>Logic 0 (or cleared) = normal default condition.</p> <p>Logic 1 = RX trigger level.</p> <p>An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to <a href="#">Table 10</a>.</p>   |
| 5-4 | FCR[5-4]                            | Not used; initialized to logic 0.  |
| 3   | FCR[3]                              | <p>DMA mode select.</p> <p>Logic 0 = Set DMA mode '0'</p> <p>Logic 1 = Set DMA mode '1'</p> <p><b>Transmit operation in mode '0':</b> When the SC16C2550 is in the 16C450 mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO or transmit holding register, the TXRDY pin in PLCC44 or LQFP48 packages will be a logic 0. Once active, the TXRDY pin will go to a logic 1 after the first character is loaded into the transmit holding register.</p> <p><b>Receive operation in mode '0':</b> When the SC16C2550 is in mode '0' (FCR[0] = logic 0), or in the FIFO mode (FCR[3] = logic 0) and there is at least one character in the receive FIFO, the RXRDY pin will be a logic 0. Once active, the RXRDY pin on PLCC44 and LQFP48 packages will go to a logic 1 when there are no more characters in the receiver.</p> <p><b>Transmit operation in mode '1':</b> When the SC16C2550 is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1), the TXRDY pin on PLCC44 and LQFP48 packages will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty.</p> <p><b>Receive operation in mode '1':</b> When the SC16C2550 is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1) and the trigger level has been reached, or a Receive Time-Out has occurred, the RXRDY pin on PLCC44 and LQFP48 packages will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.</p> |
| 2   | FCR[2]                              | <p>XMIT FIFO reset.</p> <p>Logic 0 = Transmit FIFO not reset (normal default condition).</p> <p>Logic 1 = Clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.</p>   |

Table 9: FIFO Control Register bits description...continued

| Bit | Symbol | Description  |
|-----|--------|--|
| 1   | FCR[1] | RCVR FIFO reset.<br>Logic 0 = Receive FIFO not reset (normal default condition).<br>Logic 1 = Clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO. |
| 0   | FCR[0] | FIFOs enabled.<br>Logic 0 = Disable the transmit and receive FIFO (normal default condition).<br>Logic 1 = Enable the transmit and receive FIFO. <b>This bit must be a '1' when other FCR bits are written to, or they will not be programmed.</b>   |

Table 10: RCVR trigger levels

| FCR[7] | FCR[6] | RX FIFO trigger level |
|--------|--------|-----------------------|
| 0      | 0      | 01                    |
| 0      | 1      | 04                    |
| 1      | 0      | 08                    |
| 1      | 1      | 14                    |

## 7.4 Interrupt Status Register (ISR)

The SC16C2550 provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. A lower level interrupt may be seen after servicing the higher level interrupt and re-reading the interrupt status bits. Table 11 "Interrupt source" shows the data values (bits 0-3) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 11: Interrupt source

| Priority level | ISR[5] | ISR[4] | ISR[3] | ISR[2] | ISR[1] | ISR[0] | Source of the interrupt                          |
|----------------|--------|--------|--------|--------|--------|--------|--|
| 1              | 0      | 0      | 0      | 1      | 1      | 0      | LSR (Receiver Line Status Register)              |
| 2              | 0      | 0      | 0      | 1      | 0      | 0      | RXRDY (Received Data Ready)                      |
| 2              | 0      | 0      | 1      | 1      | 0      | 0      | RXRDY (Receive Data time-out)                    |
| 3              | 0      | 0      | 0      | 0      | 1      | 0      | TXRDY (Transmitter Holding Register Empty)       |
| 4              | 0      | 0      | 0      | 0      | 0      | 0      | MSR (Modem Status Register)                      |
| 5              | 0      | 1      | 0      | 0      | 0      | 0      | RXRDY (Received Xoff signal) / Special character |
| 6              | 1      | 0      | 0      | 0      | 0      | 0      | CTS, RTS change of state                         |

**Table 12: Interrupt Status Register bits description**

| Bit | Symbol   | Description   |
|-----|----------|---|
| 7-6 | ISR[7-6] | FIFOs enabled. These bits are set to a logic 0 when the FIFOs are not being used in the 16C450 mode. They are set to a logic 1 when the FIFOs are enabled in the SC16C2550 mode.<br>Logic 0 or cleared = default condition.   |
| 5-4 | ISR[5-4] | INT priority bits 4-3. These bits are enabled when EFR[4] is set to a logic 1. ISR[4] indicates that matching Xoff character(s) have been detected. ISR[5] indicates that CTS, RTS have been generated. Note that once set to a logic 1, the ISR[4] bit will stay a logic 1 until Xon character(s) are received.<br>Logic 0 or cleared = default condition. |
| 3-1 | ISR[3-1] | INT priority bits 2-0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see <a href="#">Table 11</a> ).<br>Logic 0 or cleared = default condition.  |
| 0   | ISR[0]   | INT status.<br>Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.<br>Logic 1 = No interrupt pending (normal default condition).  |

## 7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

**Table 13: Line Control Register bits description**

| Bit | Symbol   | Description   |
|-----|----------|---|
| 7   | LCR[7]   | Divisor latch enable. The internal baud rate counter latch and Enhance Feature mode enable.<br>Logic 0 = Divisor latch disabled (normal default condition).<br>Logic 1 = Divisor latch enabled.   |
| 6   | LCR[6]   | Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0.<br>Logic 0 = no TX break condition (normal default condition)<br>Logic 1 = forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition. |
| 5-3 | LCR[5-3] | Programs the parity conditions (see <a href="#">Table 14</a> ).   |
| 2   | LCR[2]   | Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see <a href="#">Table 15</a> ).<br>Logic 0 or cleared = default condition.   |
| 1-0 | LCR[1-0] | Word length bits 1, 0. These two bits specify the word length to be transmitted or received (see <a href="#">Table 16</a> ).<br>Logic 0 or cleared = default condition.   |

Table 14: LCR[5-3] parity selection

| LCR[5] | LCR[4] | LCR[3] | Parity selection  |
|--------|--------|--------|-------------------|
| X      | X      | 0      | no parity         |
| X      | 0      | 1      | ODD parity        |
| 0      | 1      | 1      | EVEN parity       |
| 0      | 0      | 1      | forced parity '1' |
| 1      | 1      | 1      | forced parity '0' |

Table 15: LCR[2] stop bit length

| LCR[2] | Word length | Stop bit length (bit times) |
|--------|-------------|-----------------------------|
| 0      | 5, 6, 7, 8  | 1                           |
| 1      | 5           | 1- $\frac{1}{2}$            |
| 1      | 6, 7, 8     | 2                           |

Table 16: LCR[1-0] word length

| LCR[1] | LCR[0] | Word length |
|--------|--------|-------------|
| 0      | 0      | 5           |
| 0      | 1      | 6           |
| 1      | 0      | 7           |
| 1      | 1      | 8           |

## 7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

**Table 17: Modem Control Register bits description**

| Bit | Symbol | Description   |
|-----|--------|---|
| 7   | MCR[7] | Reserved; set to '0'.   |
| 6   | MCR[6] | IR enable.<br><br>Logic 0 = Enable the standard modem receive and transmit input/output interface (normal default condition).<br><br>Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. While in this mode, the TX/RX output/inputs are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode, the infrared TX output will be a logic 0 during idle data conditions.   |
| 5   | MCR[5] | Reserved; set to '0'.   |
| 4   | MCR[4] | Loop-back. Enable the local loop-back mode (diagnostics). In this mode the transmitter output (TX) and the receiver input (RX), CTS, DSR, CD, and RI are disconnected from the SC16C2550 I/O pins. Internally the modem data and control pins are connected into a loop-back data configuration (see <a href="#">Figure 6</a> ). In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register.<br><br>Logic 0 = Disable loop-back mode (normal default condition).<br>Logic 1 = Enable local loop-back mode (diagnostics). |
| 3   | MCR[3] | $\overline{\text{OP2}}$ /INT enable<br><br>Logic 0 = Forces INT (A-B) outputs to the 3-State mode and sets $\overline{\text{OP2}}$ to a logic 1 (normal default condition).<br><br>Logic 1 = Forces the INT (A-B outputs to the active mode and sets $\overline{\text{OP2}}$ to a logic 0.  |
| 2   | MCR[2] | ( $\overline{\text{OP1}}$ ). $\overline{\text{OP1A}}$ / $\overline{\text{OP1B}}$ are not available as an external signal in the SC16C2550. This bit is instead used in the Loop-back mode only. In the loop-back mode, this bit is used to write the state of the modem $\overline{\text{RI}}$ interface signal.  |
| 1   | MCR[1] | $\overline{\text{RTS}}$<br><br>Logic 0 = Force $\overline{\text{RTS}}$ output to a logic 1 (normal default condition).<br>Logic 1 = Force $\overline{\text{RTS}}$ output to a logic 0.  |
| 0   | MCR[0] | $\overline{\text{DTR}}$<br><br>Logic 0 = Force $\overline{\text{DTR}}$ output to a logic 1 (normal default condition).<br>Logic 1 = Force $\overline{\text{DTR}}$ output to a logic 0.  |



## 7.7 Line Status Register (LSR)

This register provides the status of data transfers between the SC16C2550 and the CPU.

**Table 18: Line Status Register bits description**

| Bit | Symbol | Description   |
|-----|--------|---|
| 7   | LSR[7] | FIFO data error.<br>Logic 0 = No error (normal default condition).<br>Logic 1 = At least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when there are no remaining error flags associated with the remaining data in the FIFO.   |
| 6   | LSR[6] | THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to '1' whenever the transmit FIFO and transmit shift register are both empty.   |
| 5   | LSR[5] | THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to a logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO. |
| 4   | LSR[4] | Break interrupt.<br>Logic 0 = No break condition (normal default condition).<br>Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.   |
| 3   | LSR[3] | Framing error.<br>Logic 0 = No framing error (normal default condition).<br>Logic 1 = Framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO.  |
| 2   | LSR[2] | Parity error.<br>Logic 0 = No parity error (normal default condition).<br>Logic 1 = Parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.  |

Table 18: Line Status Register bits description...continued

| Bit | Symbol | Description  |
|-----|--------|--|
| 1   | LSR[1] | <p>Overrun error.</p> <p>Logic 0 = No overrun error (normal default condition).</p> <p>Logic 1 = Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.</p> |
| 0   | LSR[0] | <p>Receive data ready.</p> <p>Logic 0 = No data in receive holding register or FIFO (normal default condition).</p> <p>Logic 1 = Data has been received and is saved in the receive holding register or FIFO.</p>  |

## 7.8 Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device to which the SC16C2550 is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

Table 19: Modem Status Register bits description

| Bit | Symbol | Description   |
|-----|--------|---|
| 7   | MSR[7] | <p>CD. During normal operation, this bit is the complement of the <math>\overline{CD}</math> input. Reading this bit in the loop-back mode produces the state of MCR[3] (<math>\overline{OP2}</math>).</p>  |
| 6   | MSR[6] | <p>RI. During normal operation, this bit is the complement of the <math>\overline{RI}</math> input. Reading this bit in the loop-back mode produces the state of MCR[2] (<math>OP1</math>).</p>   |
| 5   | MSR[5] | <p>DSR. During normal operation, this bit is the complement of the <math>\overline{DSR}</math> input. During the loop-back mode, this bit is equivalent to MCR[0] (<math>\overline{DTR}</math>).</p>  |
| 4   | MSR[4] | <p>CTS. During normal operation, this bit is the complement of the <math>\overline{CTS}</math> input. During the loop-back mode, this bit is equivalent to MCR[1] (<math>\overline{RTS}</math>).</p>  |
| 3   | MSR[3] | <p><math>\Delta\overline{CD}</math> [1]</p> <p>Logic 0 = No <math>\overline{CD}</math> change (normal default condition).</p> <p>Logic 1 = The <math>\overline{CD}</math> input to the SC16C2550 has changed state since the last time it was read. A modem Status Interrupt will be generated.</p> |
| 2   | MSR[2] | <p><math>\Delta\overline{RI}</math> [1]</p> <p>Logic 0 = No <math>\overline{RI}</math> change (normal default condition).</p> <p>Logic 1 = The <math>\overline{RI}</math> input to the SC16C2550 has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.</p>           |

Table 19: Modem Status Register bits description...continued

| Bit | Symbol | Description   |
|-----|--------|---|
| 1   | MSR[1] | $\Delta\overline{\text{DSR}}$ [1]<br>Logic 0 = No $\overline{\text{DSR}}$ change (normal default condition).<br>Logic 1 = The $\overline{\text{DSR}}$ input to the SC16C2550 has changed state since the last time it was read. A modem Status Interrupt will be generated. |
| 0   | MSR[0] | $\Delta\overline{\text{CTS}}$ [1]<br>Logic 0 = No $\overline{\text{CTS}}$ change (normal default condition).<br>Logic 1 = The $\overline{\text{CTS}}$ input to the SC16C2550 has changed state since the last time it was read. A modem Status Interrupt will be generated. |

[1] Whenever any MSR bit 0-3 is set to logic 1, a Modem Status Interrupt will be generated.

## 7.9 Scratchpad Register (SPR)

The SC16C2550 provides a temporary data register to store 8 bits of user information.

## 7.10 Enhanced Feature Register (EFR)

Enhanced features are enabled or disabled using this register.

Bits 0 through 4 provide single or dual character software flow control selection. When the Xon1 and Xon2 and/or Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential numbers.

Table 20: Enhanced Feature Register bits description

| Bit | Symbol | Description   |
|-----|--------|---|
| 7   | EFR[7] | Automatic CTS flow control.<br>Logic 0 = Automatic CTS flow control is disabled (normal default condition).<br>Logic 1 = Enable Automatic CTS flow control. Transmission will stop when CTS goes to a logical 1. Transmission will resume when the CTS pin returns to a logical 0.  |
| 6   | EFR[6] | Automatic RTS flow control. Automatic RTS may be used for hardware flow control by enabling EFR[6]. When Auto-RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and $\overline{\text{RTS}}$ will go to a logic 1 at the next trigger level. $\overline{\text{RTS}}$ will return to a logic 0 when data is unloaded below the next lower trigger level (programmed trigger level 1). The state of this register bit changes with the status of the hardware flow control. $\overline{\text{RTS}}$ functions normally when hardware flow control is disabled.<br>0 = Automatic RTS flow control is disabled (normal default condition).<br>1 = Enable Automatic RTS flow control. |

Table 20: Enhanced Feature Register bits description...continued

| Bit | Symbol   | Description   |
|-----|----------|---|
| 5   | EFR[5]   | <p>Special Character Detect.</p> <p>Logic 0 = Special character detect disabled (normal default condition).<br/>           Logic 1 = Special character detect enabled. The SC16C2550 compares each incoming receive character with Xoff2 data. If a match exists, the received data will be transferred to FIFO and ISR[4] will be set to indicate detection of special character. Bit-0 in the X-registers corresponds with the LSB bit for the receive character. When this feature is enabled, the normal software flow control must be disabled (EFR[3-0] must be set to a logic 0).</p>  |
| 4   | EFR[4]   | <p>Enhanced function control bit. The content of IER[7-4], ISR[5-4], FCR[5-4], and MCR[7-5] can be modified and latched. After modifying any bits in the enhanced registers, EFR[4] can be set to a logic 0 to latch the new values. This feature prevents existing software from altering or overwriting the SC16C2550 enhanced functions.</p> <p>Logic 0 = disable/latch enhanced features. IER[7-4], ISR[5-4], FCR[5-4], and MCR[7-5] are saved to retain the user settings, then IER[7-4] ISR[5-4], FCR[5-4], and MCR[7-5] are set to a logic 0 to be compatible with SC16C554 mode. (Normal default condition.)</p> <p>Logic 1 = Enables the enhanced functions. When this bit is set to a logic 1, all enhanced features of the SC16C2550 are enabled and user settings stored during a reset will be restored.</p> |
| 3-0 | EFR[3-0] | <p>Cont-3-0 Tx, Rx control. Logic 0 or cleared is the default condition. Combinations of software flow control can be selected by programming these bits. See Table 21.</p>   |

Table 21: Software flow control functions<sup>[1]</sup>

| Cont-3 | Cont-2 | Cont-1 | Cont-0 | TX, RX software flow controls   |
|--------|--------|--------|--------|---|
| 0      | 0      | X      | X      | No transmit flow control  |
| 1      | 0      | X      | X      | Transmit Xon1/Xoff1   |
| 0      | 1      | X      | X      | Transmit Xon2/Xoff2   |
| 1      | 1      | X      | X      | Transmit Xon1 and Xon2/Xoff1 and Xoff2  |
| X      | X      | 0      | 0      | No receive flow control   |
| X      | X      | 1      | 0      | Receiver compares Xon1/Xoff1  |
| X      | X      | 0      | 1      | Receiver compares Xon2/Xoff2  |
| 1      | 0      | 1      | 1      | Transmit Xon1/Xoff1<br>Receiver compares Xon1 and Xon2, Xoff1 and Xoff2                   |
| 0      | 1      | 1      | 1      | Transmit Xon2/Xoff2<br>Receiver compares Xon1 and Xon2/Xoff1 and Xoff2                    |
| 1      | 1      | 1      | 1      | Transmit Xon1 and Xon2/Xoff1 and Xoff2<br>Receiver compares Xon1 and Xon2/Xoff1 and Xoff2 |

[1] When using a software flow control the Xon/Xoff characters cannot be used for data transfer.

## 7.11 SC16C2550 external reset condition

Table 22: Reset state for registers

| Register | Reset state                            |
|----------|--|
| IER      | IER[7-0] = 0                           |
| FCR      | FCR[7-0] = 0                           |
| ISR      | ISR[7-1] = 0; ISR[0] = 1               |
| LCR      | LCR[7-0] = 0                           |
| MCR      | MCR[7-0] = 0                           |
| LSR      | LSR[7] = 0; LSR[6-5] = 1; LSR[4-0] = 0 |
| MSR      | MSR[7-4] = input signals; MSR[3-0] = 0 |
| SPR      | SFR[7-0] = 1                           |
| DLL      | DLL[7-0] = X                           |
| DLM      | DLM[7-0] = X                           |

Table 23: Reset state for outputs

| Output     | Reset state       |
|------------|-------------------|
| TXA, TXB   | Logic 1           |
| OP2A, OP2B | Logic 1           |
| RTSA, RTSB | Logic 1           |
| DTRA, DTRB | Logic 1           |
| INTA, INTB | 3-State condition |

## 8. Limiting values

Table 24: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol          | Parameter                           | Conditions | Min       | Max            | Unit |
|-----------------|-------------------------------------|------------|-----------|----------------|------|
| $V_{CC}$        | supply voltage                      |            | -         | 7              | V    |
| $V_n$           | voltage at any pin                  |            | GND - 0.3 | $V_{CC} + 0.3$ | V    |
| $T_{amb}$       | operating temperature               |            | -40       | +85            | °C   |
| $T_{stg}$       | storage temperature                 |            | -65       | +150           | °C   |
| $P_{tot(pack)}$ | total power dissipation per package |            | -         | 500            | mW   |

## 9. Static characteristics

**Table 25: DC electrical characteristics**

$T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{CC} = 2.5\text{ V}$ ,  $3.3\text{ V}$  or  $5.0\text{ V} \pm 10\%$ , unless otherwise specified.

| Symbol       | Parameter   | Conditions  | 2.5 V |          | 3.3 V |          | 5.0 V |          | Unit          |
|--------------|---|---|-------|----------|-------|----------|-------|----------|---------------|
|              |   |   | Min   | Max      | Min   | Max      | Min   | Max      |               |
| $V_{IL(CK)}$ | LOW-level clock input voltage                             |   | -0.3  | 0.45     | -0.3  | 0.6      | -0.5  | 0.6      | V             |
| $V_{IH(CK)}$ | HIGH-level clock input voltage                            |   | 1.8   | $V_{CC}$ | 2.4   | $V_{CC}$ | 3.0   | $V_{CC}$ | V             |
| $V_{IL}$     | LOW-level input voltage<br>(except X1 clock)              |   | -0.3  | 0.65     | -0.3  | 0.8      | -0.5  | 0.8      | V             |
| $V_{IH}$     | HIGH-level input voltage<br>(except X1 clock)             |   | 1.6   | -        | 2.0   | -        | 2.2   | -        | V             |
| $V_{OL}$     | LOW-level output voltage<br>on all outputs <sup>[1]</sup> | $I_{OL} = 5\text{ mA}$<br>(databus)                   | -     | -        | -     | -        | -     | 0.4      | V             |
|              |   | $I_{OL} = 4\text{ mA}$<br>(other outputs)             | -     | -        | -     | 0.4      | -     | -        | V             |
|              |   | $I_{OL} = 2\text{ mA}$<br>(databus)                   | -     | 0.4      | -     | -        | -     | -        | V             |
|              |   | $I_{OL} = 1.6\text{ mA}$<br>(other outputs)           | -     | 0.4      | -     | -        | -     | -        | V             |
| $V_{OH}$     | HIGH-level output voltage                                 | $I_{OH} = -5\text{ mA}$<br>(databus)                  | -     | -        | -     | -        | 2.4   | -        | V             |
|              |   | $I_{OH} = -1\text{ mA}$<br>(other outputs)            | -     | -        | 2.0   | -        | -     | -        | V             |
|              |   | $I_{OH} = -800\text{ }\mu\text{A}$<br>(data bus)      | 1.85  | -        | -     | -        | -     | -        | V             |
|              |   | $I_{OH} = -400\text{ }\mu\text{A}$<br>(other outputs) | 1.85  | -        | -     | -        | -     | -        | V             |
| $I_{LIL}$    | LOW-level input leakage<br>current                        |   | -     | $\pm 10$ | -     | $\pm 10$ | -     | $\pm 10$ | $\mu\text{A}$ |
| $I_{CL}$     | clock leakage   |   | -     | $\pm 30$ | -     | $\pm 30$ | -     | $\pm 30$ | $\mu\text{A}$ |
| $I_{CC}$     | supply current  | $f = 5\text{ MHz}$                                    | -     | 3.5      | -     | 4.5      | -     | 4.5      | mA            |
| $C_i$        | input capacitance   |   | -     | 5        | -     | 5        | -     | 5        | pF            |

[1] Except  $x_2$ ,  $V_{OL} = 1\text{ V}$  typical.

## 10. Dynamic characteristics

Table 26: AC electrical characteristics

$T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{CC} = 2.5\text{ V}$ ,  $3.3\text{ V}$  or  $5.0\text{ V} \pm 10\%$ , unless otherwise specified.

| Symbol              | Parameter   | Conditions | 2.5 V |              | 3.3 V |              | 5.0 V |              | Unit      |
|---------------------|---|------------|-------|--------------|-------|--------------|-------|--------------|-----------|
|                     |   |            | Min   | Max          | Min   | Max          | Min   | Max          |           |
| $t_{1w}$ , $t_{2w}$ | clock pulse duration  |            | 10    | -            | 6     | -            | 6     | -            | ns        |
| $t_{3w}$            | oscillator/clock frequency  | [1]        | -     | 48           | -     | 80           | -     | 80           | MHz       |
| $t_{6s}$            | address set-up time   |            | 0     | -            | 0     | -            | 0     | -            | ns        |
| $t_{6h}$            | address hold time   |            | 0     | -            | 0     | -            | 0     | -            | ns        |
| $t_{7d}$            | $\overline{\text{IOR}}$ delay from chip select                        |            | 10    | -            | 10    | -            | 10    | -            | ns        |
| $t_{7w}$            | $\overline{\text{IOR}}$ strobe width                                  | 25 pF load | 77    | -            | 26    | -            | 23    | -            | ns        |
| $t_{7h}$            | chip select hold time from $\overline{\text{IOR}}$                    |            | 0     | -            | 0     | -            | 0     | -            | ns        |
| $t_{9d}$            | read cycle delay  | 25 pF load | 20    | -            | 20    | -            | 20    | -            | ns        |
| $t_{12d}$           | delay from $\overline{\text{IOR}}$ to data                            | 25 pF load | -     | 77           | -     | 26           | -     | 23           | ns        |
| $t_{12h}$           | data disable time   | 25 pF load | -     | 15           | -     | 15           | -     | 15           | ns        |
| $t_{13d}$           | $\overline{\text{IOW}}$ delay from chip select                        |            | 10    | -            | 10    | -            | 10    | -            | ns        |
| $t_{13w}$           | $\overline{\text{IOW}}$ strobe width                                  |            | 20    | -[2]         | 20    | -[2]         | 15    | -[2]         | ns        |
| $t_{13h}$           | chip select hold time from $\overline{\text{IOW}}$                    |            | 0     | -            | 0     | -            | 0     | -            | ns        |
| $t_{15d}$           | write cycle delay   | [3]        | 25    | -            | 25    | -            | 20    | -            | ns        |
| $t_{16s}$           | data set-up time  |            | 20    | -            | 20    | -            | 15    | -            | ns        |
| $t_{16h}$           | data hold time  |            | 15    | -            | 5     | -            | 5     | -            | ns        |
| $t_{17d}$           | delay from $\overline{\text{IOW}}$ to output                          | 25 pF load | -     | 100          | -     | 33           | -     | 29           | ns        |
| $t_{18d}$           | delay to set interrupt from Modem input                               | 25 pF load | -     | 100          | -     | 24           | -     | 23           | ns        |
| $t_{19d}$           | delay to reset interrupt from $\overline{\text{IOR}}$                 | 25 pF load | -     | 100          | -     | 24           | -     | 23           | ns        |
| $t_{20d}$           | delay from stop to set interrupt                                      |            | -     | 1            | -     | 1            | -     | 1            | $R_{clk}$ |
| $t_{21d}$           | delay from $\overline{\text{IOR}}$ to reset interrupt                 | 25 pF load | -     | 100          | -     | 29           | -     | 28           | ns        |
| $t_{22d}$           | delay from start to set interrupt                                     |            | -     | 100          | -     | 45           | -     | 40           | ns        |
| $t_{23d}$           | delay from $\overline{\text{IOW}}$ to transmit start                  |            | 8     | 24           | 8     | 24           | 8     | 24           | $R_{clk}$ |
| $t_{24d}$           | delay from $\overline{\text{IOW}}$ to reset interrupt                 |            | -     | 100          | -     | 45           | -     | 40           | ns        |
| $t_{25d}$           | delay from stop to set $\overline{\text{RXRDY}}$                      |            | -     | 1            | -     | 1            | -     | 1            | $R_{clk}$ |
| $t_{26d}$           | delay from $\overline{\text{IOR}}$ to reset $\overline{\text{RXRDY}}$ |            | -     | 100          | -     | 45           | -     | 40           | ns        |
| $t_{27d}$           | delay from $\overline{\text{IOW}}$ to set $\overline{\text{TXRDY}}$   |            | -     | 100          | -     | 45           | -     | 40           | ns        |
| $t_{28d}$           | delay from start to reset $\overline{\text{TXRDY}}$                   |            | -     | 8            | -     | 8            | -     | 8            | $R_{clk}$ |
| $t_{\text{RESET}}$  | Reset pulse width   |            | 200   | -            | 40    | -            | 40    | -            | ns        |
| N                   | baud rate divisor   |            | 1     | $2^{16} - 1$ | 1     | $2^{16} - 1$ | 1     | $2^{16} - 1$ | $R_{clk}$ |

[1] Applies to external clock, crystal oscillator max 24 MHz.

$$[2] \quad \overline{\text{IOW}}\text{strobe}_{max} = \frac{1}{2(\text{Baudrate}_{max})}$$

= 333 ns (for  $\text{Baudrate}_{max} = 1.5\text{ Mbits/s}$ )

= 1  $\mu\text{s}$  (for  $\text{Baudrate}_{max} = 460.8\text{ kbits/s}$ )

= 4  $\mu\text{s}$  (for  $\text{Baudrate}_{max} = 115.2\text{ kbits/s}$ )

[3] When in **both** DMA mode 0 **and** FIFO enable mode, the write cycle delay should be larger than one  $x_1$ , clock cycle.

10.1 Timing diagrams

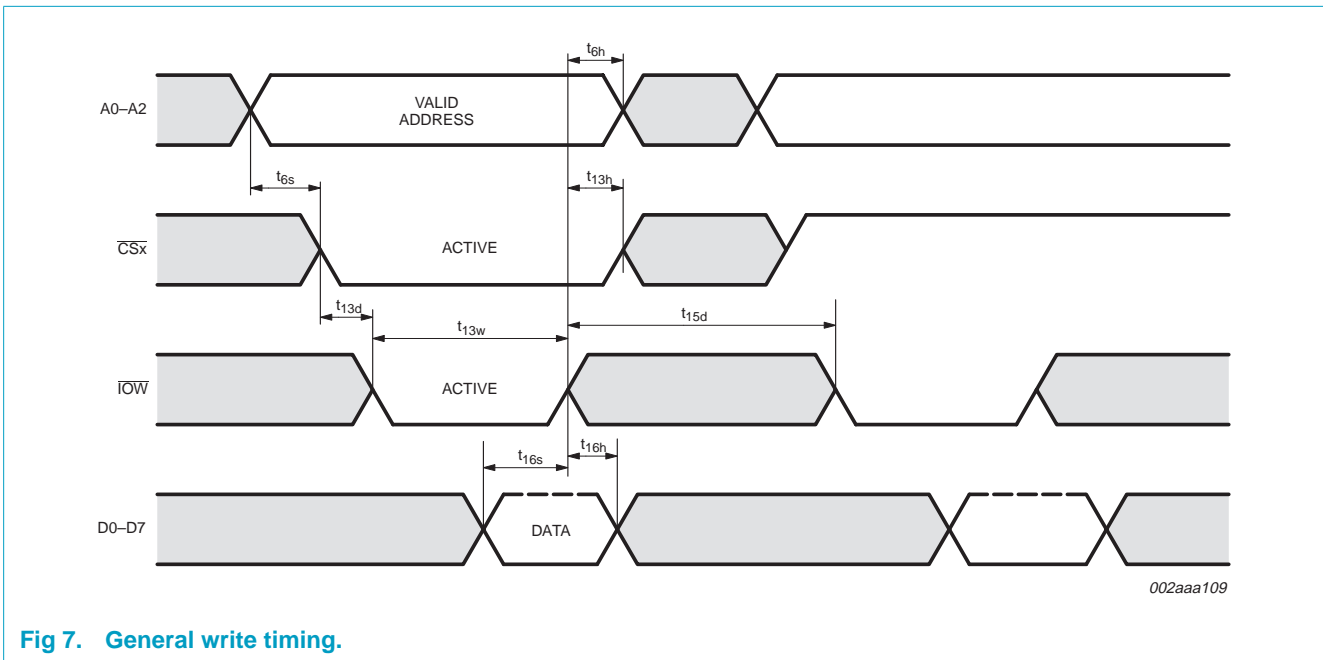


Fig 7. General write timing.

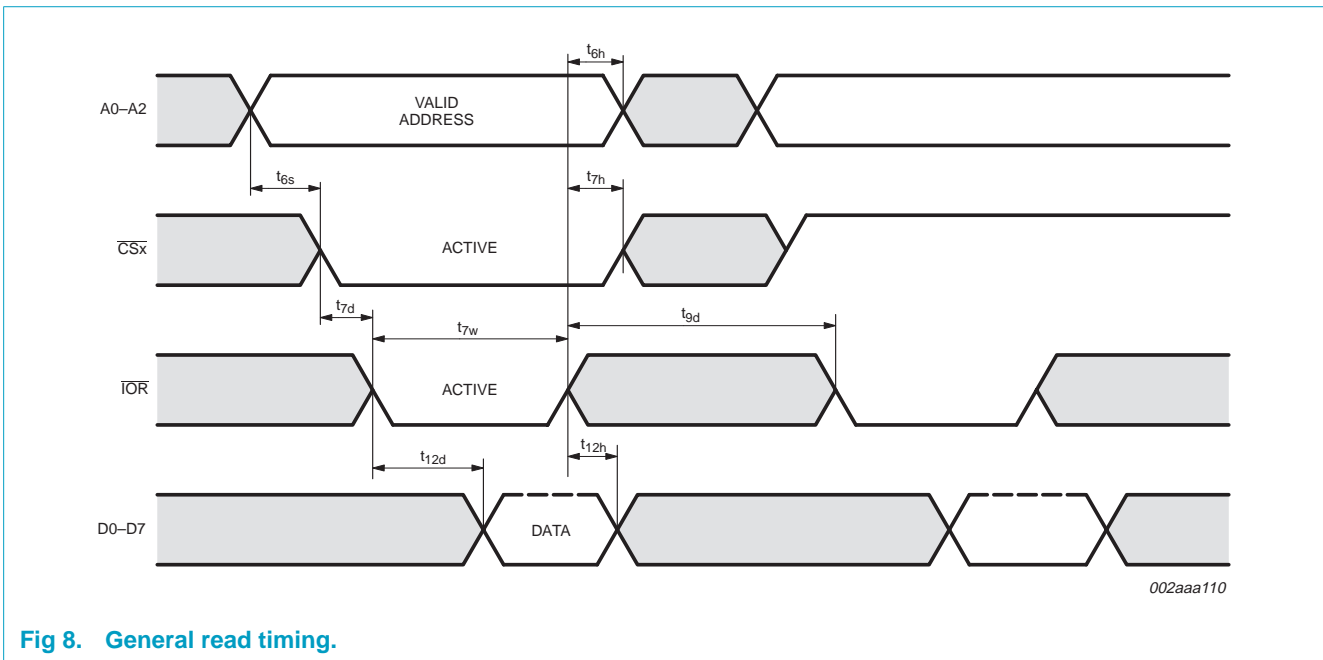
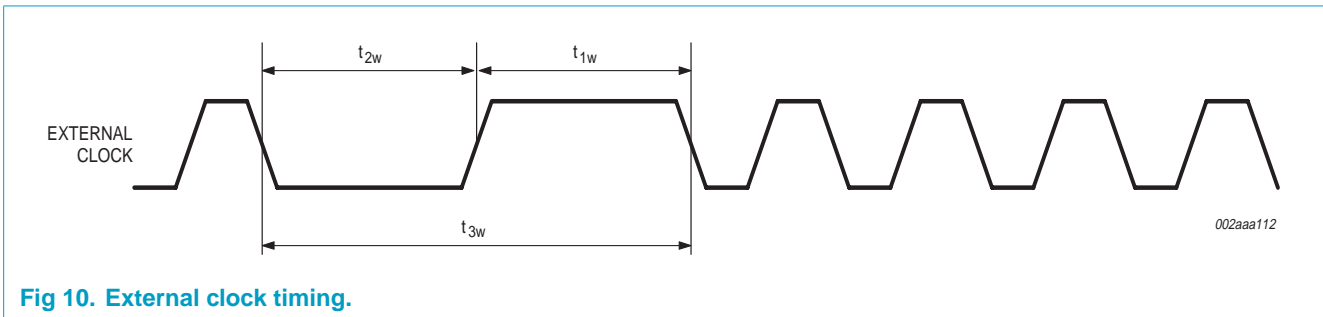
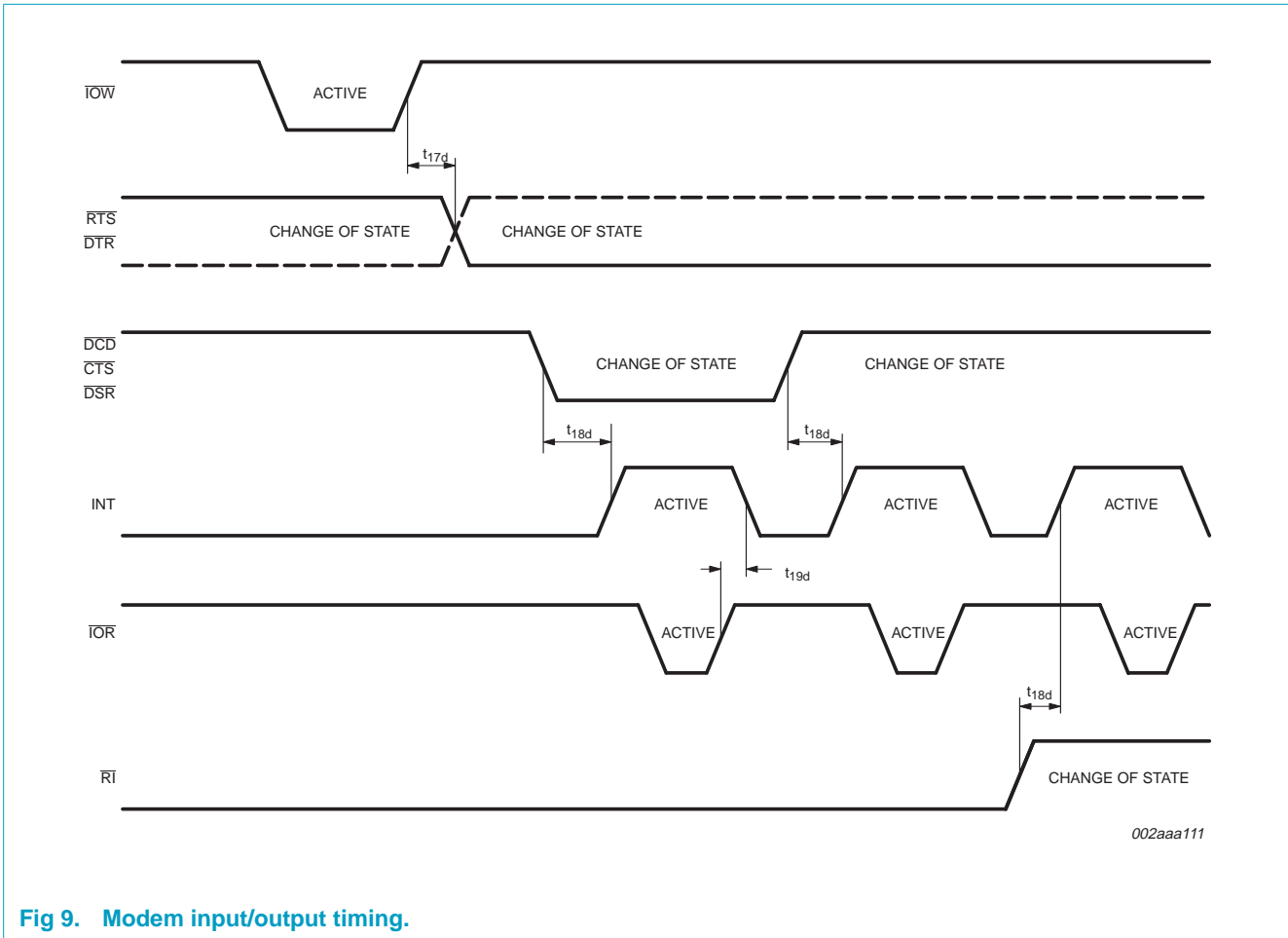


Fig 8. General read timing.





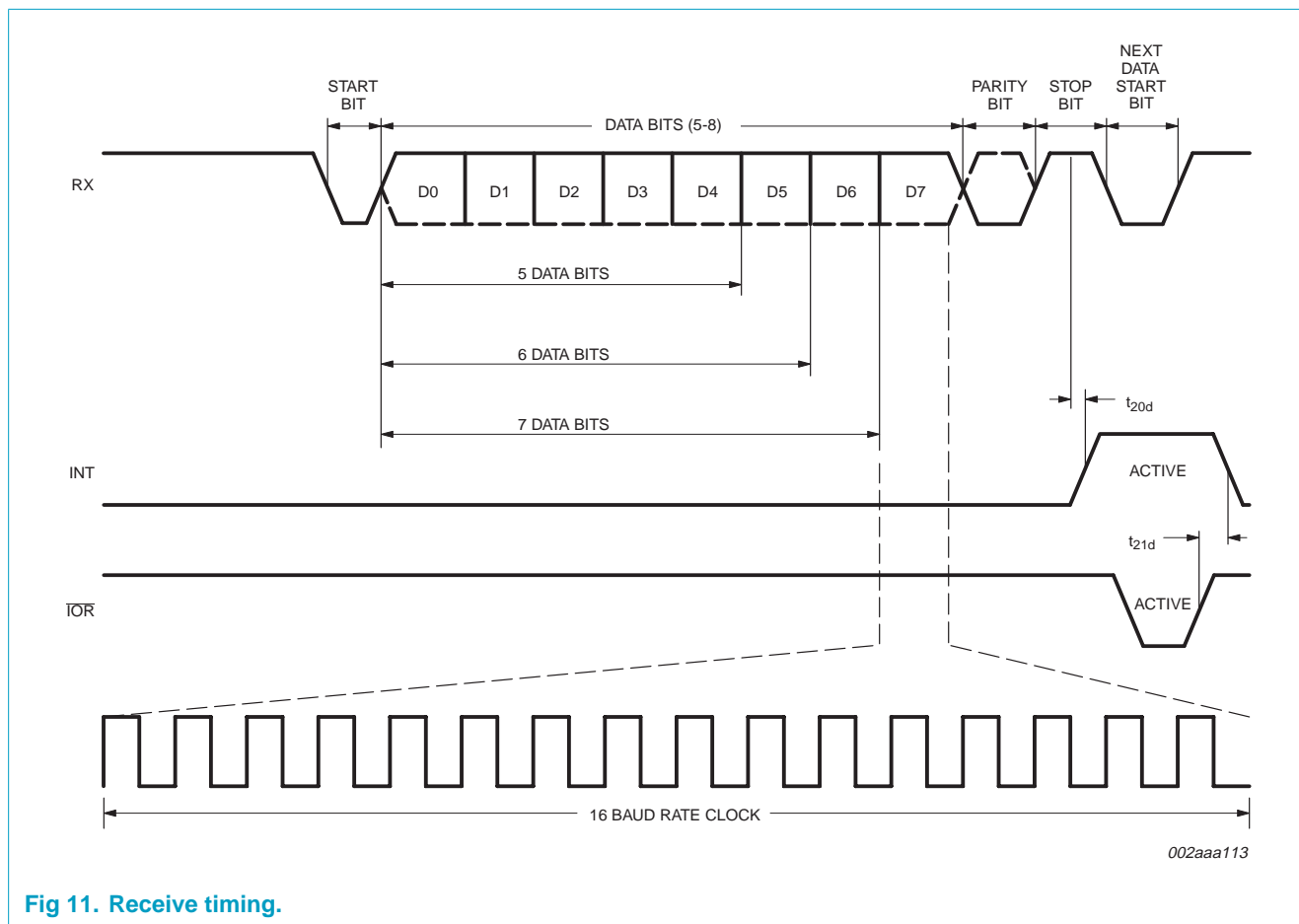


Fig 11. Receive timing.

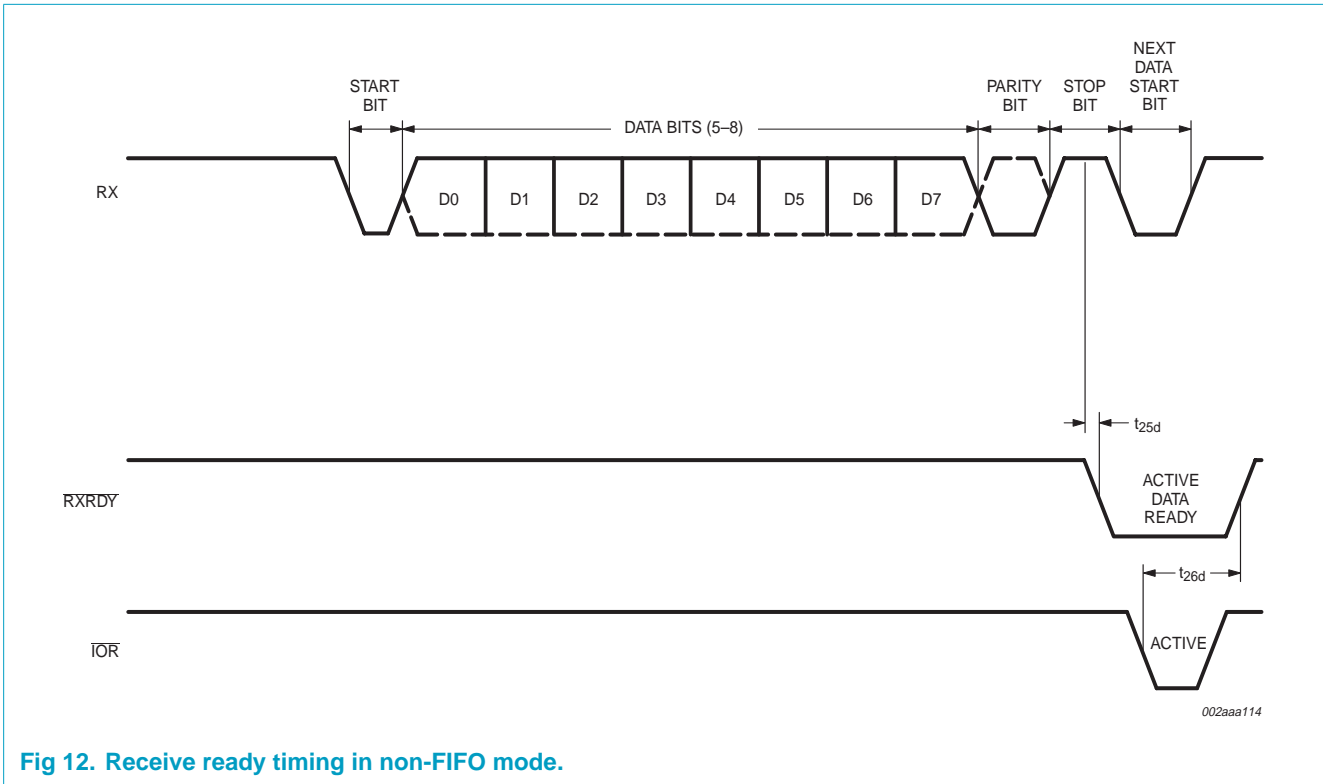


Fig 12. Receive ready timing in non-FIFO mode.

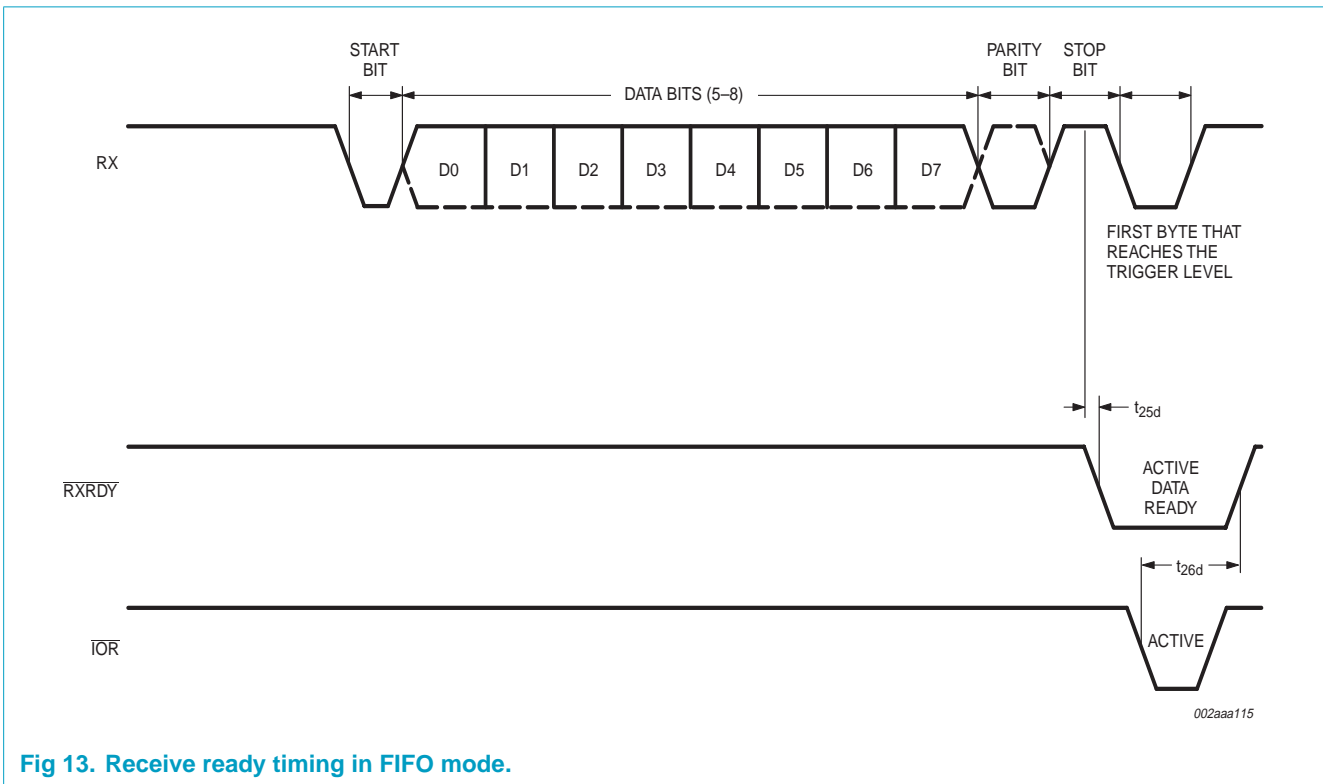


Fig 13. Receive ready timing in FIFO mode.

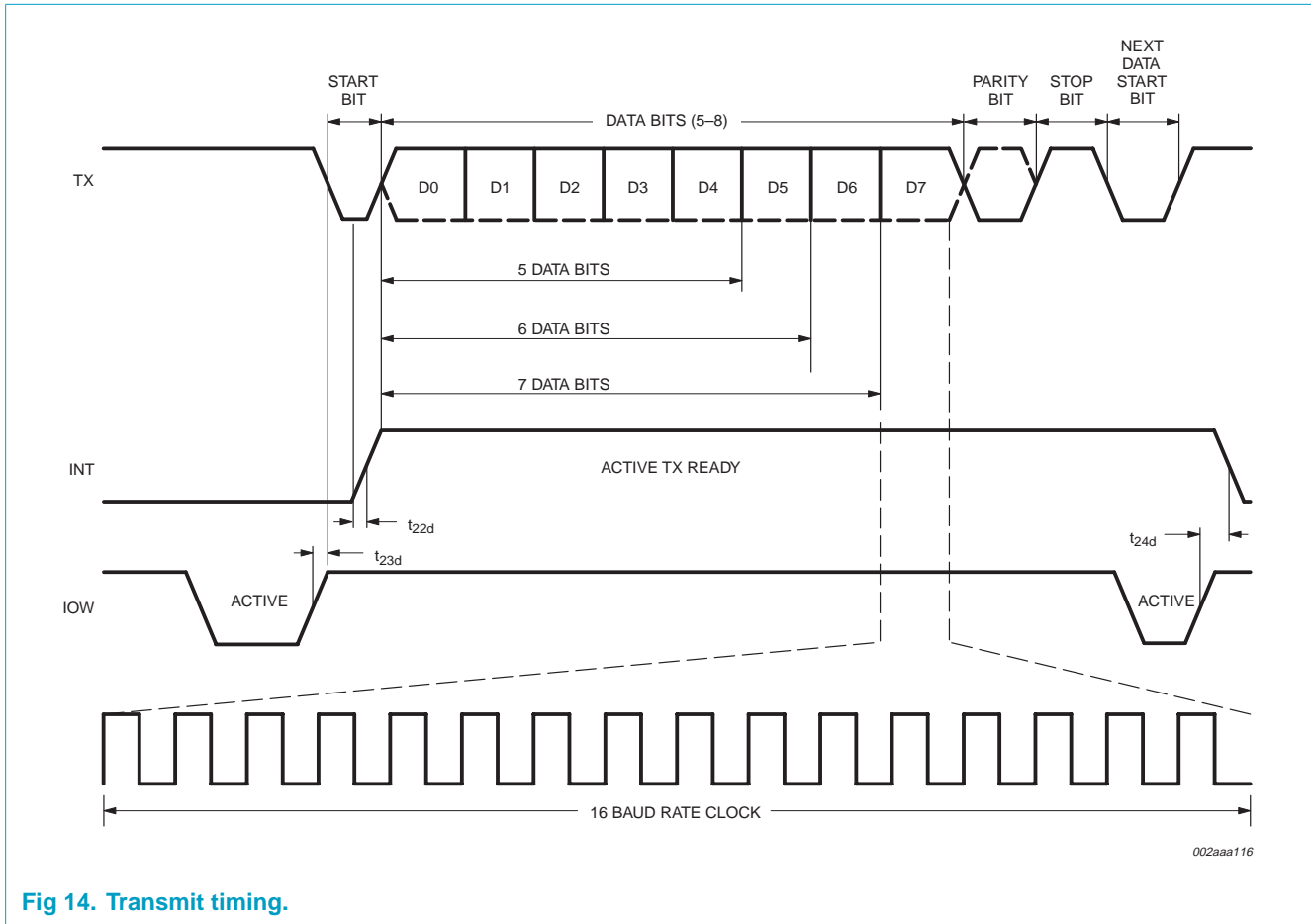


Fig 14. Transmit timing.

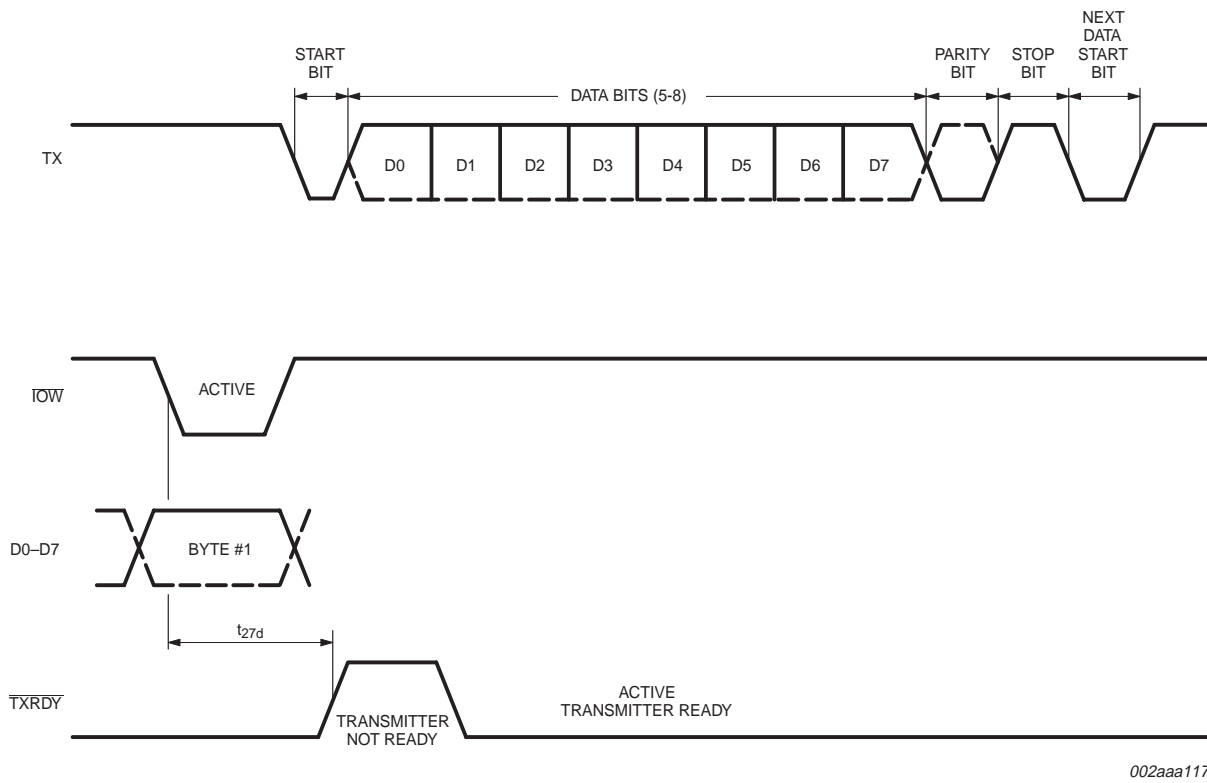


Fig 15. Transmit ready timing in non-FIFO mode.

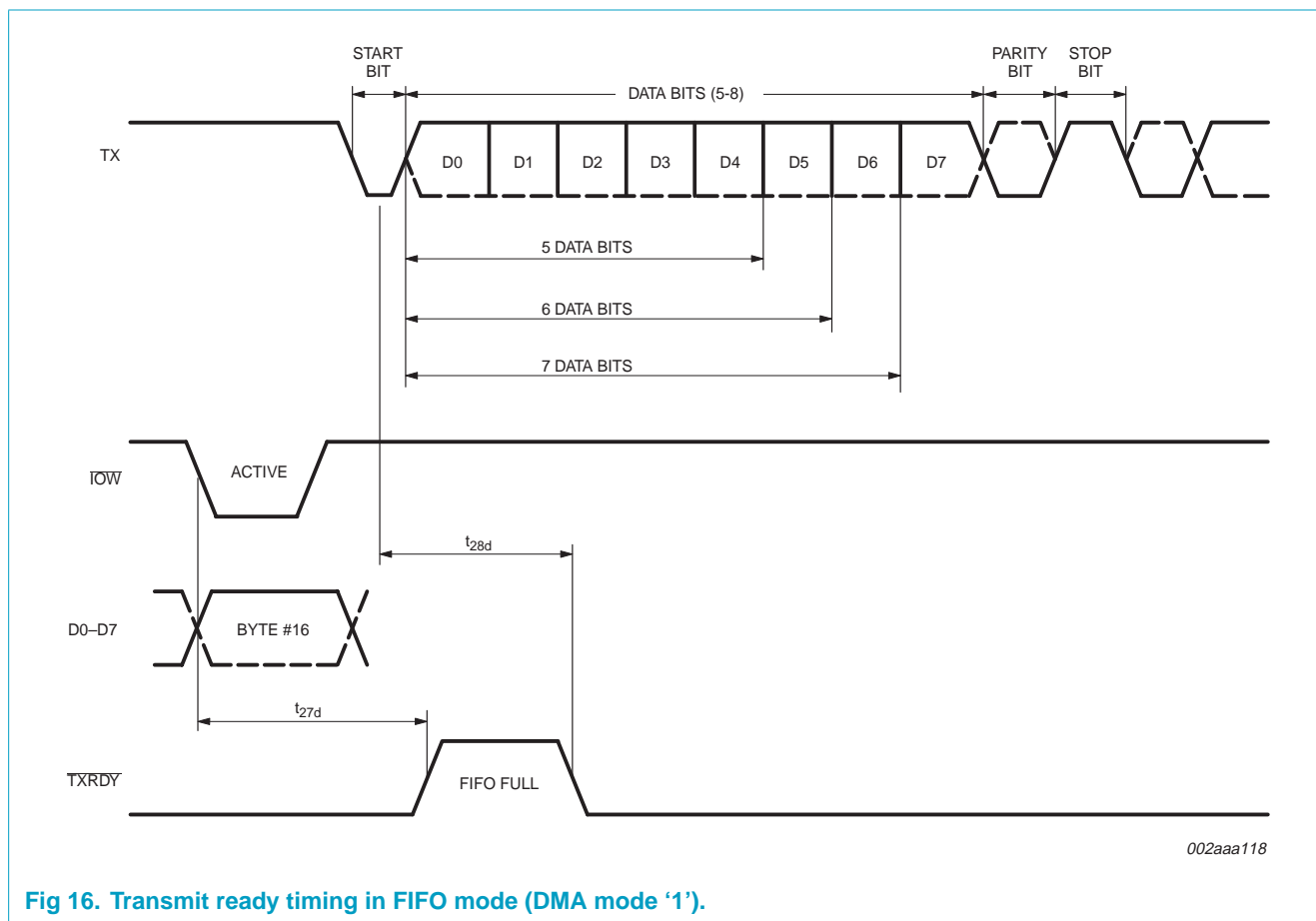


Fig 16. Transmit ready timing in FIFO mode (DMA mode '1').

11. Package outline

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1

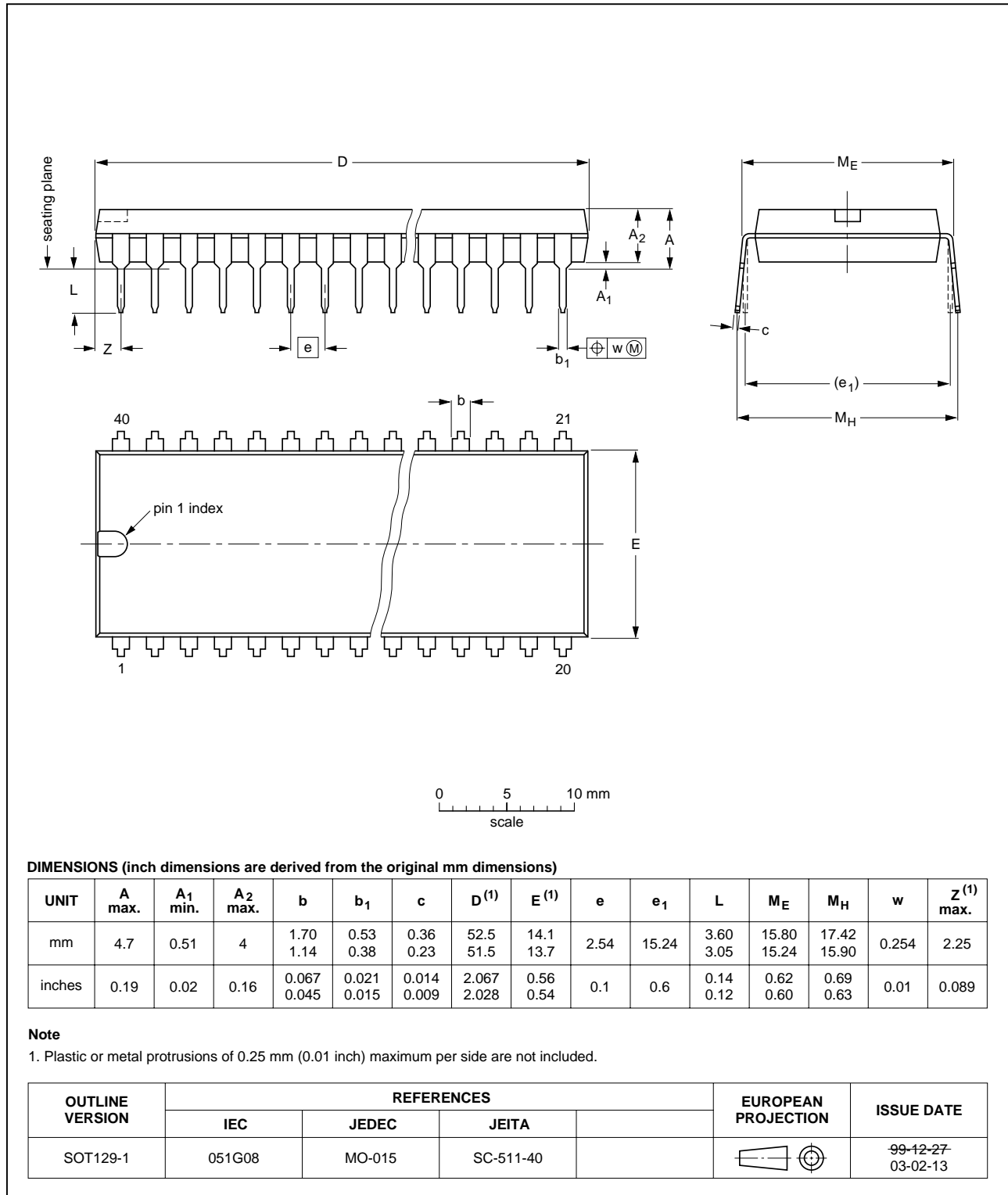


Fig 17. DIP40 package outline (SOT129-1).

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2

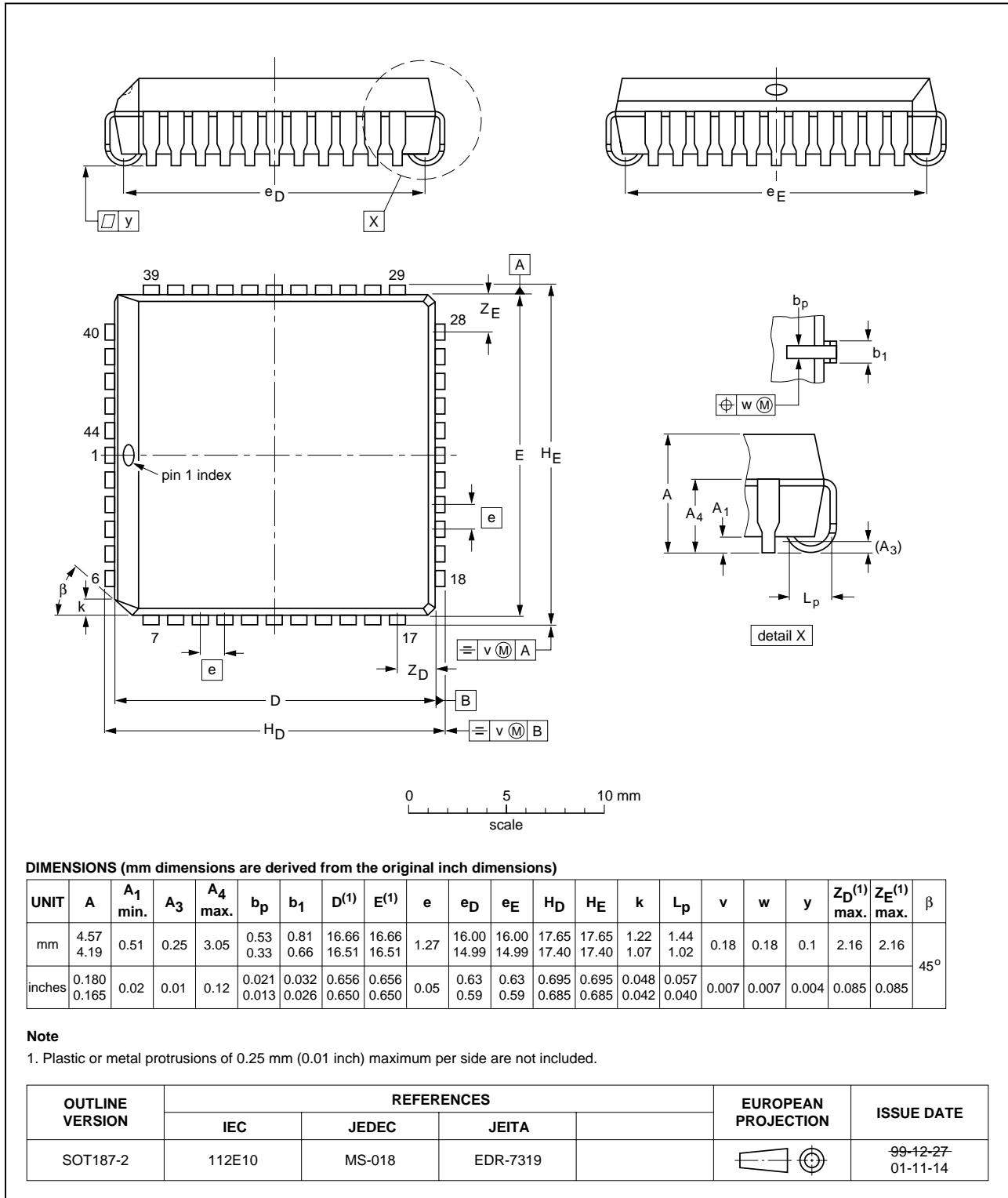


Fig 18. PLCC44 package outline (SOT187-2).



LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2

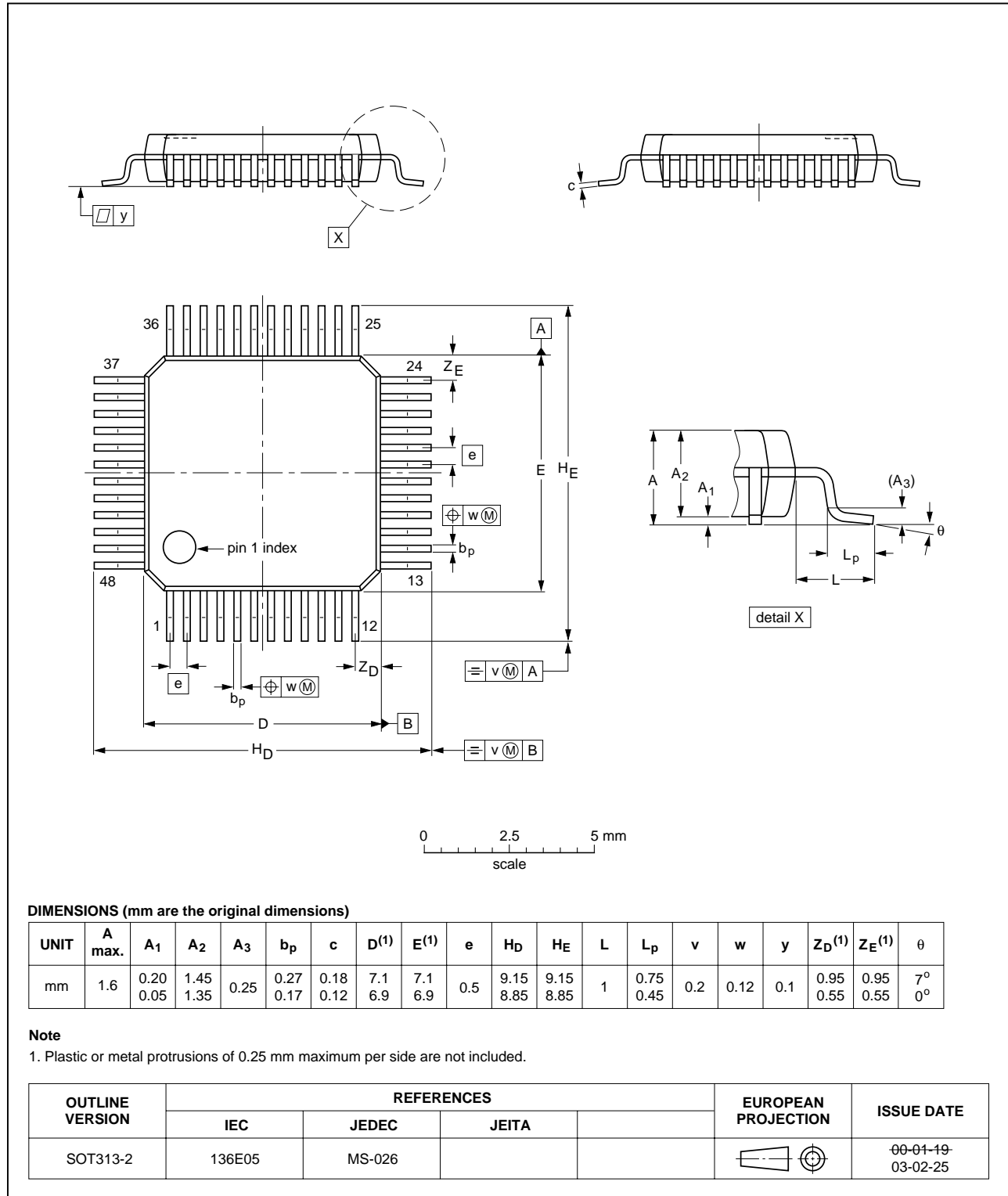


Fig 19. LQFP48 package outline (SOT313-2).

## 12. Soldering

### 12.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

### 12.2 Through-hole mount packages

#### 12.2.1 Soldering by dipping or by solder wave

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### 12.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### 12.3 Surface mount packages

#### 12.3.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA and SSOP-T packages

- for packages with a thickness  $\geq 2.5$  mm
- for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

### 12.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 12.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 12.4 Package related soldering information

Table 27: Suitability of IC packages for wave, reflow and dipping soldering methods

| Mounting           | Package <sup>[1]</sup>   | Soldering method                  |                       |          |
|--------------------|--|-----------------------------------|-----------------------|----------|
|                    |  | Wave                              | Reflow <sup>[2]</sup> | Dipping  |
| Through-hole mount | DBS, DIP, HDIP, SDIP, SIL  | suitable <sup>[3]</sup>           | –                     | suitable |
| Surface mount      | BGA, LBGA, LFBGA, SQFP, SSOP-T <sup>[4]</sup> , TFBGA, VFBGA             | not suitable                      | suitable              | –        |
|                    | DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable <sup>[5]</sup>       | suitable              | –        |
|                    | PLCC <sup>[6]</sup> , SO, SOJ  | suitable                          | suitable              | –        |
|                    | LQFP, QFP, TQFP  | not recommended <sup>[6][7]</sup> | suitable              | –        |
|                    | SSOP, TSSOP, VSO, VSSOP  | not recommended <sup>[8]</sup>    | suitable              | –        |

- [1] For more detailed information on the BGA packages refer to the *(LFBGA) Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.
- [2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.
- [3] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
- [4] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding  $217 \text{ }^\circ\text{C} \pm 10 \text{ }^\circ\text{C}$  measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [5] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [6] If wave soldering is considered, then the package must be placed at a  $45^\circ$  angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [7] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [8] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## 13. Revision history

Table 28: Revision history

| Rev | Date     | CPCN | Description   |
|-----|----------|------|---|
| 03  | 20030619 | -    | <b>Product data (9397 750 11621). ECN 853-2368 30033 of 16 June 2003.</b><br>Modifications:<br><ul style="list-style-type: none"> <li>Figure 5 "Crystal oscillator connection." on page 13: changed capacitors' values and added connection with resistor.</li> </ul> |
| 02  | 20030314 | -    | <b>Product data (9397 750 11204). ECN 853-2368 29624 of 07 March 2003.</b>  |
| 01  | 20020904 | -    | <b>Product data (9397 750 08831). ECN 853-2368 28865 of 04 September 2002.</b>  |

## 14. Data sheet status

| Level | Data sheet status <sup>[1]</sup> | Product status <sup>[2][3]</sup> | Definition   |
|-------|----------------------------------|----------------------------------|--|
| I     | Objective data                   | Development                      | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
| II    | Preliminary data                 | Qualification                    | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.             |
| III   | Product data                     | Production                       | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 15. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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