Single channel T3/E3 Framer & Line Interface for ATM, Frame Relay and PPP/IP.

The TE3-FALC® is a complete solution for a T3/E3 broadband interface. It includes DS3/E3 framing, analog line interface, two jitter attenuators and the mapping of ATM or PPP/HDLC. The TE3-FALC® also integrates a microcontroller which is running the device driver and gathering statistics as managed MIB objects.

On the line side the TE3-FALC® interfaces to a 75 Ω co-axial cable via transformers. Highly accurate analog pulse shaping removes the need to measure cable length and set the Line Build Out.

On the system side, industry standard UTOPIA and POS-PHY interface as well as a serial clock/data port are provided. This allows the TE3-FALC® to be connected to a wide array of Layer 2/3 & 4 network processors.

Applications
- Wireless base stations
- LAN/WAN router
- DSLAMs
- Remote access/concentrator
- Multimedia gateways

Analog Line Interface
- Single channel T3/E3 analog receive & transmit circuitry
- Identical T3/E3 transformer interface. True software switchable
- Clock & data recovery
- Analog LOS detection
- Single pulse template for all line length 0 - 450 ft, no need for setting of Line Build Out

Digital Jitter Attenuator
- Two separate transmit and receive jitter attenuators
- Meets jitter transfer requirements
- All line rate clocks generated internally, no requirement for external 34/45 MHz oscillators
- Clock generation unit accepts flexible frequency reference clocks, 4 MHz to 52 MHz

DS3/E3 Framer
- E3 Framer supporting G.832, G.751 & TBR24
- DS3 framer supporting M23 and C-Bit parity modes
- Processing of all DS3 overhead channels including the FEAC and MDL link
- Processing of all E3 overhead channels such as trail trace
- PLCP sub frame for DS3/E3 G.751 allowing the mapping of ATM cells
- DS3/E3 BERT unit

ATM Cell Processor
- Cell processor as per G.804
- Mapping cells directly into DS3/E3 frames or via PLCP frame

PPP Processor
- Bit and byte synchronous HDLC controller
- Generation and detection of flags, bit stuffing, CRC-16/32

System Interfaces
- Utopia Level 2 interface 8/16 Bit
- POS-PHY interface 8/16 Bit
- Serial clock and data interface
- 8/16 Bit Motorola/Intel processor interface

Test and Diagnostic
- JTAG test port
- OCDS debug port

Embedded Controller
- Embedded microcontroller with all code & data memory

General Features
- 3.3 V I/O CMOS technology
- 1.8 V core logic supply
- P-BGA-272 package 27 x 27 mm body size, 1.27 mm ball pitch
- Industrial temperature range package, -40 °C to +85 °C
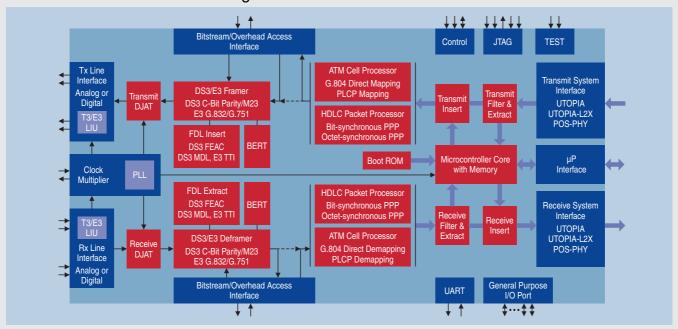
Key Features
- Integrated T3/E3 analog
- Single pulse template for all line lengths, no LBO requirement
- Jitter attenuation in both Tx and Rx
- Full featured DS3/E3 framer
- ATM and PPP/HDLC mapping
- UTOPIA or POS-PHY interface
- Integrated µC running S/W driver
- Control via 8/16 Bit Motorola/Intel µP i/f or inband ATM/PPP messages
- High level message based API
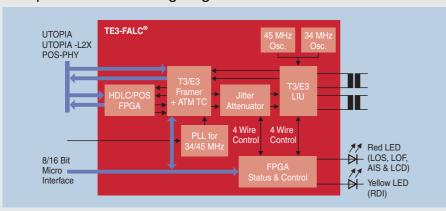
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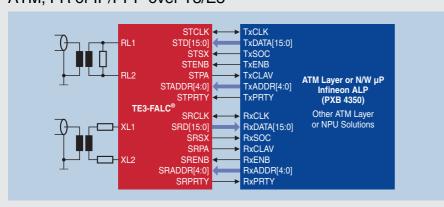N e v e r   s t o p   t h i n k i n g .

TE3-FALC® PEF 3460E Block Diagram

TE3-FALC® PEF 3460E Application Examples
Comparison with existing single channel solution

ATM, FR or IP/PPP over T3/E3

Documentation and Support Package

- Product overview
- Product Data Sheet
- Firmware Brief
- Application Notes
- Evaluation Tool EASY3460
- Configuration Assistant
- IBIS Model
- BSDL File

Infineon Companion Products

- FALC® 56: PEB 2256
- QuadFALC™: PEB 22554
- QuadLIU™: PEB 22504
- TE3-LIU™: PEB 3452
- TE3-MUX™: PEB 3445
- DSCC4: PEB 20534
- TE3-CHATT: PEB 3456
- ALP: PXB 4350
- AOP: PXB 4340
- ABM: PXB 4330
- IWE8: PXB 4220/4221
- IWORX: PXB 4225

Attention please!

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Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide.

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