

# FlexiSLIC™

Subscriber Line Interface Circuit

PBL 38640/2, Version 2

Wireline Communications



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**FlexiSLIC****Revision History:** 2005-04-14

Rev. 2.0

**Previous Version:** DS1

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<b>Page</b>	<b>Subjects (major changes since last revision)</b>
all	Package P-DSO-24-1 changed to P-/PG-DSO-24-8
all	Package type abbreviation SOIC changed to PDSO
all	Package P-LCC-28-2 changed to P-/PG-LCC-28-3
all	Package P-SSOP-24-1 changed to P-/PG-SSOP-24-1
<b>Page 17</b>	<b>Table 5:</b> Thermal resistance for 24-pin PDSO changed from 80.2 °C/W to 50.3 °C/W
<b>Page 30</b>	<b>Figure 9:</b> SLIC/codec circuitry changed
<b>Page 31</b>	<b>Table 6:</b> values of $R_R$ , $R_T$ , $R_{RX}$ , $R_{TX}$ , $R_B$ changed, $R_{FB}$ removed
<b>Page 36</b>	<b>Figure 11</b> changed

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# FlexiSLIC Subscriber Line Interface Circuit

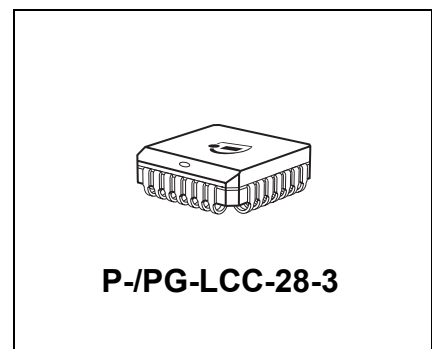
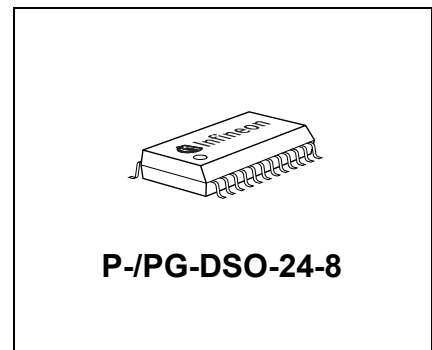
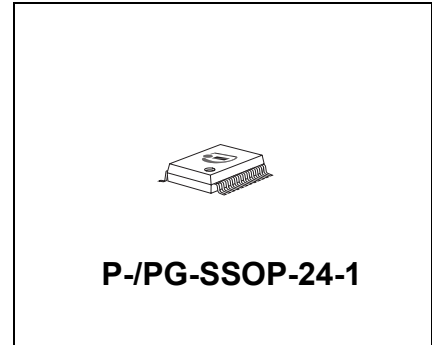
PBL 38640/2

## Version 2

### 1 Overview

#### 1.1 Features

- 24-pin SSOP package
- High and low battery with automatic switching
- 65 mW on-hook power dissipation in active state
- On-hook transmission
- Long loop battery feed tracks Vbat for maximum line voltage
- Selectable transmit gain (1x or 0.5 x)
- No power-up sequence
- 43 V open loop voltage @ -48 V battery feed
- Close tolerance current feeding
- Constant loop voltage for line leakage < 5 mA (RLeak ~ > 10 kΩ @ -48 V)
- Full longitudinal current capability during on-hook state
- Longitudinal balance > 60 dB
- Analog overtemperature protection permits transmission while the protection circuits is active
- Line voltage measurement
- Polarity reversal
- Ground key detector
- Tip open state with ring ground detector
- Programmable signal headroom
- -40 °C to +85 °C ambient temperature range



Type	Package
PBL 38640/2 SH	P-/PG-SSOP-24-1
PBL 38640/2 SO	P-/PG-DSO-24-8
PBL 38640/2 QN	P-/PG-LCC-28-3



## 1.2 Typical Applications

- Basic functionality Central Office Line card
- Digital Loop Carriers (DLC)

## 1.3 Description

The PBL 38640/2 Subscriber Line Interface Circuit (SLIC) is a 90 V bipolar integrated circuit for use in PBX, Terminal adapters and other telecommunications equipment. The PBL 38640/2 SLIC has been optimized for low total line interface cost and for a high degree of flexibility in different applications.

The PBL 38640/2 SLIC emulates resistive loop feed, programmable between  $2 \times 50 \Omega$  and  $2 \times 900 \Omega$ , with short loop current limiting adjustable to maximum 45 mA. In the current limited region the loop feed is nearly constant current with a slight slope corresponding to  $2 \times 30 \text{ k}\Omega$ .

A second lower battery voltage may be connected to the device to reduce short loop power dissipation. The SLIC automatically switches between the two battery supply voltages without need for external components or external control.

The SLIC incorporates loop current, ground key and ring-trip detection functions. The PBL 38640/2 is compatible with both loop and ground start signalling.

Two- to four-wire and four- to two-wire voice frequency (VF) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter, for example SiCoFi PEB 2466. The programmable two-wire impedance, complex or real, is set by a simple external network.

Longitudinal voltages are suppressed by a feedback loop in the SLIC and the longitudinal balance specifications meet Bellcore TR909 requirements.

The PBL 38640/2 SLIC package options are 24-pin SSOP, 24-pin PDSO or 28-pin PLCC.

### 1.4 Block Diagram

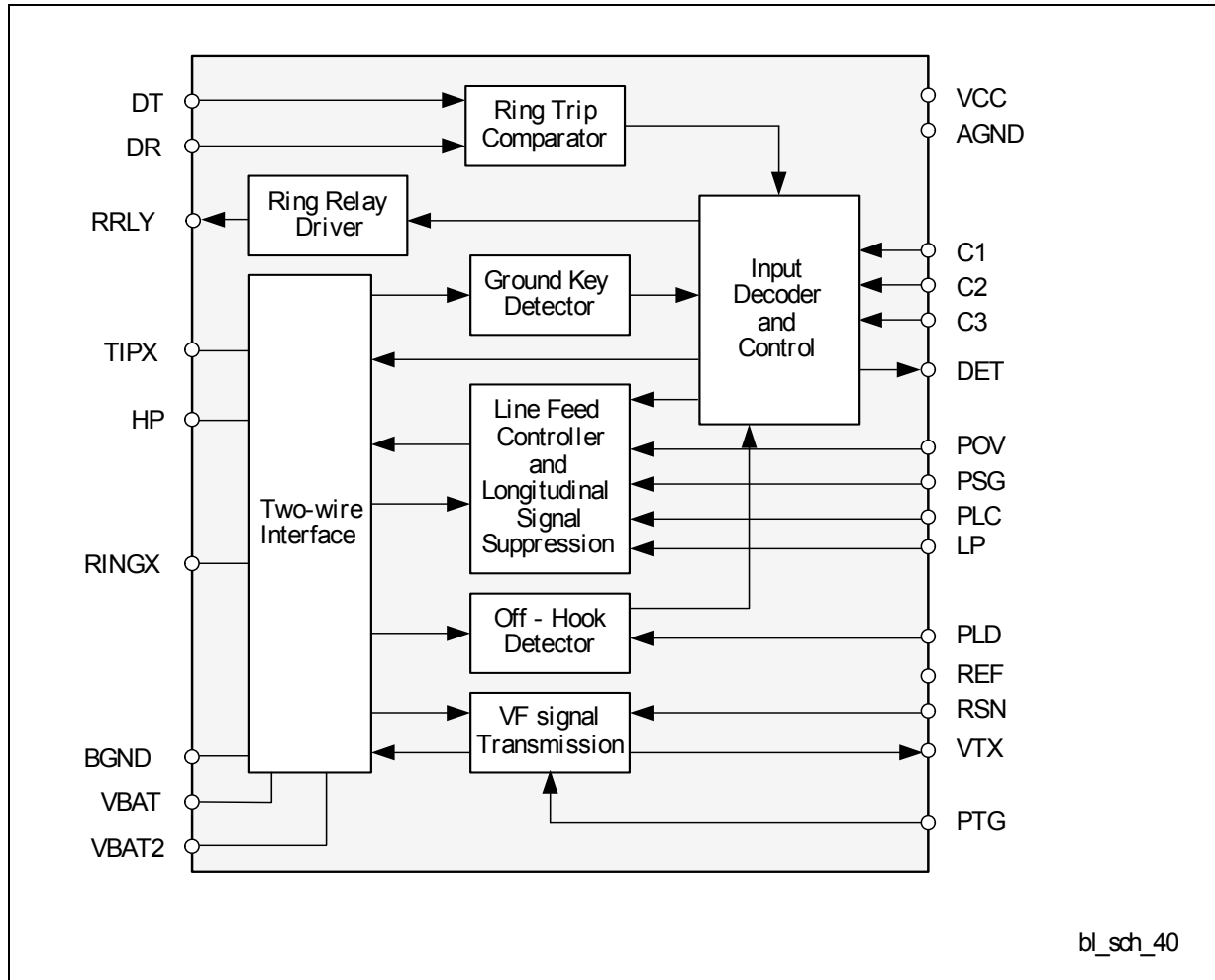
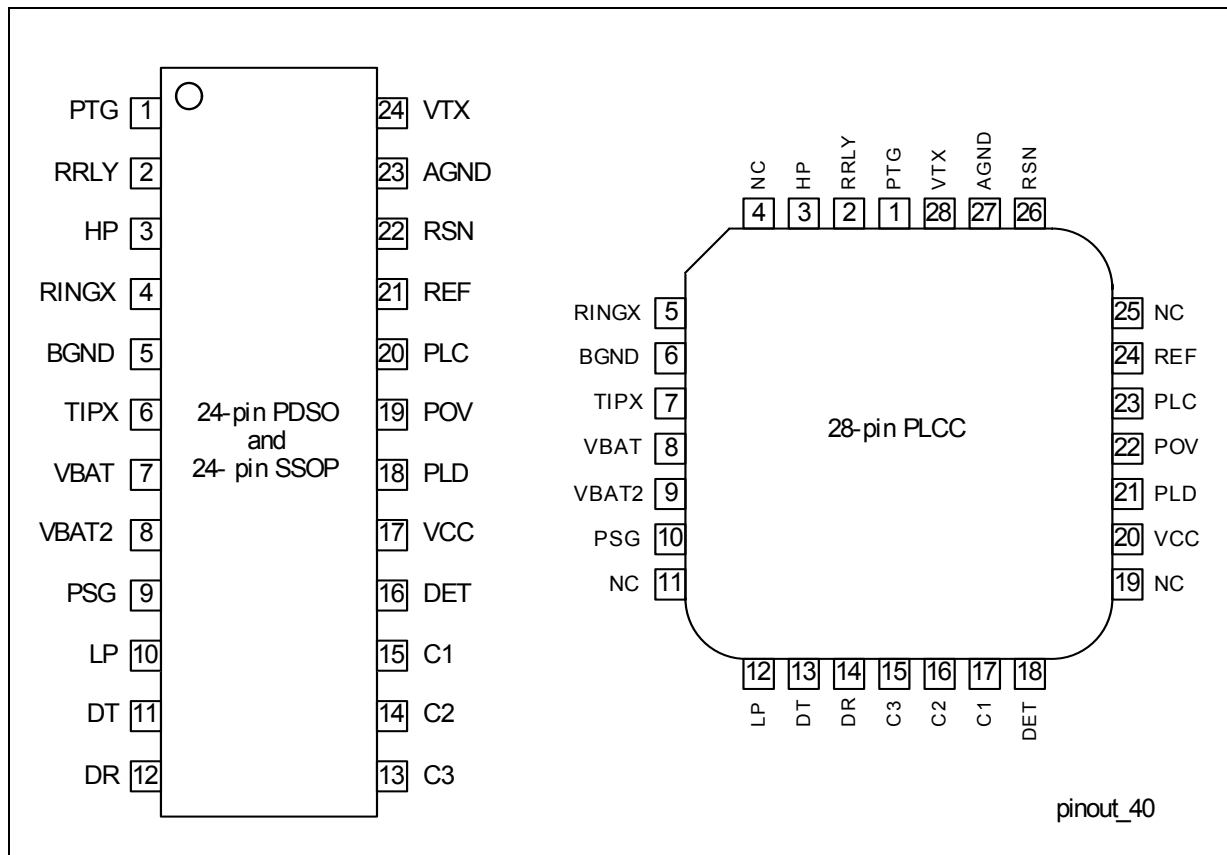


Figure 1 Block Diagram

## 2 Pin Configuration



**Figure 2 Pin Configuration, 24L-PDSO, 24L-SSOP and 28L-PLCC (top view)**

**Table 1 Pin Definition and Functions**

PDSO SSOP Pin No.	PLCC Pin No.	Name	Pin Type	Function
1	1	PTG	–	Programmable transmit gain. Left open transmit gain = 0.0 dB, connected to AGND transmit gain = -6.02 dB.
2	2	RRLY	O	Ring relay driver output. The relay coil may be connected to maximum +14 V.
3	3	HP	–	Connection for high pass filter capacitor, $C_{HP}$ . Other end of $C_{HP}$ connects to TIPX.

**Pin Configuration**
**Table 1 Pin Definition and Functions (cont'd)**

PDSO SSOP Pin No.	PLCC Pin No.	Name	Pin Type	Function
4	5	RINGX	–	The RINGX pin connects to the ring lead of the two-wire interface via over voltage protection components and ring relay (and optional test relay).
5	6	BGND	–	Battery ground, should be tied together with AGND.
6	7	TIPX	–	The TIPX pin connects to the tip lead of the two-wire interface via over voltage protection components and ring relay (and optional test relay).
7	8	$V_{BAT}$	–	Battery supply voltage. Negative with respect to GND.
8	9	$V_{BAT2}$	–	An optional second (2) Battery Voltage connects to this pin via an external diode.
9	10	PSG	–	Programmable saturation guard. The resistive part of the DC feed characteristics is programmed by a resistor connected from this pin to $V_{BAT}$ .
10	12	LP	–	Connection for low pass filter capacitor, $C_{LP}$ . Other end of $C_{LP}$ connects to $V_{BAT}$ .
11	13	DT	I	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The external ring trip network connects to this input.
12	14	DR	I	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The external ring trip network connects to this input.
13	15	C3	I	C1, C2, C3 are digital inputs (positive logic, internal pull-up), which control the SLIC operating states. Refer to <b>Table 2</b> for details.
14	16	C2	I	
15	17	C1	I	

**Pin Configuration**
**Table 1 Pin Definition and Functions (cont'd)**

<b>PDSO SSOP Pin No.</b>	<b>PLCC Pin No.</b>	<b>Name</b>	<b>Pin Type</b>	<b>Function</b>
16	18	DET	O	Detector output. Active low when indicating loop or ring-trip detection, active high when indicating ground key detection.
17	20	$V_{CC}$	–	+5 V power supply.
18	21	PLD	–	Programmable loop detector threshold. The loop detection threshold is programmed by a resistor connected from this pin to AGND.
19	22	POV	–	Programmable overhead voltage. If pin is left open: The overhead voltage is internally set to min 2.7 V in off-hook and min 1.1 V in on-hook. If a resistor is connected between this pin and AGND: The overhead voltage can be set to higher values.
20	23	PLC	–	Programmable line current, the constant current part of the DC feed characteristic is programmed by a resistor connected from this pin to AGND.
21	24	REF	–	A reference, 49.9 k $\Omega$ , resistor should be connected from this pin to AGND.
22	26	RSN	–	Receive summing node. 200 times the AC current flowing into this pin equals the metallic (transversal) AC current flowing from RINGX to TIPX. Programming networks for two-wire impedance and receive gain connect to the receive node. A resistor should be connected from this pin to AGND.
23	27	AGND	–	Analog ground, should be tied together with BGND.

**Table 1 Pin Definition and Functions (cont'd)**

PDSO SSOP Pin No.	PLCC Pin No.	Name	Pin Type	Function
24	28	VTX	O	Transmit vf output. The AC voltage difference between TIPX and RINGX, the AC metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of one (or one half, see pin PTG). The two-wire impedance programming network connects between VTX and RSN.
-	4, 11,19, 25	NC	–	Not Connected.

**Table 2 SLIC Operating States**

State	C3	C2	C1	SLIC Operating State	Active Detector (DET Response)
0	0	0	0	Open circuit	No active detector (DET is set high)
1	0	0	1	Ringing	Ring-trip detector (DET active low)
2	0	1	0	Active	Loop detector (DET active low)
3	0	1	1	Active	Line voltage measurement <sup>1)</sup>
4	1	0	0	Tip open	Loop detector (DET active low)
5	1	0	1	Active	Ground key detector (DET active high)
6	1	1	0	Active reverse	Loop detector (DET active low)
7	1	1	1	Active reverse	Ground key detector (DET active high)

1) Previous state must be active - loop or ground key detector.

### 3 Electrical Characteristics

**Table 3 Absolute Maximum Ratings**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
<b>Temperature, Humidity</b>						
Storage temperature range	$T_{Stg}$	-55	–	150	°C	–
Operating temperature range	$T_{Amb}$	-40	–	110	°C	–
Operating junction temperature range <sup>1)</sup>	$T_J$	-40	–	140	°C	–
<b>Power Supply (<math>-40\text{ °C} \leq T_{Amb} \leq +85\text{ °C}</math>)</b>						
$V_{CC}$ with respect to A/BGND	$V_{CC}$	-0.4	–	6.5	V	–
$V_{BAT2}$ with respect to A/BGND	$V_{BAT2}$	$V_{BAT}$	–	0.4	V	–
$V_{BAT}$ with respect to A/BGND, continuous	$V_{BAT}$	-75	–	0.4	V	–
$V_{BAT}$ with respect to A/BGND, 10 ms	$V_{BAT}$	-80	–	0.4	V	–
<b>Power Dissipation</b>						
Continuous power dissipation	$P_D$	–	–	1.5	W	$T_{Amb} \leq +85\text{ °C}$
<b>Ground</b>						
Voltage between AGND and BGND	$V_G$	-0.3	–	0.3	V	–
<b>Relay Driver</b>						
Ring relay supply voltage	–	–	–	BGND +14	V	–
<b>Ring Trip Comparator</b>						
Input voltage	$V_{DT}, V_{DR}$	$V_{BAT}$	–	AGND	V	–
Input current	$I_{DT}, I_{DR}$	-5	–	5	mA	–
<b>Digital Inputs, Outputs (C1, C2, C3, DET)</b>						
Input voltage	$V_{ID}$	-0.4	–	$V_{CC}$	V	–
Output voltage	$V_{OD}$	-0.4	–	$V_{CC}$	V	–

**Electrical Characteristics**
**Table 3 Absolute Maximum Ratings (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
<b>TIPX and RINGX Terminals</b> ( $-40\text{ }^{\circ}\text{C} \leq T_{\text{Amb}} \leq +85\text{ }^{\circ}\text{C}$ , $V_{\text{BAT}} = -50\text{ V}$ )						
TIPX or RINGX current	$I_{\text{TIPX}}$ , $I_{\text{RINGX}}$	-100	–	100	mA	–
TIPX or RINGX voltage, continuous (referenced to AGND) <sup>2)</sup>	$V_{\text{TA}}$ , $V_{\text{RA}}$	-80	–	2	V	–
TIPX or RINGX <sup>2)</sup>	$V_{\text{TA}}$ , $V_{\text{RA}}$	$V_{\text{BAT}}$ - 10	–	5	V	pulse < 10 ms, $t_{\text{Rep}} > 10\text{ s}$
TIPX or RINGX <sup>2)</sup>	$V_{\text{TA}}$ , $V_{\text{RA}}$	$V_{\text{BAT}}$ - 25	–	10	V	pulse < 1 $\mu\text{s}$ , $t_{\text{Rep}} > 10\text{ s}$
TIP or RING <sup>2)3)</sup>	$V_{\text{TA}}$ , $V_{\text{RA}}$	$V_{\text{BAT}}$ - 35	–	15	V	pulse < 250 ns, $t_{\text{Rep}} > 10\text{ s}$

1) The circuit includes thermal protection. Operation above max. junction temperature may degrade device reliability.

2) With the diodes  $D_{\text{VB}}$  and  $D_{\text{VB2}}$  included, see [Figure 9](#).

3)  $R_{\text{F1}}$  and  $R_{\text{F2}} > 20\text{ }\Omega$  is also required. Pulse is supplied to RING and TIP outside  $R_{\text{F1}}$  and  $R_{\text{F2}}$ .

**Attention: Stresses above those values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

**Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

**Table 4 Operating Range**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Ambient temperature	$T_{\text{Amb}}$	-40	–	85	$^{\circ}\text{C}$	–
$V_{\text{CC}}$ with respect to AGND	$V_{\text{CC}}$	4.75	–	5.25	V	–
$V_{\text{BAT}}$ with respect to AGND	$V_{\text{BAT}}$	-58	–	-8	V	–
AGND with respect to BGND	$V_{\text{G}}$	-100	–	100	mV	–



### 3.1 Characteristics

The specification is made with following setup:  $-40\text{ °C} \leq T_{\text{Amb}} \leq +85\text{ °C}$ , PTG = open (see pin description),  $V_{\text{CC}} = +5\text{ V} \pm 5\%$ ,  $V_{\text{BAT}} = -58\text{ V}$  to  $-40\text{ V}$ ,  $V_{\text{BAT2}} = -32\text{ V}$ ,  $R_{\text{LC}} = 32.4\text{ k}\Omega$ ,  $I_{\text{L}} = 27\text{ mA}$ ,  $R_{\text{L}} = 600\text{ }\Omega$ ,  $R_{\text{F1}} = R_{\text{F2}} = 0$ ,  $R_{\text{REF}} = 49.9\text{ k}\Omega$ ,  $C_{\text{HP}} = 47\text{ nF}$ ,  $C_{\text{LP}} = 0.15\text{ }\mu\text{F}$ ,  $R_{\text{T}} = 120\text{ k}\Omega$ ,  $R_{\text{SG}} = 0\text{ k}\Omega$ ,  $R_{\text{RX}} = 60\text{ k}\Omega$ ,  $R_{\text{R}} = 52.3\text{ k}\Omega$ ,  $R_{\text{OV}} = \text{infinite}$ .

Current definition: current is positive if flowing into a pin unless stated otherwise.

**Table 5 Characteristics**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
<b>Two-Wire Port</b>						
Overhead level <sup>1)</sup> , $18\text{ mA} \leq I_{\text{LDC}}$ Active, 1% THD $R_{\text{OV}} = \text{infinite}$ see <a href="#">Figure 3</a>	$V_{\text{TRO}}$	2.7	–	–	$V_{\text{Peak}}$	–
		1.1	–	–	$V_{\text{Peak}}$	On-Hook, $I_{\text{LDC}} \leq 5\text{ mA}$
Input impedance <sup>2)</sup>	$Z_{\text{TRX}}$	–	$Z_{\text{T}}/200$	–	$\Omega$	–
Longitudinal impedance	$Z_{\text{LOT}},$ $Z_{\text{LOR}}$	–	20	35	$\Omega/\text{wire}$	$0 < f < 100\text{ Hz}$
Longitudinal current limit	$I_{\text{LOT}},$ $I_{\text{LOR}}$	28	–	–	$\text{mA}_{\text{rms}}/\text{wire}$	Active

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition	
		Min.	Typ.	Max.			
Longitudinal to metallic balance (IEEE standard 455-1985), $Z_{TRX} = 736 \Omega$ Normal polarity	$B_{LM}$	63	66	–	dB	$0.2 \text{ kHz} \leq f \leq 1.0 \text{ kHz}$ $T_{AMB} 0-70 \text{ }^\circ\text{C}$	
		60	66	–	dB	$1.0 \text{ kHz} < f < 3.4 \text{ kHz}$ $T_{AMB} 0-70 \text{ }^\circ\text{C}$	
60		66				$0.2 \text{ kHz} \leq f \leq 1.0 \text{ kHz}$ $T_{AMB} -40-85 \text{ }^\circ\text{C}$	
55		66	–	dB	$1.0 \text{ kHz} < f < 3.4 \text{ kHz}$ $T_{AMB} -40-85 \text{ }^\circ\text{C}$		
Reverse polarity		59	66	–	dB	$0.2 \text{ kHz} \leq f \leq 1.0 \text{ kHz}$ $T_{AMB} 0-70 \text{ }^\circ\text{C}$	
		55	66	–	dB	$1.0 \text{ kHz} < f < 3.4 \text{ kHz}$ $T_{AMB} 0-70 \text{ }^\circ\text{C}$	
		55	66				$0.2 \text{ kHz} \leq f \leq 1.0 \text{ kHz}$ $T_{AMB} -40-85 \text{ }^\circ\text{C}$
		55	66	–	dB	$1.0 \text{ kHz} < f < 3.4 \text{ kHz}$ $T_{AMB} -40-85 \text{ }^\circ\text{C}$	

Electrical Characteristics

Table 5 Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Longitudinal to metallic balance $B_{LME} = 20 \times \log E_{LO}/V_{TR} $ , see <a href="#">Figure 4</a> Normal polarity  Reverse polarity	$B_{LME}$	63	66	–	dB	0.2 kHz $\leq f \leq$ 1.0 kHz $T_{AMB}$ 0-70 °C
		60	66	–	dB	1.0 kHz $< f <$ 3.4 kHz $T_{AMB}$ 0-70 °C
		60	66			0.2 kHz $\leq f \leq$ 1.0 kHz $T_{AMB}$ -40-85 °C
		55	66	–	dB	1.0 kHz $< f <$ 3.4 kHz $T_{AMB}$ -40-85 °C
		59	66	–	dB	0.2 kHz $\leq f \leq$ 1.0 kHz $T_{AMB}$ 0-70 °C
		55	66	–	dB	1.0 kHz $< f <$ 3.4 kHz $T_{AMB}$ 0-70 °C
		55	66			0.2 kHz $\leq f \leq$ 1.0 kHz $T_{AMB}$ -40-85 °C
		55	66	–	dB	1.0 kHz $< f <$ 3.4 kHz $T_{AMB}$ -40-85 °C

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Longitudinal to four-wire balance $B_{LFE} = 20 \times \log E_{LO}/V_{TX} $ , see <a href="#">Figure 4</a> Normal polarity	$B_{LFE}$	63	66	–	dB	0.2 kHz $\leq f \leq$ 1.0 kHz $T_{AMB}$ 0-70 °C
		60	66	–	dB	1.0 kHz $< f <$ 3.4 kHz $T_{AMB}$ 0-70 °C
		60	66			0.2 kHz $\leq f \leq$ 1.0 kHz $T_{AMB}$ -40-85 °C
		55	66	–	dB	1.0 kHz $< f <$ 3.4 kHz $T_{AMB}$ -40-85 °C
		59	66	–	dB	0.2 kHz $\leq f \leq$ 1.0 kHz $T_{AMB}$ 0-70 °C
		55	66	–	dB	1.0 kHz $< f <$ 3.4 kHz $T_{AMB}$ 0-70 °C
		55	66			0.2 kHz $\leq f \leq$ 1.0 kHz $T_{AMB}$ -40-85 °C
		55	66	–	dB	1.0 kHz $< f <$ 3.4 kHz $T_{AMB}$ -40-85 °C
Reverse polarity	$B_{LFE}$	59	66	–	dB	0.2 kHz $\leq f \leq$ 1.0 kHz $T_{AMB}$ 0-70 °C
		55	66	–	dB	1.0 kHz $< f <$ 3.4 kHz $T_{AMB}$ 0-70 °C
Metallic to longitudinal balance $B_{MLE} = 20 \times \log V_{TR}/V_{LO} $ , $E_{RX} = 0$ V, see <a href="#">Figure 5</a>	$B_{MLE}$	40	50	–	dB	0.2 kHz $< f <$ 3.4 kHz
Four-wire to longitudinal balance $B_{FLE} = 20 \times \log E_{RX}/V_{LO} $ , see <a href="#">Figure 5</a>	$B_{FLE}$	40	50	–	dB	0.2 kHz $< f <$ 3.4 kHz

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Two-wire return loss <sup>3)</sup> $r = 20 \times \log \frac{ Z_{TRX} + Z_L }{ Z_{TRX} - Z_L }$	$r$	30	35	–	dB	0.2 kHz < $f$ < 1.0 kHz
		20	22	–	dB	1.0 kHz < $f$ < 3.4 kHz
TIPX idle voltage	$V_{TI}$	–	-1.3	–	V	Active, $I_L < 5$ mA
RINGX idle voltage	$V_{RI}$	–	$V_{BAT+}$ 3.0	–	V	Active, $I_L < 5$ mA
		–	$V_{BAT+}$ 3.0	–	V	Tip open, $I_L < 5$ mA
Open loop voltage	$V_{TR}$	–	$V_{BAT+}$ 4.3	–	V	Active, $I_L < 5$ mA

**Four-Wire Transmit Port (VTX)**

Overhead level <sup>4)</sup> , Load imp. > 20 k $\Omega$ 1% THD see <a href="#">Figure 6</a>	$V_{TXO}$	2.7	–	–	$V_{Peak}$	$I_L > 18$ mA
		1.1	–	–	$V_{Peak}$	On-Hook, $I_L \leq 5$ mA
Output offset voltage	$\Delta V_{TX}$	-100	–	100	mV	–
Output impedance	$Z_{TX}$	–	15	50	$\Omega$	0.2 kHz < $f$ < 3.4 kHz

**Four-Wire Receive Port (receive summing node = RSN)**

RSN DC voltage	$V_{RSNdc}$	1.15	1.25	1.35	V	$I_{RSN} = -55$ $\mu$ A
RSN impedance		–	8	20	$\Omega$	0.2 kHz < $f$ < 3.4 kHz
RSN current ( $I_{RSN}$ ) to metallic loop current ( $I_L$ ) gain	$\alpha_{RSN}$	–	200	–	ratio	0.3 kHz < $f$ < 3.4 kHz

**Frequency Response**

Two-wire to four-wire, relative to 0 dBm, 1.0 kHz, $E_{RX} = 0$ V, see <a href="#">Figure 7</a>	$g_{2-4}$	-0.20	–	0.10	dB	0.3 kHz < $f$ < 3.4 kHz
		-1.0	–	0.1	dB	$f = 8$ kHz, 12 kHz, 16 kHz

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Four-wire to two-wire, relative to 0 dBm, 1.0 kHz, $E_L = 0$ V, see <a href="#">Figure 7</a>	$g_{4-2}$	-0.2	–	0.1	dB	$0.3 \text{ kHz} < f < 3.4 \text{ kHz}$
		-1.0	–	0	dB	$f = 8 \text{ kHz}, 12 \text{ kHz}$
		-2.0	–	0	dB	$f = 16 \text{ kHz}$
Four-wire to four-wire, relative to 0 dBm, 1.0 kHz, $E_L = 0$ V, see <a href="#">Figure 7</a>	$g_{4-4}$	-0.2	–	0.1	dB	$0.3 \text{ kHz} < f < 3.4 \text{ kHz}$
<b>Insertion Loss</b>						
Two-wire to four-wire <sup>5)</sup> , $G_{2-4} = 20 \times \log V_{TX}/V_{TR} $ 0 dBm, 1.0 kHz $E_{RX} = 0$ V	$G_{2-4}$	-0.2	–	0.2	dB	PTG = Open see <a href="#">Figure 7</a>
		-6.22	-6.02	-5.82	dB	PTG = AGND
Four-wire to two-wire <sup>6)</sup> , $G_{4-2} = 20 \times \log V_{TR}/V_{RX} $ , $E_L = 0$ V, see <a href="#">Figure 7</a>	$G_{4-2}$	-0.2	–	0.2	dB	0 dBm, 1.0 kHz
<b>Gain Tracking</b>						
Two-wire to four-wire <sup>7)</sup> , Ref. -10 dBm, 1.0 kHz, see <a href="#">Figure 7</a>		-0.1	–	0.1	dB	-40 dBm to +3 dBm
		-0.2	–	0.2	dB	-55 dBm to -40 dBm
Four-wire to two-wire, Ref. -10 dBm, 1.0 kHz, see <a href="#">Figure 7</a>		-0.1	–	0.1	dB	-40 dBm to +3 dBm
		-0.2	–	0.2	dB	-55 dBm to -40 dBm
<b>Noise</b>						
Idle channel noise at two-wire port <sup>8)</sup> (TIPX-RINGX) or four-wire (VTX) output		–	–	12	dBrnC	C-message weighting
		–	–	-78	dBmp	Psophometrical weighting

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
<b>Harmonic Distortion</b>						
Two-wire to four-wire, see <a href="#">Figure 7</a>		–	-67	-50	dB	0 dBm $0.3 \text{ kHz} < f <$ 3.4 kHz
Four-wire to two-wire		–	-67	-50	dB	
<b>Battery Feed Characteristics</b>						
Loop current in the current limited region, reference A, B & C see <a href="#">Figure 13</a>	$I_L$	$0.92 \times I_L$	$I_L$	$1.08 \times I_L$	mA	$18 \text{ mA} \leq I_L \leq 45 \text{ mA}$
Tip open state TIPX current see <a href="#">Figure 8</a>	$I_{\text{Leak}}$	–	–	-100	$\mu\text{A}$	S = closed; R = 7 k $\Omega$ <sup>9)</sup>
Tip open state RINGX current see <a href="#">Figure 8</a>	$I_{\text{LRT0}}$	–	$I_L$	–	mA	$R_{\text{LRT0}} = 0 \Omega,$ $V_{\text{Bat}} = -48 \text{ V}$
		–	17	–	mA	$R_{\text{LRT0}} = 2.5 \text{ k}\Omega,$ $V_{\text{Bat}} = -48 \text{ V}$
Tip open state RINGX voltage see <a href="#">Figure 8</a>	$V_{\text{RT0}}$	–	$V_{\text{Bat}} + 6$	–	V	$I_{\text{LRT0}} < 23 \text{ mA}$
Tip voltage (ground start) see <a href="#">Figure 8</a>	–	-4	-2.2	–	V	Active state, Tip lead open (S open), Ring lead to ground through 150 $\Omega$
Tip voltage (ground start) see <a href="#">Figure 8</a>	–	-6	-2.4	–	V	Active state, Tip lead to -48 V through 7 k $\Omega$ (S closed), Ring lead to ground through 150 $\Omega$
Open circuit loop current	$I_{\text{LOC}}$	-100	0	100	$\mu\text{A}$	$R_L = 0 \Omega$

**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
<b>Loop Detector</b>						
Programmable threshold,	$I_{LTh}$	$0.85 \times I_{LTh}$	$I_{LTh}$	$1.15 \times I_{LTh}$	mA	$I_{LTh} = 500/R_{LD}$ $R_{LD}$ in k $\Omega$ , $7 \text{ mA} \leq I_{LTh}$
Tip open state	–	$0.85 \times I_{LTh}$	$I_{LTh}$	$1.15 \times I_{LTh}$	mA	$I_{LTh} = 500/R_{LD}$
<b>Ground Key Detector</b>						
Ground key detector threshold	–	10	16	22	mA	( $I_{LTIPX}$ and $I_{LRINGX}$ current difference to trigger ground key detector)
<b>Line Voltage Measurement</b>						
Pulse width <sup>10)</sup>	$t_{LVM}$	–	5.5	–	$\mu\text{s/V}$	
<b>Ring Trip Comparator</b>						
Offset voltage	$\Delta V_{DTDR}$	-20	0	20	mV	Source resistance, $R_S = 0 \Omega$
Input bias current	$I_B$	-200	-20	200	nA	$I_B = (I_{DT} + I_{DR})/2$
Input common mode range	$V_{DT}, V_{DR}$	$V_{BAT} + 1$	–	-1	V	
<b>Ring Relay Driver</b>						
Saturation voltage	$V_{OL}$	–	0.2	0.5	V	$I_{OL} = 50 \text{ mA}$
Off state leakage current	$I_{LK}$	–	–	10	$\mu\text{A}$	$V_{OH} = 12 \text{ V}$
<b>Digital Inputs (C1, C2, C3)</b>						
Input low voltage	$V_{IL}$	0	–	0.5	V	–
Input high voltage	$V_{IH}$	2.5	–	$V_{CC}$	V	–
Input low current	$I_{IL}$	–	–	-50	$\mu\text{A}$	$V_{IL} = 0.5 \text{ V}$
Input high current	$I_{IH}$	–	–	50	$\mu\text{A}$	$V_{IH} = 2.5 \text{ V}$



**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
<b>Detector Output (DET)</b>						
Output low voltage	$V_{OL}$	–	–	0.7	V	$I_{OL} = 0.5 \text{ mA}$
Internal pull-up resistor to $V_{CC}$		–	15	–	k $\Omega$	–
<b>Power Dissipation (<math>V_{BAT} = -48 \text{ V}</math>, <math>V_{BAT2} = -32 \text{ V}</math>)</b>						
Power Dissipation	$P_1$	–	10	15	mW	Open circuit (C1, C2, C3 = 0)
Power Dissipation	$P_2$	–	65	85	mW	Active (On-hook) Long current = 0 mA
Power Dissipation	$P_3$	–	730	–	mW	Active (Off-hook) $R_L = 300 \Omega$
Power Dissipation	$P_4$	–	360	–	mW	Active (Off-hook) $R_L = 800 \Omega$
<b>Power Supply Currents (<math>V_{BAT} = -48 \text{ V}</math>)</b>						
$V_{CC}$ current	$I_{CC}$	–	1.2	2.0	mA	Open circuit (C1, C2, C3 = 0)
$V_{BAT}$ current	$I_{BAT}$	-0.1	-0.05	–	mA	Open circuit (C1, C2, C3 = 0)
$V_{CC}$ current	$I_{CC}$	–	2.8	4.0	mA	Active, On-hook, Long current = 0 mA
$V_{BAT}$ current	$I_{BAT}$	-1.5	-1.0	–	mA	Active, On-hook, Long current = 0 mA
<b>Power Supply Rejection Ratios</b>						
$V_{CC}$ to 2- or 4-wire port		30	42	–	dB	Active, $f = 1 \text{ kHz}$ , $V_n = 100 \text{ mV}$
$V_{BAT2}$ to 2- or 4-wire port		40	60	–	dB	Active, $f = 1 \text{ kHz}$ , $V_n = 100 \text{ mV}$
$V_{BAT}$ to 2- or 4-wire port		36	45	–	dB	Active, $f = 1 \text{ kHz}$ , $V_n = 100 \text{ mV}$

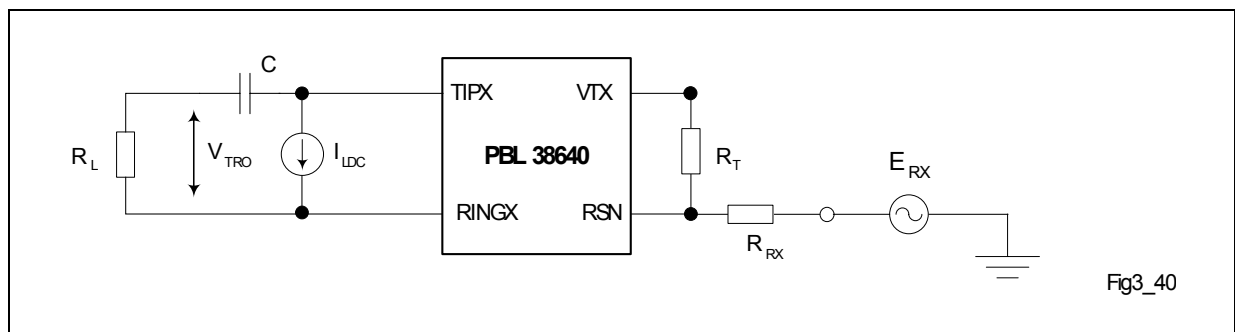
**Electrical Characteristics**
**Table 5 Characteristics (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
<b>Temperature Guard</b>						
Junction threshold temperature	$T_{JG}$	–	145	–	°C	–
<b>Thermal Resistance</b>						
24-pin SSOP	$R_{th, j\text{p}}$	–	55	–	°C/W	–
	$R_{th, jA}$	–	66.9	–	°C/W	P-/PG-SSOP-24-1, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber
24-pin PDSO	$R_{th, j\text{p}}$	–	43	–	°C/W	–
	$R_{th, jA}$	–	50.3	–	°C/W	P-/PG-DSO-24-8, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber
28-pin PLCC	$R_{th, j\text{p}}$	–	39	–	°C/W	–
	$R_{th, jA}$	–	50.4	–	°C/W	P-/PG-LCC-28-3, 4-layer PCB; Junction to ambient thermal resistance in JEDEC still air chamber

1) The overhead level can be adjusted with the resistor  $R_{OV}$  for higher levels, for example min 3.1  $V_{Peak}$ , and is specified at the two-wire port with the signal source at the four-wire receive port.

## Electrical Characteristics

- 2) The two-wire impedance is programmable by selection of external component values according to:  
 $Z_{TRX} = Z_T / (G_{2-4S} \times \alpha_{RSN})$  where:  
 $Z_{TRX}$  = impedance between the TIPX and RINGX terminals  
 $Z_T$  = programming network between the VTX and RSN terminals  
 $G_{2-4S}$  = transmit gain, nominally = 1 (or 0.5, see pin PTG)  
 $\alpha_{RSN}$  = receive current gain, nominally 200 (current defined as positive flowing into the receive summing node, RSN, and when flowing from ring to tip).
- 3) Higher return loss values can be achieved by adding a reactive component to  $R_T$ , the two-wire terminating impedance programming resistance, for example by dividing  $R_T$  into two equal halves and connecting a capacitor from the common point to ground.
- 4) The overhead level can be adjusted with the resistor  $R_{OV}$  for higher levels, for example min  $3.1 V_{Peak}$ , and is specified at the four-wire transmit port, (VTX) with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is  $G_{2-4S} = 1$  (or 0.5, see pin PTG).
- 5) Pin PTG = Open sets transmit gain to nom. 0.0 dB.  
 Pin PTG = AGND sets transmit gain to nom. -6.02 dB  
 Secondary protection resistor  $R_F$  (see [Figure 9](#)) impacts the insertion loss as explained in [Chapter 5](#). The specified insertion loss is valid for  $R_F = 0$ .
- 6) The specified insertion loss tolerance does not include errors caused by external components.
- 7) The level is specified at the two-wire port.
- 8) The two-wire idle noise is specified with the port terminated in  $600 \Omega$  ( $R_L$ ), and with the four-wire receive port grounded ( $E_{RX} = 0$ ; see [Figure 7](#)). The four-wire idle noise at  $V_{TX}$  is specified with the two-wire port terminated in  $600 \Omega$  ( $R_L$ ). The noise specification is referenced to a  $600 \Omega$  programmed two-wire impedance level at  $V_{TX}$ . The four-wire receive port is grounded ( $E_{RX} = 0$ ).
- 9) If  $|V_{Bat} + 2 V| \leq |V_{BExt}|$ , where  $V_{Bat}$  is the voltage at VBAT, the current  $I_{Leak}$  is limited to  $\sim 5$  mA,
- 10) Previous state must be active - loop or ground key detector.



**Figure 3 Overhead Level,  $V_{TRO}$ , Two-Wire Port**

$$1/\omega C \ll R_L, R_L = 600 \Omega, R_T = 120 \text{ k}\Omega, R_{RX} = 60 \text{ k}\Omega$$

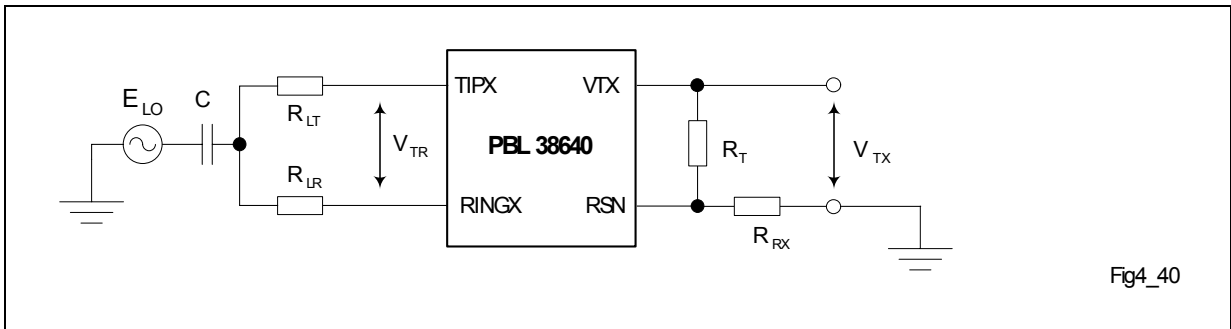


Fig4\_40

**Figure 4 Longit. to Metallic,  $B_{LME}$  and Longit. to Four-Wire,  $B_{LFE}$  Balance**

$1/\omega C \ll 150 \Omega$ ,  $R_{LT} = R_{LR} = R_L / 2 = 300 \Omega$ ,  $R_T = 120 \text{ k}\Omega$ ,  $R_{RX} = 60 \text{ k}\Omega$

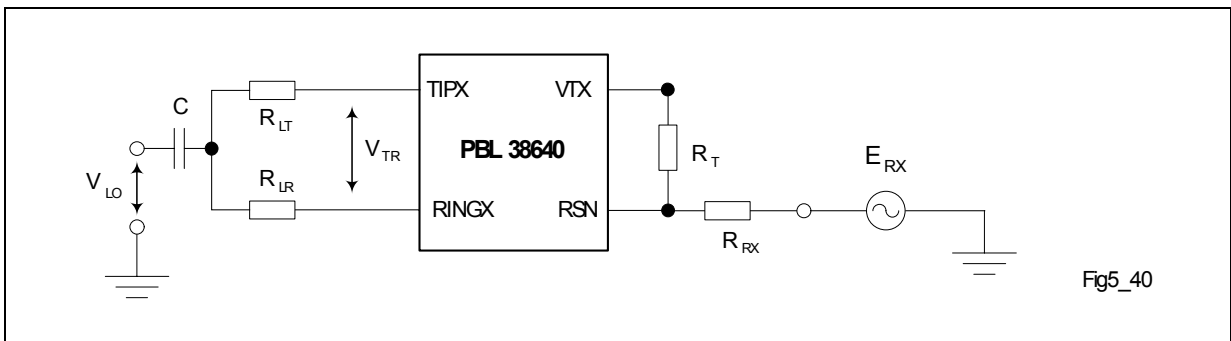


Fig5\_40

**Figure 5 Metallic to Longit.,  $B_{MLE}$  and Four-Wire to Longit. Balance,  $B_{FLE}$**

$1/\omega C \ll 150 \Omega$ ,  $R_{LT} = R_{LR} = R_L / 2 = 300 \Omega$ ,  $R_T = 120 \text{ k}\Omega$ ,  $R_{RX} = 60 \text{ k}\Omega$

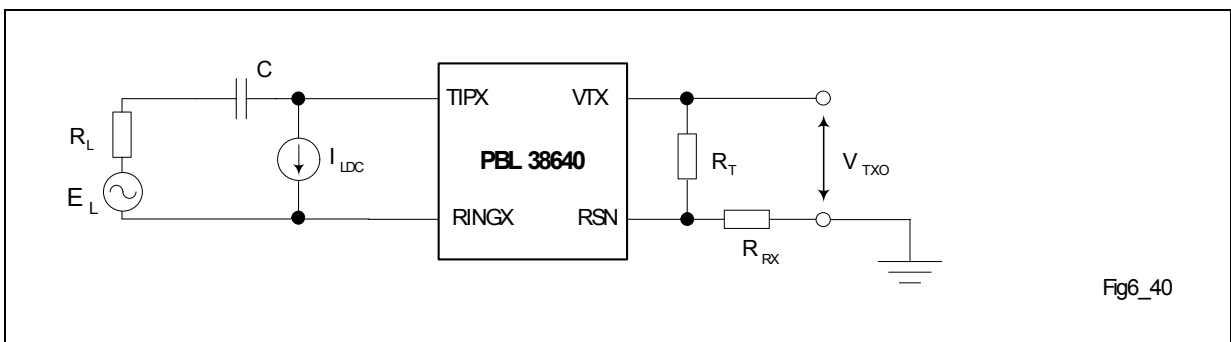
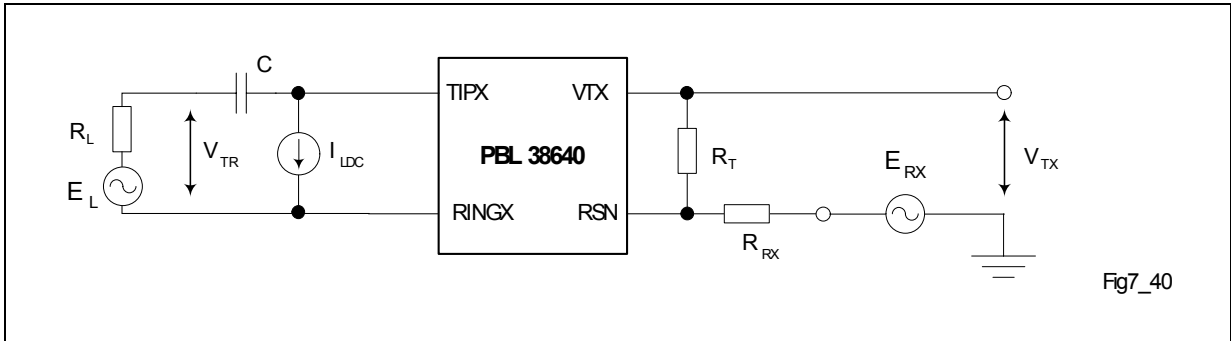


Fig6\_40

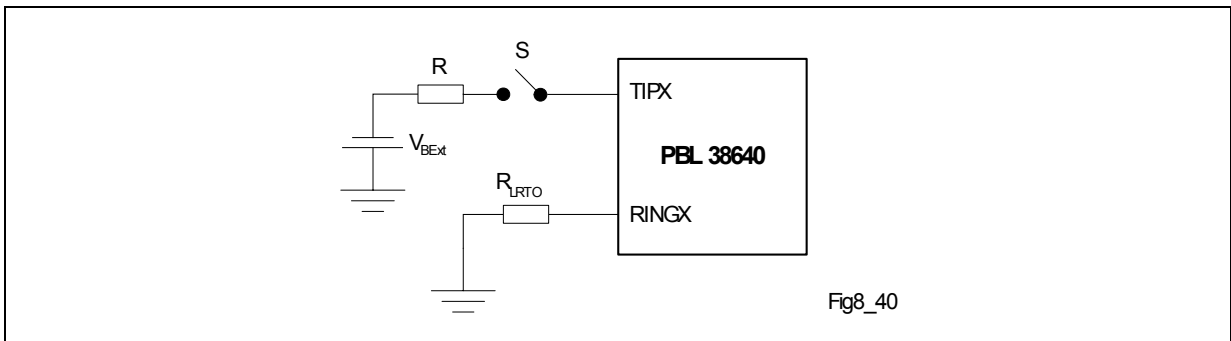
**Figure 6 Overhead Level,  $V_{TXO}$ , Four-Wire Transmit Port**

$1/\omega C \ll R_L$ ,  $R_L = 600 \Omega$ ,  $R_T = 120 \text{ k}\Omega$ ,  $R_{RX} = 60 \text{ k}\Omega$



**Figure 7 Frequency Response, Insertion Loss, Gain Tracking**

$1/\omega C \ll R_L$ ,  $R_L = 600 \Omega$ ,  $R_T = 120 \text{ k}\Omega$ ,  $R_{RX} = 60 \text{ k}\Omega$



**Figure 8 TIPX Voltage**



## 4.1 Recommended Components

**Table 6 Resistors**

Resistor	Value	Tolerance	Specification
$R_{SG}$	0 $\Omega$	–	1/10 W
$R_{LD}$	49.9 k $\Omega$	1%	1/10 W
$R_{OV}$	User programmable	–	–
$R_{LC}$	32.4 k $\Omega$	1%	1/10 W
$R_{REF}$	49.9 k $\Omega$	1%	1/10 W
$R_R$	22.7 k $\Omega$	1%	1/10 W
$R_T$	51 k $\Omega$	1%	1/10 W
$R_{RX}$	51 k $\Omega$	1%	1/10 W
$R_{TX}$	3.6 k $\Omega$	1%	1/10 W
$R_B$	6.2 k $\Omega$	1%	1/10 W
$R_1$	604 k $\Omega$	1%	1/10 W
$R_2$	604 k $\Omega$	1%	1/10 W
$R_3$	249 k $\Omega$	1%	1/10 W
$R_4$	280 k $\Omega$	1%	1/10 W
$R_{RT}$	330 $\Omega$	5%	2 W
$R_{F1}, R_{F2}$	Line resistor, 40 $\Omega$	1%	–

**Table 7 Capacitors**

Capacitor	Value	Tolerance	Specification
$C_{VB}$	100 nF	10%	100 V
$C_{VB2}$	150 nF	10%	100 V
$C_{TC}$	2.2 nF	10%	100 V
$C_{RC}$	2.2 nF	10%	100 V
$C_{HP}$	47 nF	10%	100 V
$C_{VCC}$	100 nF	10%	10 V
$C_{LP}$	150 nF	10%	100 V
$C_{TX}$	100 nF	10%	10 V
$C_{GG}$	220 nF	10%	100 V

**Table 7 Capacitors (cont'd)**

Capacitor	Value	Tolerance	Specification
$C_1$	330 nF	10%	63 V
$C_2$	330 nF	10%	63 V

**Table 8 Diodes**

Diode	Value	Tolerance	Specification
$D_{VB}$	1N4448		
$D_{VB2}$	1N4448		
$D_{BB}$	1N4448		
$D_{HP}$	1N4448 <sup>1)</sup>		

1) It is required to connect  $D_{HP}$  between terminals HP and ground if  $C_{HP} > 47$  nF

## OVP

Secondary protection (Bournes TISP PBL2). The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferably to a ground plane.

## 4.2 Design Supporting Tools

The following supporting tools are available for the PBL 38640/2:

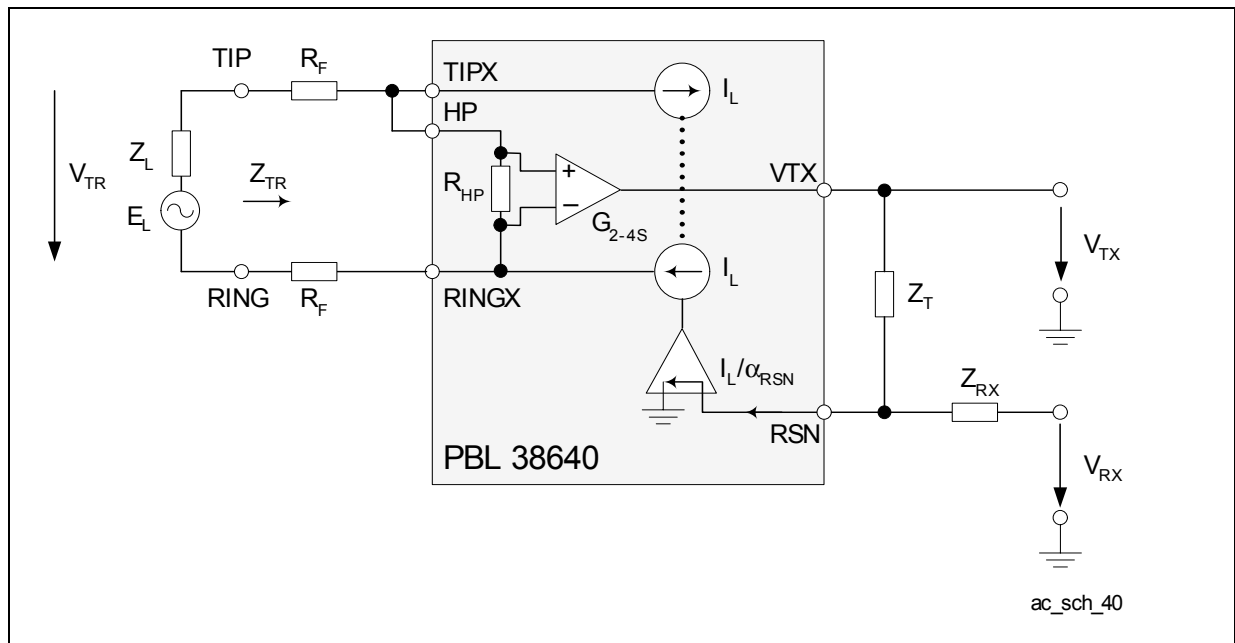
- Test board TB208 for PLCC package
- Test board TB208SSOP for SSOP package
- Pspice model for PBL 38640/2



## 5 Transmission

### 5.1 General

A simplified AC model of the transmission circuit is shown in **Figure 10**.



**Figure 10** Simplified AC Model of PBL 38640/2

Circuit analysis from the AC model in **Figure 10** yields following equations:

$$V_{TR} = \frac{V_{TX}}{G_{2-4S}} + I_L \times 2R_F \quad [1]$$

$$\frac{I_L}{\alpha_{RSN}} = \frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} \quad [2]$$

$$V_{TR} = E_L - I_L \times Z_L \quad [3]$$

where:

$V_{TX}$	Is the ground referenced version of the AC metallic voltage between the TIPX and RINGX terminals.
$V_{TR}$	Is the AC metallic voltage between TIP and RING.
$E_L$	Is the line open circuit AC metallic voltage.
$I_L$	Is the AC metallic current.
$R_F$	Is a fuse resistor.
$G_{2-4S}$	Is the programmable SLIC two-wire to four-wire gain (transmit direction) <sup>1)</sup> .
$Z_L$	Is the line impedance.
$Z_{RX}$	Controls four- to two-wire gain.
$Z_T$	Determines the SLIC TIPX to RINGX impedance at voice frequencies.
$V_{RX}$	Is the analog ground referenced receive signal.
$\alpha_{RSN}$	Is the receive summing node current to metallic loop current gain. $\alpha_{RSN} = 200$

1) The SLIC two-wire to four-wire gain,  $G_{2-4S}$ , is user programmable between two fixed values. See [Table 5](#).

## 5.2 Two-Wire Impedance

To calculate  $Z_{TR}$ , the impedance presented to the two-wire line by the SLIC including the fuse resistor  $R_F$ , let  $V_{RX} = 0$ .

From [Equation \[1\]](#) and [Equation \[2\]](#):

$$Z_{TR} = \frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F \quad [4]$$

Thus with  $Z_{TR}$ ,  $G_{2-4S}$ ,  $\alpha_{RSN}$  and  $R_F$  known:

$$Z_T = \alpha_{RSN} \times G_{2-4S} \times (Z_{TR} - 2R_F) \quad [5]$$

## 5.3 Two-Wire to Four-Wire Gain

From [Equation \[1\]](#) and [Equation \[2\]](#) with  $V_{RX} = 0$ :

$$G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T / \alpha_{RSN}}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F} \quad [6]$$

## 5.4 Four-Wire to Two-Wire Gain

From [Equation \[1\]](#) to [Equation \[3\]](#) with  $E_L = 0$ :

$$G_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \times \frac{1}{G_{2-4S}} \times \frac{Z_L}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_F} \quad [7]$$

For applications where

$$\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F = Z_L \quad [8]$$

the expression for  $G_{4-2}$  simplifies to:

$$G_{4-2} = -\frac{Z_T}{Z_{RX}} \times \frac{1}{2 \times G_{2-4S}} \quad [9]$$

## 5.5 Four-Wire to Four-Wire Gain

From [Equation \[1\]](#) to [Equation \[3\]](#) with  $E_L = 0$ :

$$G_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \times \frac{Z_L + 2R_F}{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_F} \quad [10]$$

## 5.6 Hybrid Function

The hybrid function can easily be implemented utilizing the uncommitted amplifier in conventional non software programmable codec/filters. Please, refer to [Figure 11](#). Via impedance  $Z_B$  a current proportional to  $V_{RX}$  is injected into the summing node of the combination codec/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain,  $G_{4-4}$ , a voltage proportional to  $V_{RX}$  is returned to  $V_{TX}$ . This voltage is converted by  $R_{TX}$  to a current flowing into the same summing node. These currents can be cancelled by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \quad (E_L = 0) \quad [11]$$

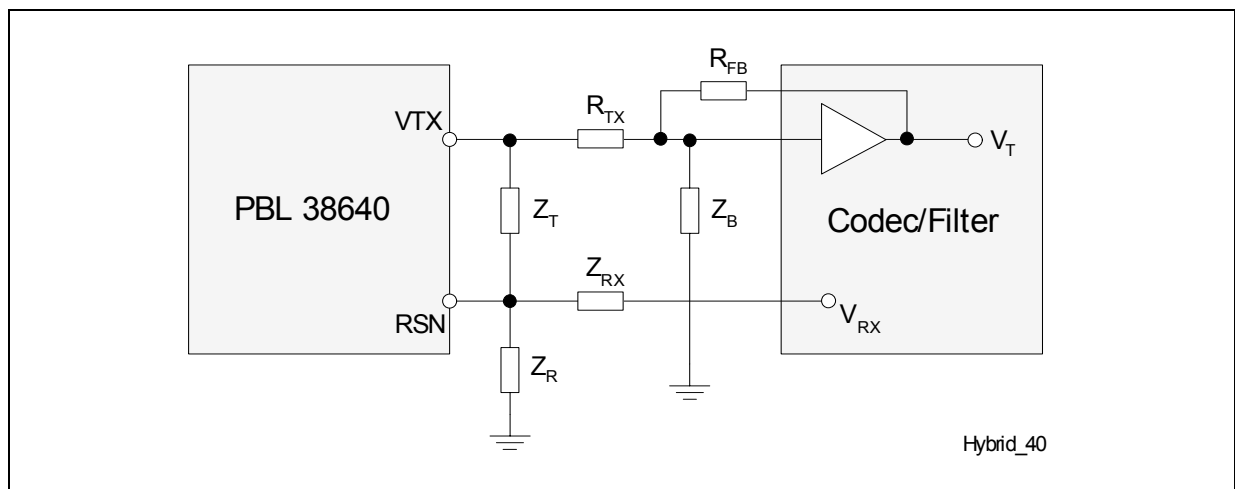
The four-wire to four-wire gain,  $G_{4-4}$ , includes the required phase shift and thus the balance network  $Z_B$  can be calculated from:

$$Z_B = -R_{TX} \times \frac{V_{RX}}{V_{TX}} = R_{TX} \times \frac{Z_{RX}}{Z_T} \times \frac{\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + Z_L + 2R_F}{Z_L + 2R_F} \quad [12]$$

When selecting the  $R_{TX}$  resistance value, make sure the load resistance on the  $V_{TX}$  terminal is at least 20 k $\Omega$ .

If calculation of the  $Z_B$  formula above yields a balance network containing an inductor, please contact Infineon's support group for assistance.

The PBL 38640/2 SLIC may also be used together with programmable CODEC/filters. The programmable CODEC/filter allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the transmit and receive gain may be adjusted. Please, refer to the programmable CODEC/filter data sheets for design information.



**Figure 11 Hybrid Function**

## 5.7 Longitudinal Impedance

A feedback loop within the SLIC counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range.

The SLIC longitudinal impedance per wire,  $Z_{LOT}$  and  $Z_{LOR}$ , appears as typically  $20\ \Omega$  to longitudinal disturbances. It should be noted that longitudinal currents may exceed the DC loop current without disturbing the VF transmission.

## 5.8 Capacitors $C_{TC}$ and $C_{RC}$

The capacitors designated  $C_{TC}$  and  $C_{RC}$  in **Figure 9**, connected between TIPX and ground as well as between RINGX and ground, can be used for RFI filtering. The recommended value for  $C_{TC}$  and  $C_{RC}$  is 2200 pF. Higher capacitance values may be used, but care must be taken to prevent degradation of either longitudinal balance or return loss.  $C_{TC}$  and  $C_{RC}$  contribute to a metallic impedance of  $1/(\pi \times f \times C_{TC}) = 1/(\pi \times f \times C_{RC})$ , a TIPX to ground impedance of  $1/(2\pi \times f \times C_{TC})$  and a RINGX to ground impedance of  $1/(2\pi \times f \times C_{RC})$ .

## 5.9 AC - DC Separation Capacitor, $C_{HP}$

The high pass filter capacitor connected between terminals HP and TIPX provides the separation of the AC and DC signals, such that only AC signals are forwarded to the VTX terminal.  $C_{HP}$  positions the low end frequency response break point of the AC feedback loop in the SLIC. A  $C_{HP}$  value of 150 nF will position the low end frequency response 3 dB break point of the AC loop at 1.8 Hz ( $f_{3dB}$ ) according to  $f_{3dB} = 1/(2\pi \times R_{HP} \times C_{HP})$  where  $R_{HP} = 600\ k\Omega$  (see **Table 9**).

## 5.10 High-pass Transmit Filter

The capacitor  $C_{TX}$  in **Figure 9** connected between the VTX output and the CODEC/filter forms, together with  $R_{TX}$  and/or the input impedance of a programmable CODEC/filter, a high-pass RC filter. It is recommended to position the 3 dB break point of this filter between 30 and 80 Hz to get a faster response for the DC steps that may occur at DTMF signalling.

## 5.11 Capacitor $C_{LP}$

The capacitor  $C_{LP}$ , which connects between the terminals LP and VBAT, positions the high end frequency break point of the low pass filter in the DC feedback loop (battery feed controlling loop) of the SLIC.  $C_{LP}$  together with  $C_{HP}$  and  $Z_T$  (see **Chapter 5.2**) forms the total two-wire output impedance of the SLIC. The choice of these programmable

components have an influence on the power supply rejection ratio (PSRR) from  $V_{BAT}$  to the two-wire side at sub audio frequencies. At these frequencies  $C_{LP}$  also influences the transversal to longitudinal balance in the SLIC. **Table 9** suggests a suitable value for  $C_{LP}$ . The typical value of the transversal to longitudinal balance at 200 Hz is given in the table below, for the chosen value of  $C_{LP}$ .

**Table 9 Feeding Setup**

Symbol	Value				Unit
$R_{Feed}$	2 x 50	2 x 200	2 x 400	2 x 800	$\Omega$
$R_{SG}$	0	60.4	147	301	k $\Omega$
$C_{LP}$	150	100	47	22	nF
T-L bal. @ 200 Hz	-46	-46	-43	-36	dB
$C_{HP}$	47	150	150	150	nF

## 6 Battery Feed

The PBL 38640/2 SLIC emulates resistive loop feed, programmable between 2x50  $\Omega$  and 2x900  $\Omega$ , with adjustable current limitation. In the current limited region the loop current has a slight slope corresponding to 2x30  $\Omega$ , see **Figure 13** reference B.

The open loop voltage measured between the TIPX and RINGX terminals tracks the battery voltage  $V_{BAT}$ . The signalling headroom, or overhead voltage  $V_{TRO}$ , is programmable with a resistor  $R_{OV}$  connected between terminal POV on the SLIC and ground. Please refer to **Chapter 6.2**. The battery voltage overhead,  $V_{OH}$ , depends on the programmed signal overhead voltage  $V_{TRO}$ .  $V_{OH}$  defines the TIP and RING voltage at open loop conditions according to

$$V_{TR}(at I_L = 0 \text{ mA}) = |V_{BAT}| - V_{OH}$$

Refer to **Table 10** for the typical value of  $V_{OH}$  and  $V_{OHvirt}$ . The overhead voltage is changed when line current is approaching open loop conditions. To ensure maximum open loop voltage, even with a leaking telephone line, this occurs at a line current of approximately 6 mA. When the overhead voltage has changed, the line voltage is kept nearly constant with a steep slope corresponding to 2x25  $\Omega$  (reference G in **Figure 13**). The virtual battery overhead,  $V_{OHvirt}$ , is defined as the difference between the battery voltage and the crossing point of all possible resistive feeding slopes, see **Figure 13** reference J. The virtual battery overhead is a theoretical constant needed to be able to calculate the feeding characteristics.

**Table 10 Battery Overhead**

Symbol	Value (typ)	Unit	Specification
$V_{OH}$	$3.0 + V_{TRO}$	V	–
$V_{OHvirt}$	$4.9 + V_{TRO}$	V	–

The resistive loop feed (reference D in [Figure 13](#)) is programmed by connecting a resistor,  $R_{SG}$ , between terminals PSG and  $V_{BAT}$  according to the equation:

$$R_{Feed} = \frac{R_{SG} + 2 \times 10^4}{200} + 2R_F \quad [13]$$

where  $R_{Feed}$  is in  $\Omega$  for  $R_{SG}$  and  $R_F$  in  $\Omega$ .

The current limit (reference C in [Figure 13](#)) is adjusted by connecting a resistor,  $R_{LC}$ , between terminal PLC and ground according to the equation:

$$I_{LProg} = \frac{1000}{R_{LC}} - 4.0 \quad [14]$$

where  $R_{LC}$  is in  $k\Omega$  for  $I_{LProg}$  in mA.

A second lower battery voltage may be connected to the device at terminal  $V_{BAT2}$  to reduce short loop power dissipation.

The SLIC automatically switches between the two battery supply voltages without need for external control. the silent battery switching occurs when the line voltage passes the value  $|VB2| - 40 \times I_L - (V_{OHvirt} - 1.3)$ , if  $I_L > 6$  mA.

For correct functionality it is important to connect the terminal  $V_{BAT2}$  to the second power supply via the diode  $D_{VB2}$ , see [Figure 9](#). An optional diode  $D_{BB}$  connected between terminal VB and the VB2 power supply, see [Figure 9](#), will make sure that the SLIC continues to work on the second battery even if the first battery voltage disappears. If a second battery voltage is not used,  $V_{BAT2}$  is connected to  $V_{BAT}$  on the SLIC and  $C_{VB2}$ ,  $D_{BB}$  and  $D_{VB2}$  are removed.

## 6.1 CODEC Receive Interface

The PBL 38640/2 SLIC has got a receive interface at the four- wire side which makes it possible to reduce the number of capacitors in the applications and to fit both single and dual battery feed CODECs. The RSN terminal, connecting to the CODEC receive output via the resistor  $R_{RX}$ , is DC biased with +1.25 V. This makes it possible to compensate for currents floating due to DC voltage differences between RSN and the CODEC output without using any capacitors. This is done by connecting a resistor  $R_R$  between the RSN

terminal and ground. With current directions defined as in **Figure 13**, current summation gives:

$$-I_{RSN} = I_{RT} + I_{RRX} + I_{RR} = \frac{1.25}{R_T} + \frac{1.25 - V_{CODEC}}{R_{RX}} + \frac{1.25}{R_R} \quad [15]$$

where  $V_{CODEC}$  is the reference voltage of the CODEC at the receive output. From this equation the resistor  $R_R$  can be calculated as

$$R_R = \frac{1.25}{-I_{RSN} - \frac{1.25}{R_T} - \frac{1.25 - V_{CODEC}}{R_{RX}}} \quad [16]$$

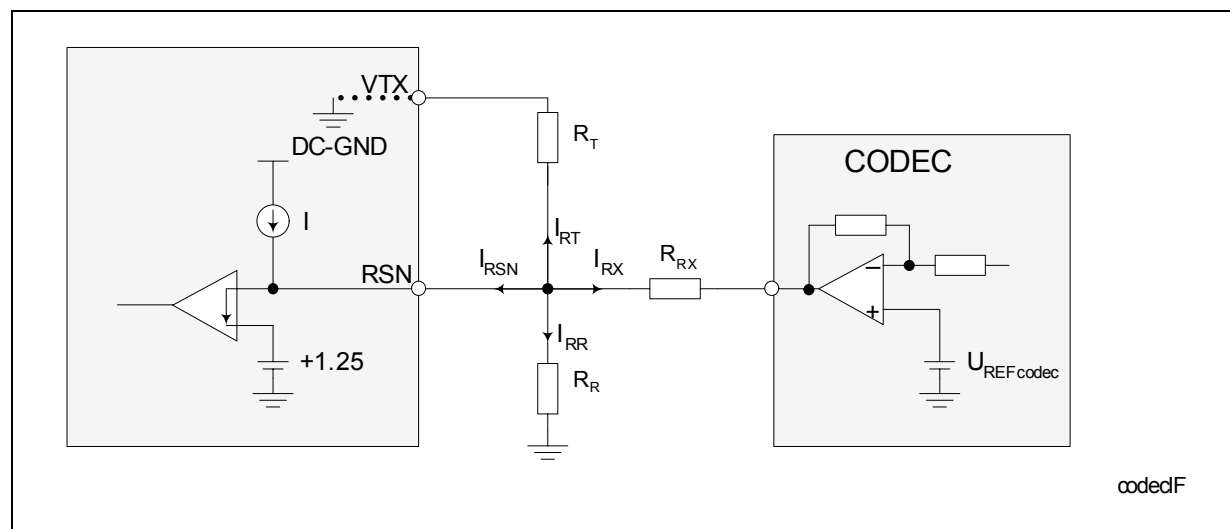
For the value on  $I_{RSN}$ , see **Table 11**.

If RSN is DC decoupled from the CODEC output, then  $R_{RX}$  can be considered to be infinite.

The resistor  $R_R$  has no influence in the AC transmission.

**Table 11 Internal Bias Current of RSN**

Symbol	Value (typ)	Unit
$I_{RSN}$	-55	$\mu\text{A}$



**Figure 12 Codec Receive Interface**



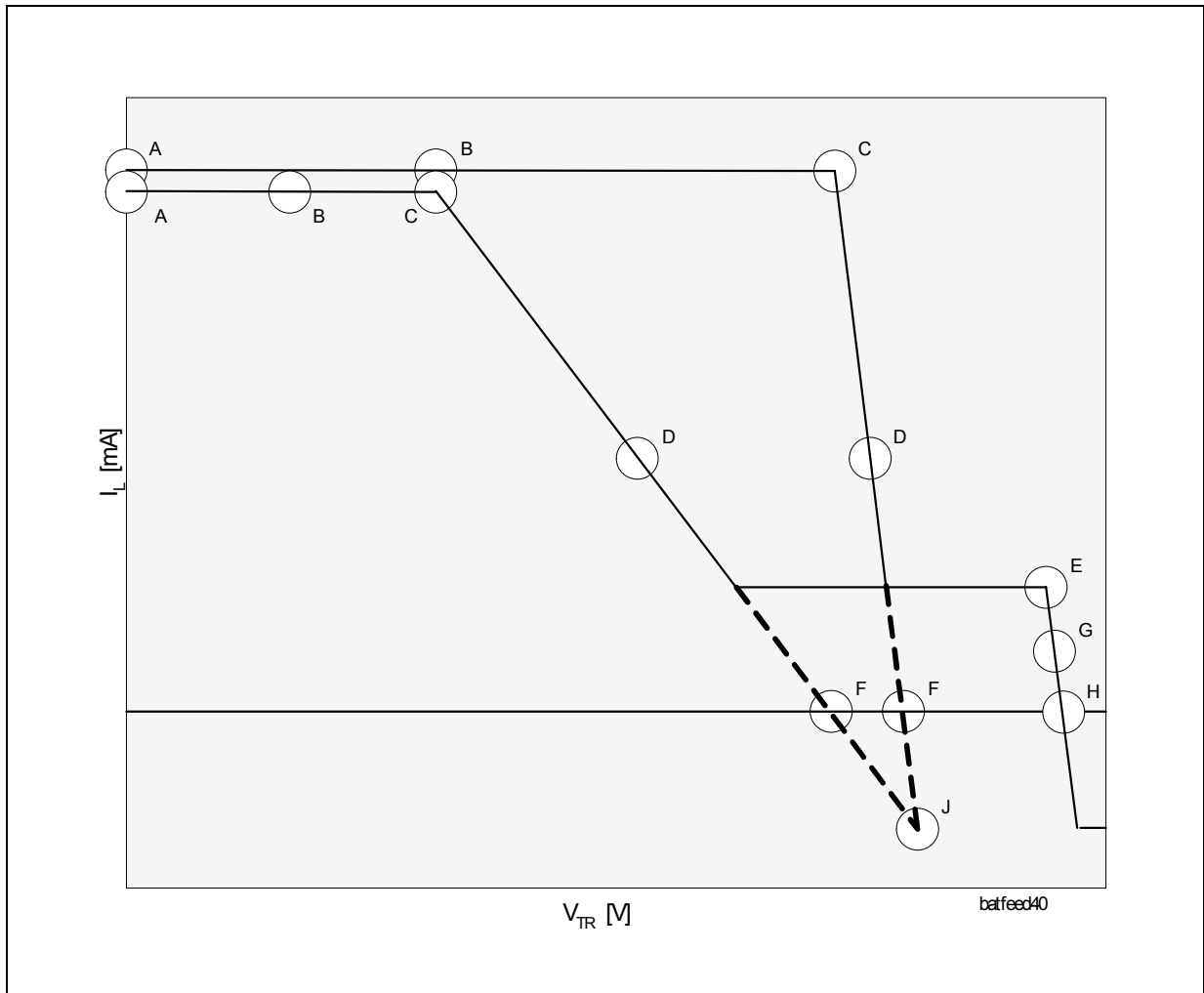


Figure 13 Battery Feed Characteristics

A	$I_L(V_{TR} = 0V) = I_{LProg} + \frac{ V_{Bat}  - V_{OHvirt} - R_{Feed} \times (I_{LProg} + 4 \times 10^{-3})}{60 \times 10^3}$
B	$R_{Feed} = 2 \times 30 \text{ k}\Omega$
C	$I_{LConst}(typ) = I_{LProg} = \frac{10^3}{R_{LC}} - 4 \times 10^{-3}$ $V_{TR} =  V_{BAT}  - V_{OHvirt} - R_{Feed} \times (I_{LProg} + 4 \times 10^{-3})$

D	$R_{\text{Feed}} = \frac{R_{\text{SG}} + 2 \times 10^4}{200} + 2R_{\text{F}}$
E	$I_{\text{L}} = 6 \text{ mA}$
F	Apparent battery $V_{\text{Bat}} (@ I_{\text{L}} = 0) =  V_{\text{BAT}}  - V_{\text{OHvirt}} - (R_{\text{Feed}} \times 4 \times 10^{-3})$
G	$R_{\text{Feed}} = 2 \times 25 \ \Omega$
H	$V_{\text{TROpen}} =  V_{\text{BAT}}  - V_{\text{OH}}$
J	Virtual battery $V_{\text{BatVirt}} (@ I_{\text{L}} = 4 \text{ mA}) =  V_{\text{BAT}}  - V_{\text{OHvirt}}$

## 6.2 Programmable Overhead Voltage (POV)

With the POV function the overhead voltage can be increased. If the POV pin is left open the overhead voltage is internally set to  $3.2 V_{Peak}$  in off-hook and  $1.3 V_{Peak}$  on-hook.. If a resistor  $R_{OV}$  is connected between the POV pin and AGND, the overhead voltage can be set to higher values, typical values can be seen in **Figure 14**. The  $R_{OV}$  and corresponding  $V_{TRO}$  (signal headroom) are typical values for THD < 1% and the signal frequency 1000 Hz.

Observe that the four-wire output terminal  $V_{TX}$  cannot handle more than  $3.2 V_{Peak}$ . So if the two- to four-wire gain is 0 dB,  $3.2 V_{Peak}$  is maximum also for the two-wire side. Signal levels between  $3.2$  and  $6.4 V_{Peak}$  on the two-wire side can be handled with the PTG shorted so that the gain  $G_{2-4S}$  becomes -6.02 dB. Please note that:

- $Z_T$
- $R_R$
- $G_{4-4}$

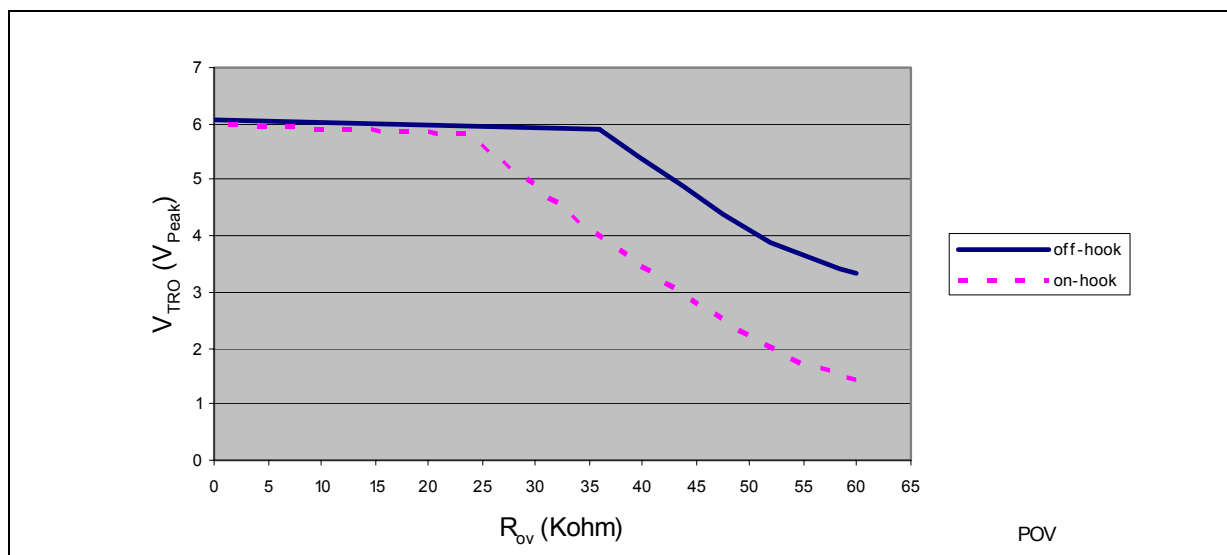
has to be recalculated if the PTG is shorted.

Please note that the maximum signal current at the two-wire side can not be higher than 9 mA.

How to use POV:

1. Decide what overhead voltage ( $V_{TRO}$ ) is needed. The POV function is only needed if the overhead voltage exceeds  $3.2 V_{Peak}$ .
2. In **Figure 14** the corresponding  $R_{OV}$  for the decided  $V_{TRO}$  can be found.

If the overhead voltage exceeds  $3.2 V_{Peak}$ , the  $G_{2-4S}$  gain has to be changed to -6.02 dB by connecting pin PTG to AGND. Please note, that the 2-wire impedance,  $R_R$  and the 4-wire to 4-wire gain has to be recalculated.



**Figure 14 Programmable Overhead Voltage (POV).  $R_L = 600 \Omega$  or Infinite**

### 6.3 Analog Temperature Guard

The widely varying environmental conditions in which SLICs operate may lead to the chip temperature limitations being exceeded. The PBL 38640/2 SLIC reduces the DC line current when the chip temperature reaches approximately 145 °C and increases line current again automatically when the temperature drops. Accordingly transmission is not lost under high ambient temperature conditions.

The detector output, DET, is forced to a logic low level when the temperature guard is active.

## 7 Loop Monitoring Functions

The loop current, ground key and ring-trip detectors report their status through a common output, DET. The particular detector to be connected to the detector pin, DET, is selected via the three bit control interface C1, C2 and C3. Please refer to Chapter 9 for a description of the control interface.

### 7.1 Loop Current Detector

The loop current detector indicates that the telephone is off-hook and that DC current is flowing in the loop by setting the output pin DET to a logic low level when selected. The loop current detector threshold value,  $I_{LTh}$ , where the loop current detector changes state, is programmable with the  $R_{LD}$  resistor.  $R_{LD}$  connects between pin PLD and ground and is calculated according to:

$$R_{LD} = \frac{500}{I_{LTh}} \quad [17]$$

The loop current detector is internally filtered and is not influenced by the AC signal at the two-wire side.

### 7.2 Ground Key Detector

The ground key detector indicates when the ground key is pressed (active) by setting the output pin DET to a logical high level when selected. The ground key detector circuit senses the difference in TIPX and RINGX currents. When the current at the RINGX side exceeds the current at the TIPX side with the threshold value the detector is triggered. For threshold current values, please refer to the datasheet.

### 7.3 Ring Trip Detector

Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR. The ringing source can be balanced or unbalanced superimposed on  $V_B$  or GND. The unbalanced ringing source may be applied to either

the ring lead or the tip lead with return via the other wire. A ring relay driven by the SLIC ring relay driver connects the ringing source to tip and ring.

The ring trip function is based on a polarity change at the comparator input when the line goes off-hook. In the on-hook state no DC current flows through the loop and the voltage at comparator input DT is more positive than the voltage at input DR. When the line goes off-hook, while the ring relay is energized, DC current flows and the comparator input voltage reverses polarity.

**Figure 9** gives an example of a ring trip detector network. This network is applicable when the ring voltage is superimposed on  $V_B$  and is injected on the ring lead of the two-wire port. The DC voltage across sense resistor  $R_{RT}$  is monitored by the ring trip comparator input DT and DR via the network  $R_1, R_2, R_3, R_4, C_1$  and  $C_2$ .

When the line is on-hook (no DC current), DT is more positive than DR and the DET output will report logic level high, that is the detector is not tripped. When the line goes off-hook, while ringing, a DC current will flow through the loop including sense resistor  $R_{RT}$  and will cause input DT to become more negative than input DR. This changes output DET to logic level low, that is tripped detector conditions. The system controller (or line card processor) responds by de-energizing the ring relay, that is ring trip.

Complete filtering of the 20 Hz AC component at terminal DT and DR is not necessary. A toggling DET output can be examined by a software routine to determine the duty cycle. When the DET output is at logic level low for more than half the time, off-hook conditions is indicated.

## 8 Relay Driver

The PBL 38640/2 SLIC incorporates a ring relay driver designed as open collector (nnp), with a current sinking capability of 50 mA. The drive transistor emitter is connected to BGND. The relay driver has an internal zener diode clamp for inductive kick back voltages.

## 9 Control Inputs

The SLIC has three digital control inputs, C1, C2 and C3 (see **Table 2**). A decoder in the SLIC interprets the control input condition and sets up the commanded operating state. C1, C2 and C3 are internally pulled up.

### 9.1 Open Circuit (C3, C2, C1 = 0, 0, 0)

In the Open Circuit state, the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum and no detectors are active. DET output is set high.

## 9.2 Ringing (C3, C2, C1 = 0, 0, 1)

The ring relay driver and the ring trip detector are activated and the ring trip detector is indicating off-hook with a logic low level at the detector output. The SLIC is in the active normal state.

## 9.3 Active States

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. VF signal transmission is normal. The loop current or ground key detector is activated. The loop current detector is indicating off hook with a logic low level and the ground key detector is indicating active ground key with a logic high level present at the detector output.

In PBL 38640/2 SLIC a line voltage measurement feature is available in the active state, which may be used for line length estimations or for line test purposes. The line voltage is presented on the detector output as a pulse at logic high level with a pulsewidth of 5.5  $\mu\text{s}/\text{V}$ . To start the line voltage measurement this mode has to be entered from the active state with the loop or ground key detector active. The pulse presented at the DET output proportional to the line voltage starts when entering the line voltage measuring mode.

## 9.4 Tip Open State

Tip open state is used for ground start signalling. In this state the SLICs present a high impedance to the line on the TIPX pin and the programmed DC characteristics, with the longitudinal current compensation (see [Chapter 5.7](#)) not active, to the line on the RINGX pin. The loop current detector is active.

## 9.5 Active Polarity Reversal State

TIPX and RINGX polarity is reversed from the active state: RINGX is the terminal closest to ground and sources loop current while TIPX is the more negative terminal and sinks current. VF signal transmission is normal. The loop current or the ground key detector is activated. The loop current detector is indicating off hook with a logic low level and the ground key detector is indicating active ground key with a logic high level present at the detector output.

# 10 Overvoltage Protection

## 10.1 Overvoltage Protection - General

The SLIC must be protected against foreign voltages on the telephone line. Overvoltages can result from lightning, AC power contact, induction and other causes.

Refer to **Table 3**, TIPX and RINGX terminals, for maximum continuous and transient voltages that may be applied to the SLIC.

## 10.2 Secondary Protection

The circuit shown in **Figure 9** utilizes series resistors ( $R_{F1}$ ,  $R_{F2}$ ) together with a programmable overvoltage protector (OVP, for example Bournes TISP PBL2) as secondary protection.

The TISP PBL2 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to the negative supply voltage (that is the battery voltage,  $V_B$ ). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by a diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage and the protector will crowbar into a low voltage on-state condition, by firing an internal thyristor.

A gate decoupling capacitor,  $C_{GG}$ , is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector.  $C_{GG}$  should be placed close to the overvoltage protection device. Without the capacitor even the low inductance in the track to the  $V_B$  supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors  $R_F$  serve the dual purposes of being non-destructive energy dissipators when transients are clamped, and of being fuses when the line is exposed to a power cross. If a PTC is chosen for  $R_F$ , note that it is important to always use PTC's in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore will not protect the SLIC.

## 11 Power-Up Sequence

No special power-up sequence is necessary, except that ground has to be present before all other power supply voltages.

## 12 Printed Circuit Board Layout

Care in Printed Circuit Board (PCB) layout is essential for proper function. The components connected to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the receive summing node (RSN). Ground plane surrounding the RSN pin is advisable.

Analog Ground (AGND) should be connected to Battery Ground (BGND) on the PCB, in one point. The capacitors for the battery should be connected with short wide leads of the same length.

## 13 Package Outlines

The SLIC is provided in three different packages: 24-pin SSOP, 24-pin PDSO and 28-pin PLCC.

### 13.1 24-pin SSOP Package

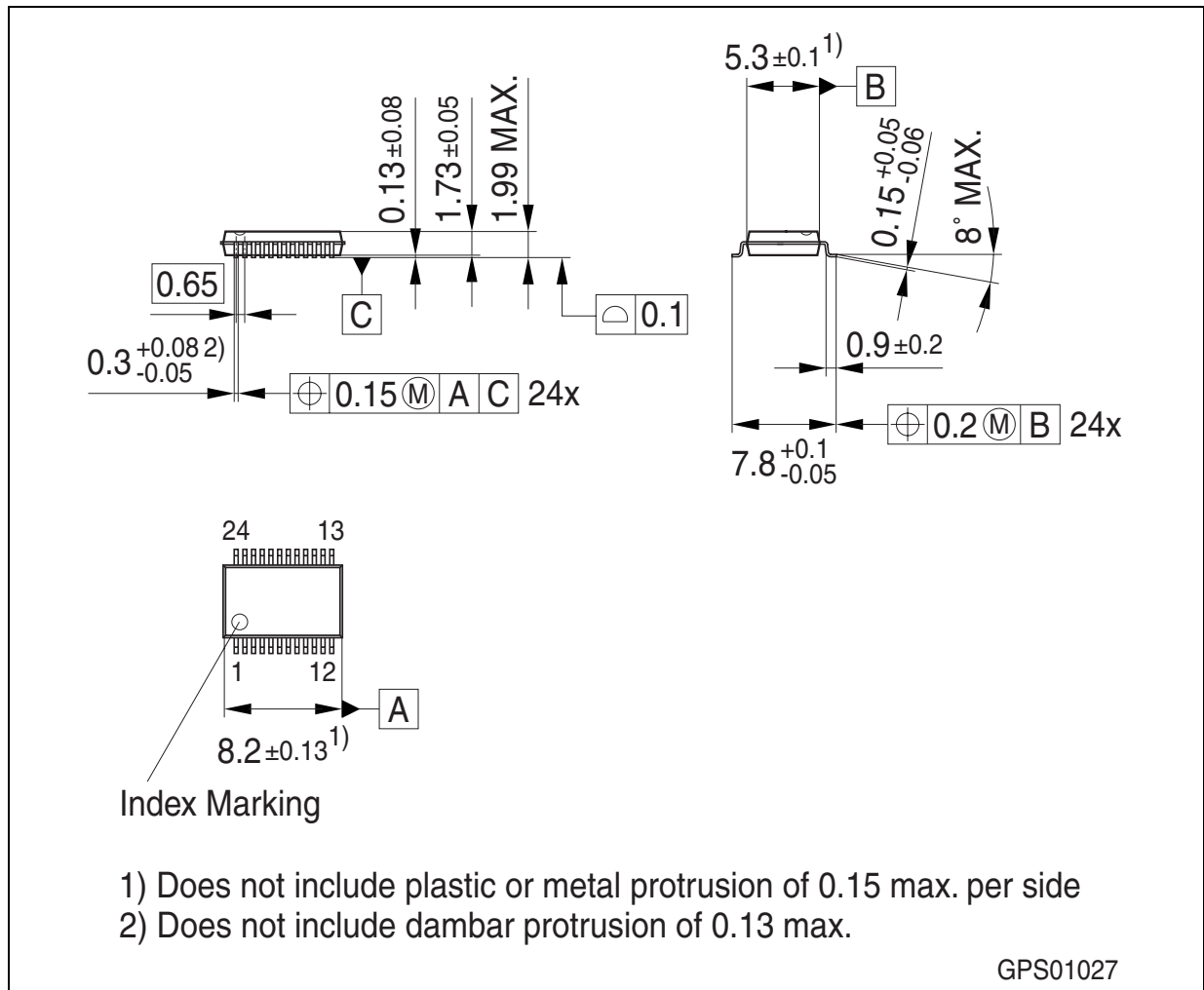


Figure 15 P-/PG-SSOP-24-1 (Plastic Shrink Small Outline Package)

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SMD = Surface Mounted Device

Dimensions in mm



### 13.2 24-pin PDSO Package

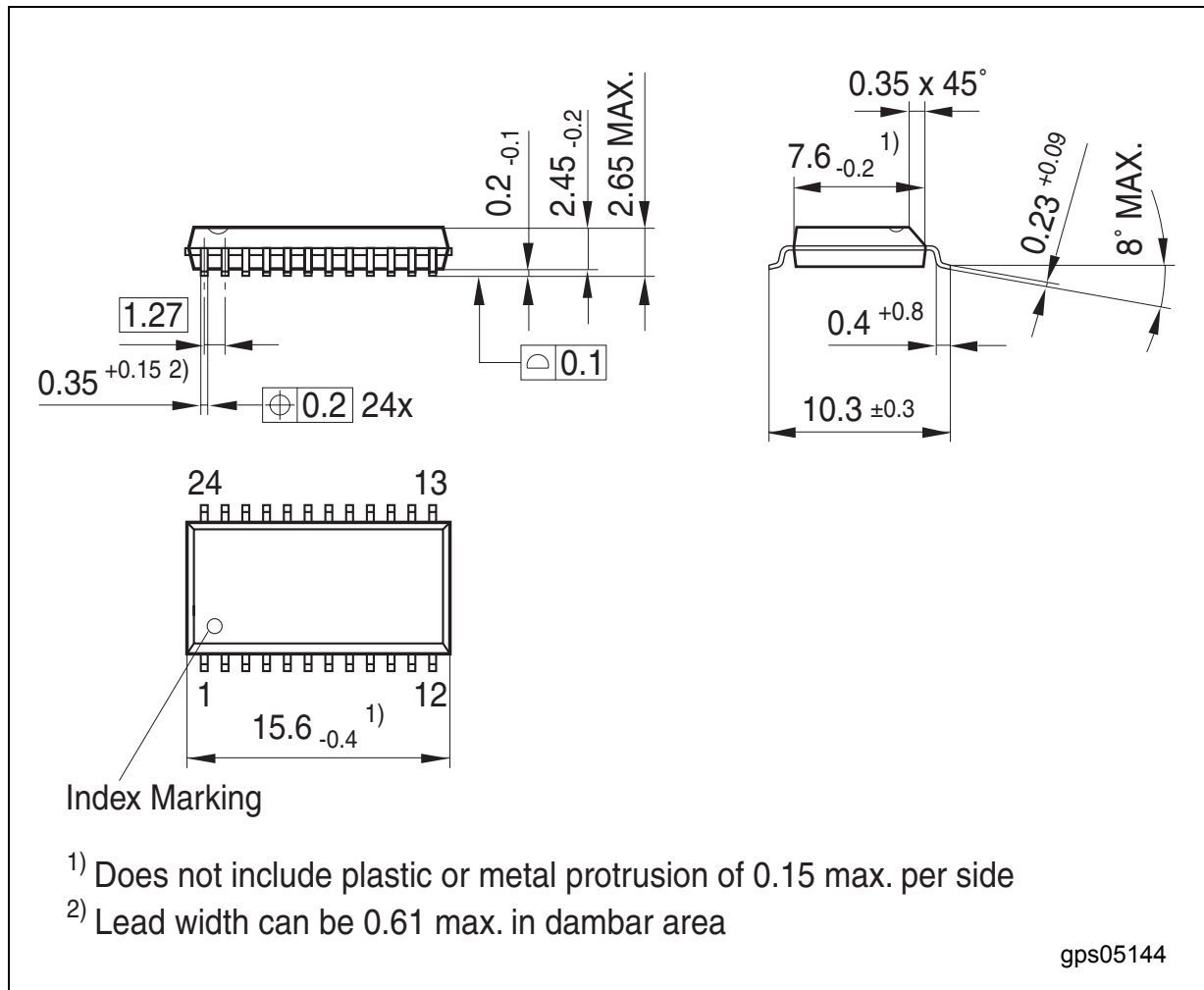


Figure 16 P-/PG-DSO-24-8 (Plastic Dual Small Outline Package)

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SMD = Surface Mounted Device

Dimensions in mm

### 13.3 28-pin PLCC Package

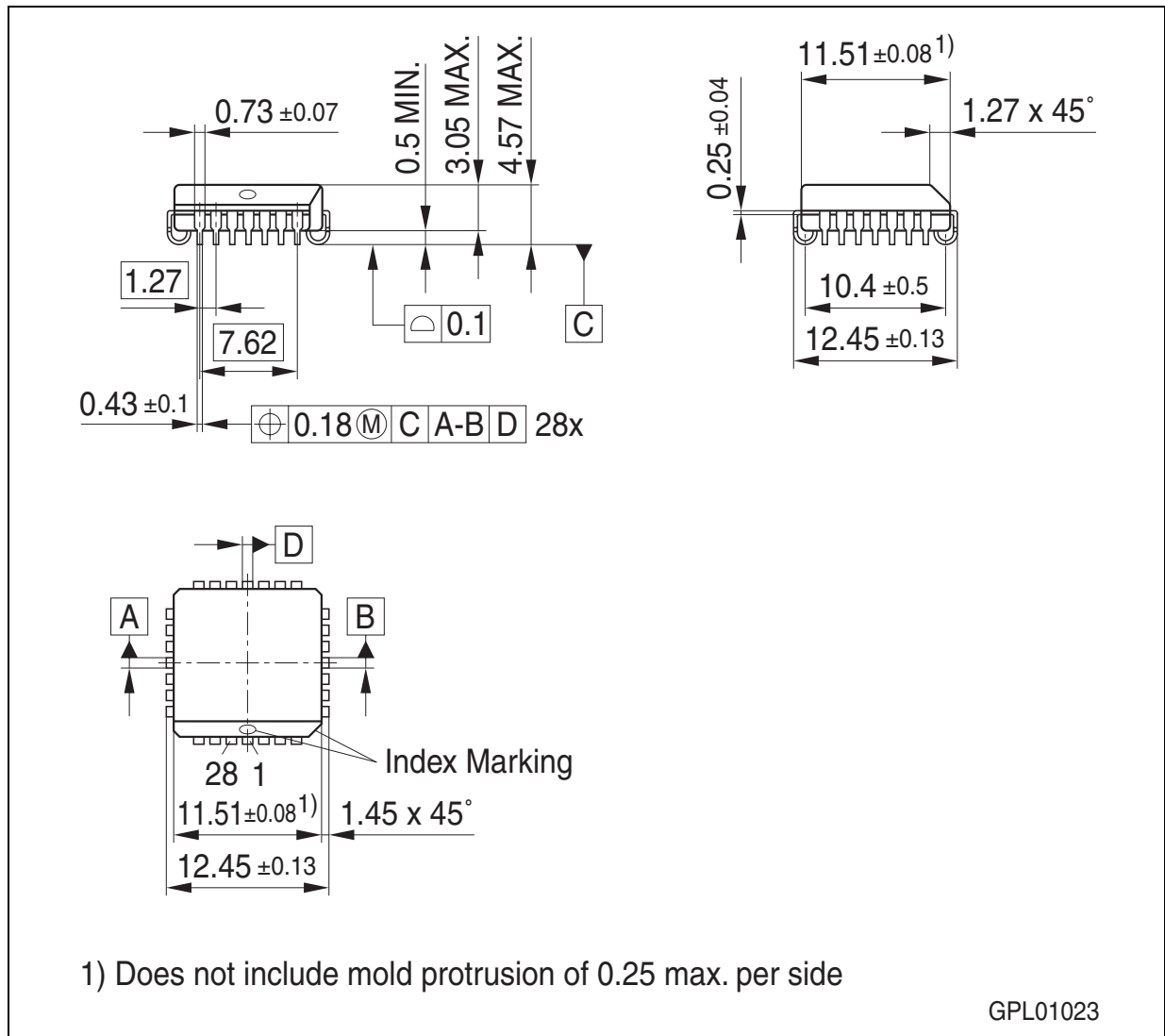


Figure 17 P-/PG-LCC-28-3 (Plastic Leaded Chip Carrier Package)

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SMD = Surface Mounted Device

Dimensions in mm

<http://www.infineon.com>

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