

MC92501

Advance Information ATM Cell Processor

The MC92501 is an Asynchronous Transfer Mode (ATM) Cell Processor layer device composed of dedicated high-performance ingress and egress cell processors combined with UTOPIA Level 2-compliant physical (PHY) and UTOPIA Level 1-compliant switch interface (see **Figure 1**). It integrates address translation, UPC/NPC, OAM, and statistical functions into a single semiconductor device. This second generation ATM cell processor in Motorola's MC92500 series can be used both in the line cards used by the switching systems in the ATM network core and in the access multiplexer. The primary function of the MC92501 in either application is to provide ATM-layer cell processing and routing functions. The advanced ATM functionality permits simultaneous transmission of voice, video, and data within broadband services such as high-speed Internet operations, LAN interconnections for commuters, and video-on-demand using a variety of applications such as Digital Subscriber Line Access Multiplexers (DSLAMs), Wide-Area Networks (WANs), Enterprise Switches, and Multi-service Platforms,

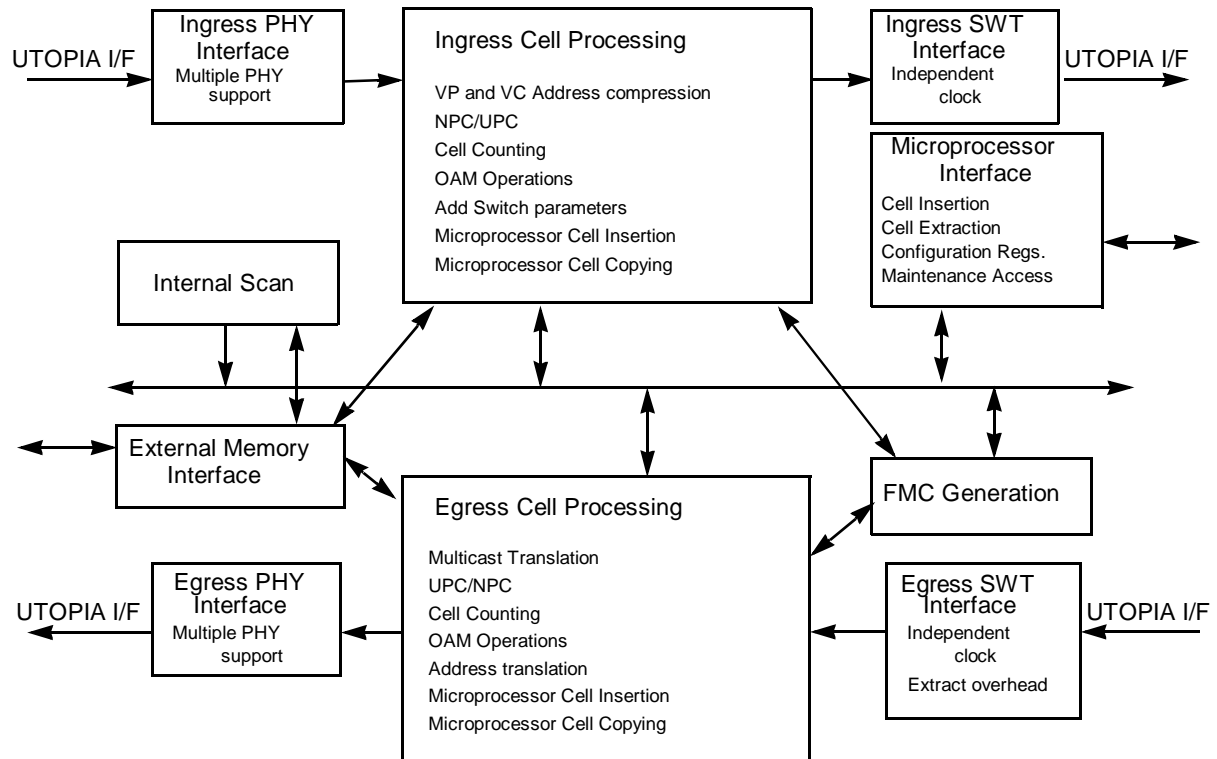


Figure 1. MC92501 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Data Sheet Conventions

This data sheet uses the following conventions:

- OVERBAR Used to indicate a signal that is active when pulled low (For example, the RESET pin is active when low.)
- asserted Means that a high true (active high) signal is high or that a low true (active low) signal is low
- deasserted Means that a high true (active high) signal is low or that a low true (active low) signal is high

| | | | | |
|-----------|-------------------------|-------------|--------------|-----------------|
| Examples: | Signal/Symbol | Logic State | Signal State | Voltage |
| | $\overline{\text{PIN}}$ | True | Asserted | V_{IL}/V_{OL} |
| | $\overline{\text{PIN}}$ | False | Deasserted | V_{IH}/V_{OH} |
| | PIN | True | Asserted | V_{IH}/V_{OH} |
| | PIN | False | Deasserted | V_{IL}/V_{OL} |

Note: Values for V_{IL} , V_{OL} , V_{IH} , and V_{OH} are defined by individual product specifications.

New Features in the MC92501

- Implements ATM Layer functions for Broadband ISDN according to ANSI recommendations, ATM Forum UNI 4.0 and TM 4.0 Specifications, ITU recommendations, and Bellcore recommendations.
- Provides ABR Relative Rate marking and EFCI marking according to TM 4.0
- Select Discard CLP = 1 (or CLP = 0 + 1) Flow on selected connections
- UTOPIA Level 2 PHY Interface and UTOPIA ATM Layer Interface
- Supports both Partial Packet Discard (PPD) and Early Packet Discard (EPD)
- Change ABR RM Cell priority
- Supports CLP transparency
- Unidirectional (Ingress or Egress) UPC or NPC

Standard ATMC Features in the MC92500 Family

- Full duplex operation at data rates up to 155 Mbps
- Performs internal VPI and VCI address compression for up to 64 K VCs
- CLP-Aware peak, average, and burst-length policing with programmable Tag/Drop action per policer
- Supports up to 16 physical links using dedicated Ingress/Egress multiPHY control signals
- Each physical link can be configured as either a UNI or NNI port
- Supports multicast, multiport address translation
- Maintains both virtual connection and physical link counters on both Ingress and Egress cell flows
- Provides a flexible 32-bit external memory port for context management
- Automated AIS, RDI, CC, and loopback functions with performance monitoring block test on all 64 K connections
- Programmable 32-bit microprocessor interface supporting Big-Endian or Little-Endian bus formats
- Unidirectional (Ingress only) UPC or NPC design with up to four leaky buckets per connection
- Supports a programmable number of additional switch overhead parameters allowing adaptation to any switch routing header format
- Provides per-link cell counters in both directions

Product Documentation

The three documents listed in the following table are required for complete description of the MC92501 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

Table 1. MC92501 Documentation

| Name | Description | Order Number |
|--|--|----------------|
| MC92501 Product Brief | MC92501 product overview | MC92501/P |
| MC92501 Technical Data | MC92501 features list and physical, electrical, timing, and package specifications | MC92501/D |
| MC92501 User's Manual | Detailed functional description of the MC92501 configuration, operation, and register programming | MC92501UM/D |
| ATM Cell Processor Evaluation Board User's Manual | Detailed description of the ATMC EVB hardware, operation, installation, and design recommendations | MC92501EVKUM/D |

Signal Descriptions

1.1 Signal Groupings

The input and output signals of the MC92501 are organized into functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**. The MC92501 is operated from a 3.3 V supply; however, some of the inputs can tolerate 5 V. A special note for this feature is added to the signal descriptions of those inputs.

Table 1-1. MC92501 Functional Signal Groupings

| Functional Group | Number of Signals | Detailed Description |
|--|-------------------|----------------------|
| Power (VDD and AVDD) and Ground (VSS and AVSS) | 47 | Table 1-2 |
| Control | 4 | Table 1-3 |
| Processor Interface | 68 | Table 1-4 |
| Ingress PHY Interface | 17 | Table 1-6 |
| Egress PHY Interface | 18 | Table 1-7 |
| PLL | 4 | Table 1-8 |
| External Memory Interface | 64 | Table 1-9 |
| Ingress Switch Interface | 13 | Table 1-10 |
| Egress Switch Interface | 13 | Table 1-11 |
| JTAG Interface | 5 | Table 1-12 |

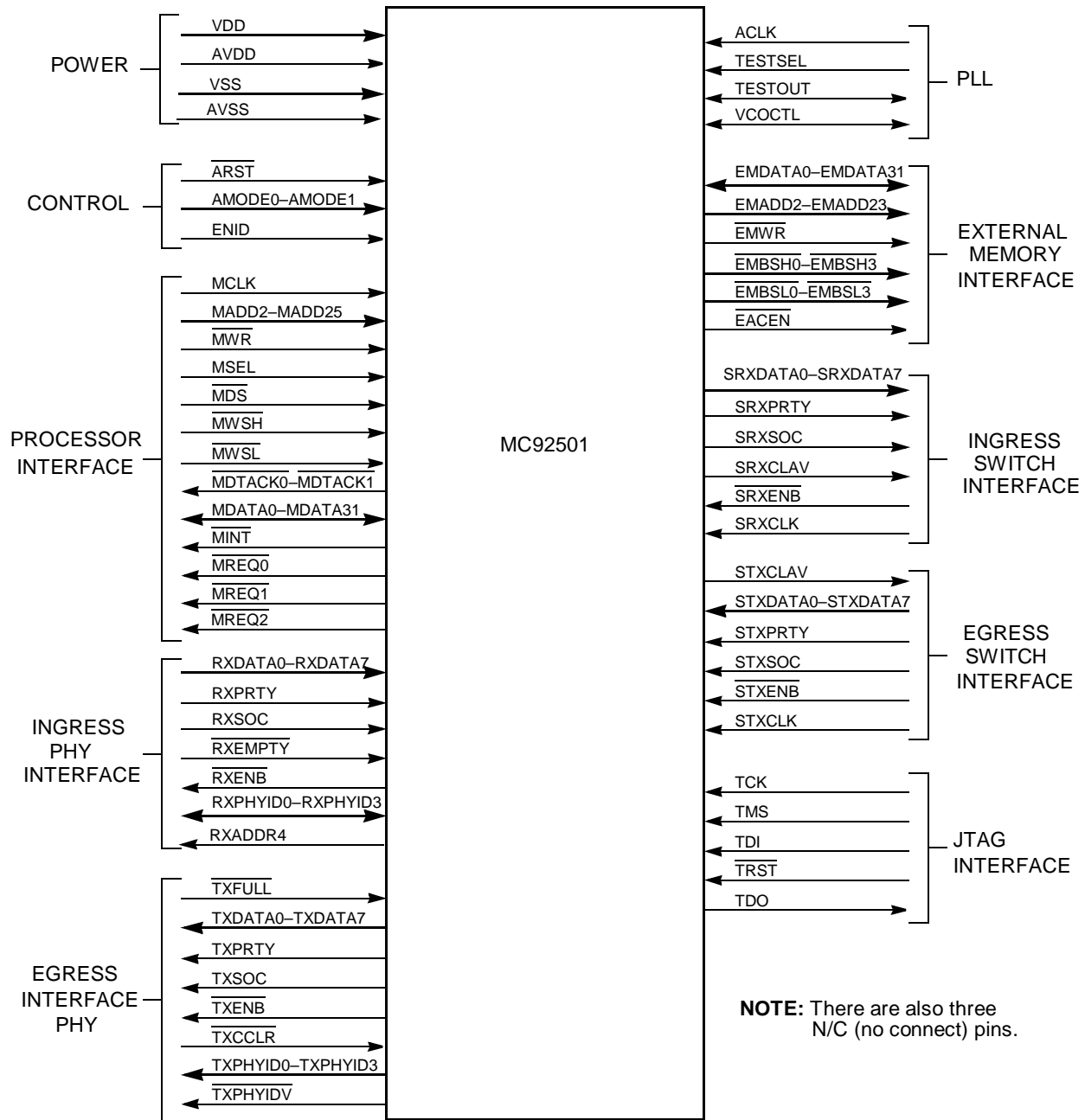


Figure 1-1. Functional Signal Groups

1.2 Power and Ground Signals

Table 1-2. Power and Ground Signals

| Signal Name | Description |
|-------------|--|
| VDD | Input Power |
| AVDD | PLL Analog Power —Isolate this input to eliminate coupling of digital switching noise into the PLL |
| VSS | System Ground |
| AVSS | PLL Analog Ground —Isolate this input to eliminate coupling of digital switching noise into the PLL |

1.3 Control Signals

Table 1-3. Control Signals

| Signal Name | Signal Type | Detailed Description |
|--------------------------|-------------|--|
| $\overline{\text{ARST}}$ | Input | ATMC Power-up Reset —This input signal is used for power-up reset of the entire chip. It must be asserted for at least the time required by the PLL to stabilize. |
| AMODE0– AMODE1 | Input | ATMC Mode —These input signals determine the operating mode of the chip's test features. In normal usage these pins should be grounded. |
| ENID | Input | Enable IDD —This input pin is used for test purposes. In normal usage the ENID pin must be grounded. |

Note: All inputs are 5 V tolerant.

1.4 Processor Interface Signals

Table 1-4. Processor Interface Signals

| Signal Name | Signal Type | Detailed Description |
|--------------|----------------|--|
| MCLK | Input | MP Clock —This input signal is used as the Microprocessor clock inside the MC92501. This signal drives the microprocessor logic in the MC92501. The duty cycle should be in the range of 40–60%. |
| MADD2–MADD25 | Input | MP Address Bus —This input bus contains the address which is used by the microprocessor to define the register being accessed. This bus is used by the MC92501 at the assertion of MSEL and sampled on the falling edge of MCLK. |
| MWR | Input | MP Write —This input signal is used to determine whether the MP is reading from the MC92501 or writing to it. This signal is sampled by the MC92501 on the falling edge of MCLK. The MC92501 drives MDATA when MSEL = 0 and MWR = 1. |
| MSEL | Input | MP Select —This input signal is used to determine that the current access to the MC92501 is valid. This signal is sampled by the MC92501 on the falling edge of MCLK. |
| MDS | Input | MP Data Select —This input signal is used to indicate when the data on MDATA is valid during a write access to the MC92501. This signal is sampled by the MC92501 on the falling edge of MCLK. |
| MWSH A1 | Input Input | MP Word Write Enable High —This signal indicates that the high word is being written. During a maintenance write access, the value detected on MWSH/A1 is driven on the appropriate EMBSH signal. During read access EMBSH signal is always asserted. Address 1 —When configured appropriately during a maintenance write access, this signal serves as Address 1. During a read access, this signal is ignored. Note: This input signal is programmed by the <i>Word Select Signals Mode (WSSM)</i> bit in the Microprocessor Configuration Register (MPCONR). The signal is sampled by the MC92501 on the falling edge of MCLK. Table 1-5 describes the combined MWSH/A1 and MWSL/Size functionality |
| MWSL SIZE | Input Input | MP Word Write Enable Low —This signal indicates that the high word is being written. During a maintenance write access, the value detected on MWSL/SIZE is driven on the appropriate EMBSL signal. During read access EMBSL signal is always asserted. Access Size —When configured appropriately during a maintenance write access, this signal indicates the size of the maintenance write access: either 32 bits or 16 bits access. During a read access, this signal is ignored and the access width is 32 bits. Note: This input signal is programmed by the <i>Word Select Signals Mode (WSSM)</i> bit in the Microprocessor Configuration Register (MPCONR). The signal is sampled by the MC92501 on the falling edge of MCLK. Table 1-5 describes the combined MWSH/A1 and MWSL/Size functionality |

Table 1-4. Processor Interface Signals (Continued)

| Signal Name | Signal Type | Detailed Description |
|---------------------------|--------------|---|
| MDTACK0– MDTACK1 | Output | MP Data Acknowledge 0–1 —These tri-statable output signals are used to indicate the end of an access from the MC92501. At the end of each access, this signal is actively pulled up and then released. The user may program the MC92501 not to drive this signal during certain types of accesses. This signal is output asynchronously to MCLK. |
| MDATA0– MDATA31 | Input/Output | MP Data Bus —This tri-state bidirectional bus provides the general data path between the MC92501 and the microprocessor. |
| MINT | Output | MP Interrupt —This output signal is used to notify the microprocessor of the occurrence of interrupting events. This signal is asserted on the rising edge of ACLK (asynchronous with respect to MCLK). |
| $\overline{\text{MREQ0}}$ | Output | MP Request 0 —This output signal can be programmed to one of three options (described below in note 2). Its default value is option #1: MP Cell In Request (MCIREQ). |
| $\overline{\text{MREQ1}}$ | Output | MP Request 1 —This output signal can be programmed to one of three options (described below in note 2). Its default value is option #2: MP Cell Out Request (MCOREQ).. |
| $\overline{\text{MREQ2}}$ | Output | MP Request 2 —This output signal can be programmed to one of three options (described below in note 2). Its default value is option #3: External Memory Maintenance Request (EMMREQ). |

Notes: 1. All inputs are 5 V tolerant.

2. $\overline{\text{MREQ0}}$, $\overline{\text{MREQ1}}$ and $\overline{\text{MREQ2}}$ signals are fully backward compatible to the MC92501 Revision A MCIREQ, MCOREQ and EMMREQ signals, respectively. The $\overline{\text{MREQ[n]}}$ signals are used by DMA devices and can be programmed to support DMA requests as follows:

- *MP Cell In Request:* $\overline{\text{MREQ[n]}}$ is an output signal that can be used by an external DMA device as a control line indicating when to start a new cell insertion cycle into the MC92501. It is asserted whenever the Cell Insertion Register array is available to be written. This signal is output on the falling edge of MCLK.
- *MP Cell Out Request:* $\overline{\text{MREQ[n]}}$ is an output signal may be used by an external DMA device as a control line indicating when to start a new cell extraction cycle from the MC92501. It is asserted whenever the Cell Extraction Register array is available to be read. It is output on the falling edge of MCLK.
- *External Memory Maintenance Request:* $\overline{\text{MREQ[n]}}$ is an output signal is asserted a programmable number of clock cycles before the start of an External Memory maintenance cycle. It is deasserted after a programmable number of maintenance accesses have been performed. It is output on the falling edge of MCLK.

Table 1-5. Host Interface Fields

| $WSSM = 0$ | | $WSSM = 1$ and DO-Data Order = 0 | | $WSSM = 1$ and DO-Data Order=1 | | Function |
|-------------------|-------------------|--|------|--------------------------------------|------|----------------|
| \overline{MWSH} | \overline{MWSL} | A1 | Size | A1 | Size | |
| 0 | 0 | x | 0 | x | 0 | Write D(31:0) |
| 0 | 1 | 0 | 1 | 1 | 1 | Write D(31:16) |
| 1 | 0 | 1 | 1 | 0 | 1 | Write D(15:00) |

Note: All Cell Extraction Register, Cell Insertion Register, and General Register accesses are long-word (32-bit) accesses, so both $\overline{MWSH}/A1$ and $\overline{MWSL}/SIZE$ should be asserted low for these write accesses when write-enable mode is selected.

1.5 Ingress PHY Interface Signals

Table 1-6. Ingress PHY Interface Signals

| Signal Name | Signal Type | Detailed Description |
|----------------------|-------------|--|
| RXDATA0–RXDATA7 | Input | Receive Data Bus —This input data bus receives octets from the PHY chip. When $RXENB$ is active, RXDATA is sampled into the MC92501. |
| RXPRTY | Input | Receive Data Bus Parity (RXPRTY) —This input is the odd parity over RXDATA. This input is ignored if $RXENB$ is not active or the parity check is disabled. |
| RXSOC | Input | Receive Start Of Cell (RXSOC) —This input, when high, indicates that the current RXDATA is the first byte of a cell. This input is sampled when $RXENB$ is active. |
| $\overline{RXEMPTY}$ | Input | Receive PHY Empty —This input, when low, indicates that currently the PHY chip has no available data. |
| \overline{RXENB} | Output | Receive Enable —This output, when low, indicates that the MC92501 is ready to receive data. |
| RXPHYID0–RXPHYID3 | Input | Receive PHY Device ID Bus 0–3 —In UTOPIA level 1, this is an input bus that indicates the ID number of the PHY device currently transferring data to the MC92501. If only a single PHY device is supported, this bus should be tied low. This bus is sampled along with the first octet of each cell. |
| RXADDR0–RXADDR3 | Output | Receive Address 0–3 —In UTOPIA Level 2, this is an output bus that indicates the 4 least significant bits of the ID number of the PHY device which is being polled or selected by the MC92501. |
| RXADDR4 | Output | Receive Address 4 —This signal is an output signal that indicates the most significant bit of the ID number of the PHY device that is being polled or selected by the MC92501. |

Note: All inputs are 5 V tolerant.

1.6 Egress PHY Interface Signals

Table 1-7. Egress PHY Interface Signals

| Signal Name | Signal Type | Detailed Description |
|------------------------------|-------------|---|
| $\overline{\text{TXFULL}}$ | Input | Transmit PHY Full —This input signal indicates, when low, that the PHY device is full. |
| TXDATA0– TXDATA7 | Output | Transmit Data Bus —This output data bus transmits octets to the PHY chip. When $\overline{\text{TXENB}}$ is active, TXDATA contains a valid octet for the PHY. |
| TXPRTY | Output | Transmit Data Bus Parity —This output signal is the odd parity over TXDATA. When $\overline{\text{TXENB}}$ is active, TXPRTY is a valid parity bit for the PHY. |
| TXSOC | Output | Transmit Start Of Cell —This output signal indicates, when high, that the current data on TXDATA is the first byte of a cell. TXSOC is valid when $\overline{\text{TXENB}}$ is asserted. |
| $\overline{\text{TXENB}}$ | Output | Transmit Enable —This output signal, when low, indicates that TXDATA, TXPRTY, and TXSOC are valid data for the PHY. |
| $\overline{\text{TXCCLR}}$ | Input | Transmit Cell Clear —This input signal indicates, when low, that the current cell should be cleared from the Egress PHY interface. |
| TXPHYID0– TXPHYID3 | Output | Transmit PHY ID 0–3 —In UTOPIA level 1, this is an output bus that indicates the ID number of the PHY device to which either the current cell or the next cell is directed. The functionality is controlled by the MC92501 General Configuration Register (GCR). |
| TXADDR0– TXADDR3 | Output | Transmit Address 0–3 —In UTOPIA level 2, this is an output bus that indicates the 4 least significant bits of the ID number of the PHY device which is being polled or selected by the MC92501. |
| $\overline{\text{TXPHYIDV}}$ | Output | Transmit Next PHY ID Valid —In UTOPIA level 1, this is an output signal that, when low, indicates that TXPHYID (when configured as the next cell's ID) is valid. If TXPHYID is configured to refer to the current cell, TXPHYIDV is not used. |
| TXADDR4 | Output | Transmit Address 4 —In UTOPIA level 2, this an output signal that indicates the most significant bit of the ID number of the PHY device which is being polled or selected by the MC92501. |

Note: All inputs are 5 V tolerant.

1.7 PLL Signals

Table 1-8. PLL Signals

| Signal Name | Signal Type | Detailed Description |
|-------------|--------------|---|
| ACLK | Input | ATMC Master Clock —This input signal is used by the PLL to generate the internal master clock of MC92501. The duty cycle should be in the range of 40–60%. |
| TESTSEL | Input | This is a dedicated test signal that must be grounded during normal system operation. |
| TESTOUT | Input/Output | This is a dedicated test signal that must be connected to the analog ground (AVSS) during normal system operation. |
| VCOCTL | Input/Output | This is a dedicated test signal that must be connected to the analog ground (AVSS) during normal system operation. |

Note: All inputs are 5 V tolerant.

1.8 External Memory Interface Signals

Table 1-9. External Memory Interface Signals

| Signal Name | Signal Type | Detailed Description |
|------------------|--------------|---|
| EMDATA0–EMDATA31 | Input/Output | External Memory Data Bus —This tri-statable bidirectional bus is the data path between the MC92501 and External Memory. |
| EMADD2–EMADD23 | Output | External Memory Address Bus —This output bus is the general address bus used by the MC92501 to access the External Memory. |
| EMWR | Output | External Memory Write —When asserted (low), this output signal indicates that the current cycle to the External Memory is a write cycle. This signal is asserted within the cycle. |
| EMBSH0–EMBSH3 | Output | External Memory Bank Select High —These output signals are used to select the high word of the appropriate memory bank. One or more of these signals is asserted for each External Memory access according to the value of EMADD. During a maintenance write access from the microprocessor, the value detected on MWSH is driven on the appropriate EMBSH signal. |
| EMBSL0–EMBSL3 | Output | External Memory Bank Select Low —These output signals are used to select the low word of the appropriate memory bank. One or more of these signals is asserted for each External Memory access according to the value of EMADD. During a maintenance write access from the microprocessor, the value detected on MWSL is driven on the appropriate EMBSL signal. |

Table 1-9. External Memory Interface Signals (Continued)

| Signal Name | Signal Type | Detailed Description |
|-------------|-------------|--|
| EACEN | Output | External Address Compression Enable —This output signal is asserted when data is being written to or read from an external address compression device using the External Memory Data Bus. |

Note: All inputs are 5 V tolerant.

1.9 Ingress Switch Interface Signals

Table 1-10. Ingress Switch Interface Signals

| Signal Name | Signal Type | Detailed Description |
|-------------------|-------------|---|
| SRXDATA0–SRXDATA7 | Output | Receive DATA BUS (SRXDATA0-SRXDATA7) —This three-state output data bus transmits bytes to the switch. When SRXENB is active, SRXDATA contains valid data for the switch. This bus is updated on the rising edge of SRXCLK. |
| SRXPRTY | Output | Receive Data Bus Parity —This three-state output is the parity protection of SRXDATA transmitted to the switch. The type of parity (even/odd) is defined by the Ingress Switch Interface Configuration Register (ISWCR).. |
| SRXSOC | Output | Receive Start Of Cell —This three-state output, when high, indicates that the current data on SRXDATA is the first byte of a cell structure (including the overhead bytes). |
| SRXCLAV | Output | Receive Switch Cell Available —This output, when asserted, indicates that the MC92501 has a cell ready to transfer to the switch. When deasserted, it indicates that currently there is no data available for the switch. |
| SRXENB | Input | Receive Enable —This input, when low, enables new values on SRXDATA, SRXPRTY and SRXSOC. |
| SRXCLK | Input | Receive Clock —This input is used to clock the Ingress switch interface signals. |

Note: All inputs are 5 V tolerant.

1.10 Egress Switch Interface Signals

Table 1-11. Egress Switch Interface Signals

| Signal Name | Signal Type | Detailed Description |
|-------------------|-------------|--|
| STXCLAV | Output | Transmit Cell Available —This output, when asserted, indicates that the MC92501 is prepared to receive a complete cell. |
| STXDATA0–STXDATA7 | Input | Transmit Data Bus —This input data bus receives bytes from the switch. When STXENB is asserted, STXDATA is sampled into the MC92501 on the rising edge of STXCLK. |
| STXPRTY | Input | Transmit Data Bus Parity —This input is the parity over STXDATA. The type of parity (even/odd) and the parity check control are defined by the Egress Switch Interface Configuration Register (ESWCR). This input is ignored if STXENB is deasserted or the parity check is disabled. It is sampled on the rising edge of STXCLK. |
| STXSOC | Input | Transmit Start Of Cell —This input indicates, when high, that the current data is the first byte of a cell structure (including the overhead bytes). This input is sampled on the rising edge of STXCLK when STXENB is asserted. |
| STXENB | Input | Transmit Enable —This input, when low, enables STXDATA, STXPRTY, and STXSOC. |
| STXCLK | Input | Transmit Clock —This input signal is used to clock the Egress switch interface signals. |

Note: All inputs are 5 V tolerant.

1.11 JTAG Interface Signals

Table 1-12. JTAG Interface Signals

| Signal Name | Signal Type | Detailed Description |
|-------------|-------------|---|
| TCK | Input | Test Clock —This input pin is the JTAG clock. The TDO, TDI, and TMS pins are synchronized by this signal. |
| TMS | Input | Test Mode Select —This input signal is sampled on the rising edge of TCK. TMS is responsible for the state change in the test access port state machine. |
| TDI | Input | Test Data Input —This input signal is sampled on the rising edge of TCK. TDI is the data to be shifted toward the TDO output. |
| TRST | Input | Test Reset —This input signal is the JTAG asynchronous reset. When asserted low, the Test Access Port is forced to the Test_Logic_Reset state. When JTAG is not being used, this signal should be hard-wired to GND or tied to ARST. |
| TDO | Output | Test Data Output —This tri-state output changes its logical value on the falling edge of TCK. |

Note: All inputs are 5 V tolerant.

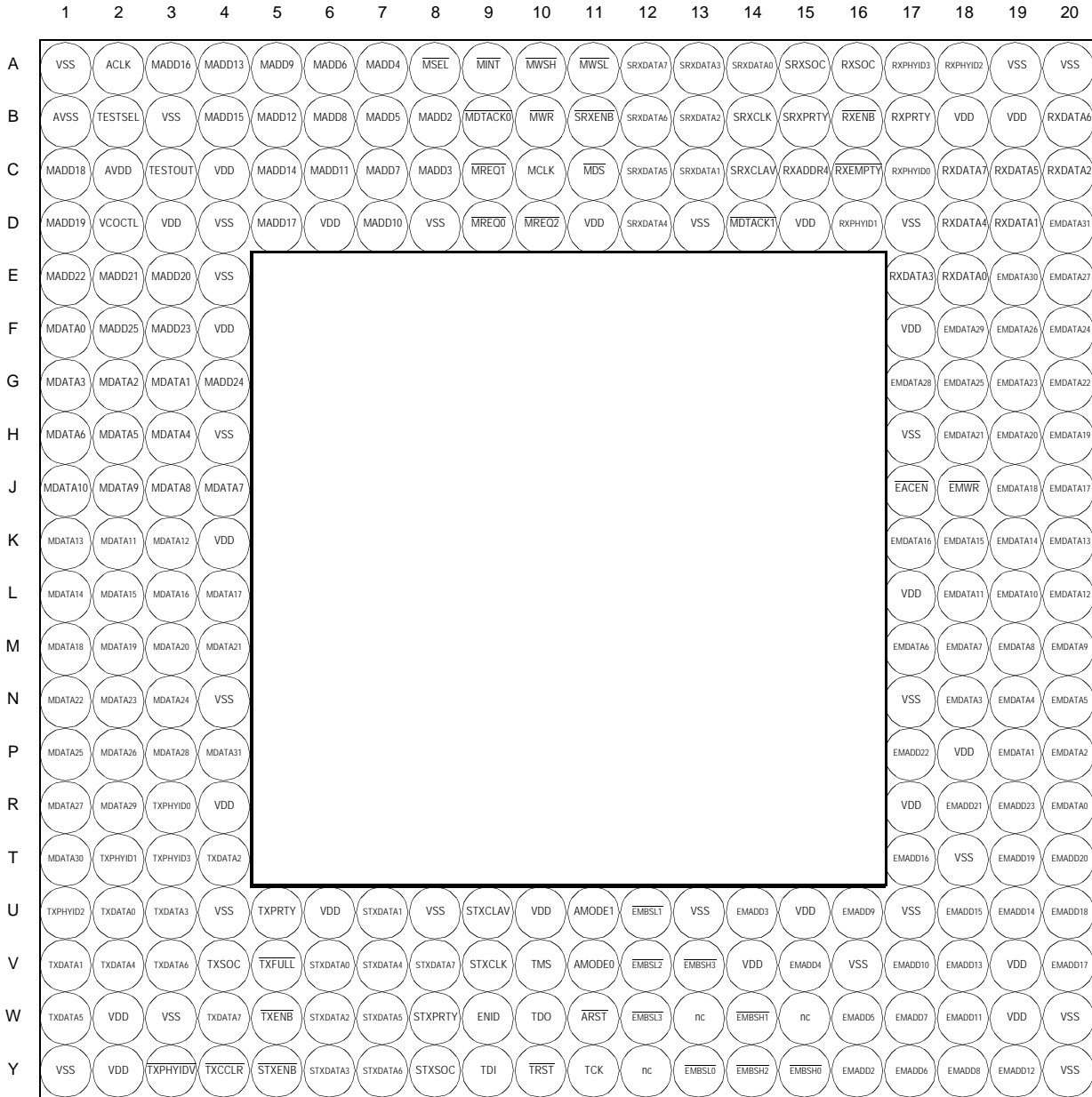
Signal and Packaging Information

2.1 Introduction

This section provides information on packaging, including a diagram of the package with signals and tables showing how the signals described in **Section 1** are allocated. The MC92501 is available in a 256-lead Glob-Top Ball Grid Array (GTBGA) package. The package mechanical drawing is provided at the end of this section.

2.2 GTBGA Package Description

A GTBGA package top view is shown in **Figure 2-1** with signal and location designators.



- Notes:**
- Locations marked as *nc* must not be connected.
 - The figure only shows the primary signal name for each lead. For the Ingress and Egress PHY Interface signals, the primary signal names are those used in UTOPIA Level 1. For UTOPIA Level 2, leads A17, A18, C17, and D16 change to RXADDR3, RXADDR2, RXADDR0, and RXADDR1, respectively. Leads R3, T2, T3, U1, and Y3 change to TXADDR0, TXADDR1, TXADDR3, TXADDR2, and TXADDR4, respectively. The Microprocessor signals also have an alternate configuration that changes leads A10 and A11 to signals A1 and SIZE, respectively.

Figure 2-1. MC92501 256-Lead GTBGA Diagram (Top View)

Table 2-1. MC92501 256-Lead GTBGA Package Signal List by Location

| Location | Signal Name | Location | Signal Name | Location | Signal Name | Location | Signal Name |
|----------|-------------------------------|----------|-----------------------------|----------|-----------------------------|----------|-----------------------------|
| A1 | VSS | B1 | AVSS | C1 | MADD18 | D1 | MADD19 |
| A2 | ACLK | B2 | TESTSEL | C2 | AVDD | D2 | VCCTL |
| A3 | MADD16 | B3 | VSS | C3 | TESTOUT | D3 | VDD |
| A4 | MADD13 | B4 | MADD15 | C4 | VDD | D4 | VSS |
| A5 | MADD9 | B5 | MADD12 | C5 | MADD14 | D5 | MADD17 |
| A6 | MADD6 | B6 | MADD8 | C6 | MADD11 | D6 | VDD |
| A7 | MADD4 | B7 | MADD5 | C7 | MADD7 | D7 | MADD10 |
| A8 | $\overline{\text{MSEL}}$ | B8 | MADD2 | C8 | MADD3 | D8 | VSS |
| A9 | $\overline{\text{MINT}}$ | B9 | $\overline{\text{MDTACK0}}$ | C9 | $\overline{\text{MREQ1}}$ | D9 | $\overline{\text{MREQ0}}$ |
| A10 | $\overline{\text{MWSH/A1}}$ | B10 | $\overline{\text{MWR}}$ | C10 | MCLK | D10 | $\overline{\text{MREQ2}}$ |
| A11 | $\overline{\text{MWSL/SIZE}}$ | B11 | $\overline{\text{SRXENB}}$ | C11 | $\overline{\text{MDS}}$ | D11 | VDD |
| A12 | SRXDATA7 | B12 | SRXDATA6 | C12 | SRXDATA5 | D12 | SRXDATA4 |
| A13 | SRXDATA3 | B13 | SRXDATA2 | C13 | SRXDATA1 | D13 | VSS |
| A14 | SRXDATA0 | B14 | SRXCLK | C14 | SRXCLAV | D14 | $\overline{\text{MDTACK1}}$ |
| A15 | SRXSOC | B15 | SRXPRTY | C15 | RXADDR4 | D15 | VDD |
| A16 | RXSOC | B16 | $\overline{\text{RXENB}}$ | C16 | $\overline{\text{RXEMPTY}}$ | D16 | RXPHYID1/ RXADDR1 |
| A17 | RXPHYID3/ RXADDR3 | B17 | RXPRTY | C17 | RXPHYID0/ RXADDR0 | D17 | VSS |
| A18 | RXPHYID2/ RXADDR2 | B18 | VDD | C18 | RXDATA7 | D18 | RXDATA4 |
| A19 | VSS | B19 | VDD | C19 | RXDATA5 | D19 | RXDATA1 |
| A20 | VSS | B20 | RXDATA6 | C20 | RXDATA2 | D20 | EMDATA31 |

Table 2-1. MC92501 256-Lead GTBGA Package Signal List by Location (Continued)

| Location | Signal Name | Location | Signal Name | Location | Signal Name | Location | Signal Name |
|----------|-------------|----------|---------------------------|----------|-------------|----------|----------------------|
| E1 | MADD22 | H1 | MDATA6 | L1 | MDATA14 | P1 | MDATA25 |
| E2 | MADD21 | H2 | MDATA5 | L2 | MDATA15 | P2 | MDATA26 |
| E3 | MADD20 | H3 | MDATA4 | L3 | MDATA16 | P3 | MDATA28 |
| E4 | VSS | H4 | VSS | L4 | MDATA17 | P4 | MDATA31 |
| E17 | RXDATA3 | H17 | VSS | L17 | VDD | P17 | EMADD22 |
| E18 | RXDATA0 | H18 | EMDATA21 | L18 | EMDATA11 | P18 | VDD |
| E19 | EMDATA30 | H19 | EMDATA20 | L19 | EMDATA10 | P19 | EMDATA1 |
| E20 | EMDATA27 | H20 | EMDATA19 | L20 | EMDATA12 | P20 | EMDATA2 |
| F1 | MDATA0 | J1 | MDATA10 | M1 | MDATA18 | R1 | MDATA27 |
| F2 | MADD25 | J2 | MDATA9 | M2 | MDATA19 | R2 | MDATA29 |
| F3 | MADD23 | J3 | MDATA8 | M3 | MDATA20 | R3 | TXPHYID0/ TXADDR0 |
| F4 | VDD | J4 | MDATA7 | M4 | MDATA21 | R4 | VDD |
| F17 | VDD | J17 | $\overline{\text{EACEN}}$ | M17 | EMDATA8 | R17 | VDD |
| F18 | EMDATA29 | J18 | $\overline{\text{EMWR}}$ | M18 | EMDATA7 | R18 | EMADD21 |
| F19 | EMDATA26 | J19 | EMDATA18 | M19 | EMDATA8 | R19 | EMADD23 |
| F20 | EMDATA24 | J20 | EMDATA17 | M20 | EMDATA9 | R20 | EMDATA0 |
| G1 | MDATA3 | K1 | MDATA13' | N1 | MDATA22 | T1 | MDATA30 |
| G2 | MDATA2 | K2 | MDATA11 | N2 | MDATA23 | T2 | TXPHYID1/ TXADDR1 |
| G3 | MDATA1 | K3 | MDATA12 | N3 | MDATA24 | T3 | TXPHYID3/ TXADDR3 |
| G4 | MADD24 | K4 | VDD | N4 | VSS | T4 | TXDATA2 |
| G17 | EMDATA28 | K17 | EMDATA16 | N17 | VSS | T17 | EMADD16 |
| G18 | EMDATA25 | K18 | EMDATA15 | N18 | EMDATA3 | T18 | VSS |
| G19 | EMDATA23 | K19 | EMDATA14 | N19 | EMDATA4 | T19 | EMADD19 |
| G20 | EMDATA22 | K20 | EMDATA13 | N20 | EMDATA5 | T20 | EMADD20 |

Table 2-1. MC92501 256-Lead GTBGA Package Signal List by Location (Continued)

| Location | Signal Name | Location | Signal Name | Location | Signal Name | Location | Signal Name |
|----------|----------------------------|----------|----------------------------|----------|----------------------------|----------|---|
| U1 | TXPHYID2/ TXADDR2 | V1 | TXDATA1 | W1 | TXDAT5 | Y1 | VSS |
| U2 | TXDATA0 | V2 | TXDATA4 | W2 | VDD | Y2 | VDD |
| U3 | TXDATA3 | V3 | TXDATA6 | W3 | VSS | Y3 | $\overline{\text{TXPHYIDV}}$ / $\overline{\text{TXADDR4}}$ |
| U4 | VSS | V4 | TXSOC | W4 | TXDATA7 | Y4 | $\overline{\text{TXCCLR}}$ |
| U5 | TXPRTY | V5 | $\overline{\text{TXFULL}}$ | W5 | $\overline{\text{TXENB}}$ | Y5 | $\overline{\text{STXENB}}$ |
| U6 | VDD | V6 | STXDATA0 | W6 | STXDATA2 | Y6 | STXDATA3 |
| U7 | STXDATA1 | V7 | STXDATA4 | W7 | STXDATA5 | Y7 | STXDATA6 |
| U8 | VSS | V8 | STXDATA7 | W8 | STXPRTY | Y8 | STXSOC |
| U9 | STXCLAV | V9 | STXCLK | W9 | ENID | Y9 | TDI |
| U10 | VDD | V10 | TMS | W10 | TDO | Y10 | $\overline{\text{TRST}}$ |
| U11 | AMODE1 | V11 | AMODE0 | W11 | $\overline{\text{ARST}}$ | Y11 | TCK |
| U12 | $\overline{\text{EMBSL1}}$ | V12 | $\overline{\text{EMBSL2}}$ | W12 | $\overline{\text{EMBSL3}}$ | Y12 | nc |
| U13 | VSS | V13 | $\overline{\text{EMBSH3}}$ | W13 | nc | Y13 | $\overline{\text{EMBSL0}}$ |
| U14 | EMADD3 | V14 | VDD | W14 | $\overline{\text{EMBSH1}}$ | Y14 | $\overline{\text{EMBSH2}}$ |
| U15 | VDD | V15 | EMADD4 | W15 | nc | Y15 | $\overline{\text{EMBSH0}}$ |
| U16 | EMADD9 | V16 | VSS | W16 | EMADD5 | Y16 | EMADD2 |
| U17 | VSS | V17 | EMADD10 | W17 | EMADD7 | Y17 | EMADD6 |
| U18 | EMADD15 | V18 | EMADD13 | W18 | EMADD11 | Y18 | EMADD8 |
| U19 | EMADD14 | V19 | VDD | W19 | VDD | Y19 | EMADD12 |
| U20 | EMADD18 | V20 | EMADD17 | W20 | VSS | Y20 | VSS |

Table 2-2. MC92501 256-Lead GTBGA Package Signal List by Name

| Signal Name | Location | Signal Name | Location | Signal Name | Location | Signal Name | Location |
|---------------------------|----------|----------------------------|----------|-------------|----------|--------------------------|----------|
| A1 | A10 | EMADD21 | R18 | EMDATA10 | L19 | EMDATA29 | F18 |
| ACLK | A2 | EMADD22 | P17 | EMDATA11 | L18 | EMDATA3 | N18 |
| AMODE0 | V11 | EMADD23 | R19 | EMDATA12 | L20 | EMDATA30 | E19 |
| AMODE1 | U11 | EMADD3 | U14 | EMDATA13 | K20 | EMDATA31 | D20 |
| $\overline{\text{ARST}}$ | W11 | EMADD4 | V15 | EMDATA14 | K19 | EMDATA4 | N19 |
| AVDD | C2 | EMADD5 | W16 | EMDATA15 | K18 | EMDATA5 | N20 |
| AVSS | B1 | EMADD6 | Y17 | EMDATA16 | K17 | EMDATA7 | M18 |
| $\overline{\text{EACEN}}$ | J17 | EMADD7 | W17 | EMDATA17 | J20 | EMDATA8 | M17 |
| EMADD10 | V17 | EMADD8 | Y18 | EMDATA18 | J19 | EMDATA8 | M19 |
| EMADD11 | W18 | EMADD9 | U16 | EMDATA19 | H20 | EMDATA9 | M20 |
| EMADD12 | Y19 | $\overline{\text{EMBSH0}}$ | Y15 | EMDATA2 | P20 | $\overline{\text{EMWR}}$ | J18 |
| EMADD13 | V18 | $\overline{\text{EMBSH1}}$ | W14 | EMDATA20 | H19 | ENID | W9 |
| EMADD14 | U19 | $\overline{\text{EMBSH2}}$ | Y14 | EMDATA21 | H18 | MADD10 | D7 |
| EMADD15 | U18 | $\overline{\text{EMBSH3}}$ | V13 | EMDATA22 | G20 | MADD11 | C6 |
| EMADD16 | T17 | $\overline{\text{EMBSL0}}$ | Y13 | EMDATA23 | G19 | MADD12 | B5 |
| EMADD17 | V20 | $\overline{\text{EMBSL1}}$ | U12 | EMDATA24 | F20 | MADD13 | A4 |
| EMADD18 | U20 | $\overline{\text{EMBSL2}}$ | V12 | EMDATA25 | G18 | MADD14 | C5 |
| EMADD19 | T19 | $\overline{\text{EMBSL3}}$ | W12 | EMDATA26 | F19 | MADD15 | B4 |
| EMADD2 | Y16 | EMDATA0 | R20 | EMDATA27 | E20 | MADD16 | A3 |
| EMADD20 | T20 | EMDATA1 | P19 | EMDATA28 | G17 | MADD17 | D5 |

Table 2-2. MC92501 256-Lead GTBGA Package Signal List by Name (Continued)

| Signal Name | Location | Signal Name | Location | Signal Name | Location | Signal Name | Location |
|-------------|----------|-------------------------|----------|-----------------------------|----------|-----------------------------|----------|
| MADD18 | C1 | MDATA16 | L3 | $\overline{\text{MDTACK0}}$ | B9 | RXDATA7 | C18 |
| MADD19 | D1 | MDATA17 | L4 | $\overline{\text{MDTACK1}}$ | D14 | $\overline{\text{RXEMPTY}}$ | C16 |
| MADD2 | B8 | MDATA18 | M1 | $\overline{\text{MINT}}$ | A9 | $\overline{\text{RXENB}}$ | B16 |
| MADD20 | E3 | MDATA19 | M2 | $\overline{\text{MREQ0}}$ | D9 | RXPHYID0 | C17 |
| MADD21 | E2 | MDATA2 | G2 | $\overline{\text{MREQ1}}$ | C9 | RXPHYID1 | D16 |
| MADD22 | E1 | MDATA20 | M3 | $\overline{\text{MREQ2}}$ | D10 | RXPHYID2 | A18 |
| MADD23 | F3 | MDATA21 | M4 | $\overline{\text{MSEL}}$ | A8 | RXPHYID3 | A17 |
| MADD24 | G4 | MDATA22 | N1 | $\overline{\text{MWR}}$ | B10 | RXPRTY | B17 |
| MADD25 | F2 | MDATA23 | N2 | $\overline{\text{MWSH}}$ | A10 | RXSOC | A16 |
| MADD3 | C8 | MDATA24 | N3 | $\overline{\text{MWSL}}$ | A11 | SIZE | A11 |
| MADD4 | A7 | MDATA25 | P1 | nc | W13 | SRXCLAV | C14 |
| MADD5 | B7 | MDATA26 | P2 | nc | W15 | SRXCLK | B14 |
| MADD6 | A6 | MDATA27 | R1 | nc | Y12 | SRXDATA0 | A14 |
| MADD7 | C7 | MDATA28 | P3 | RXADDR0 | C17 | SRXDATA1 | C13 |
| MADD8 | B6 | MDATA29 | R2 | RXADDR1 | D16 | SRXDATA2 | B13 |
| MADD9 | A5 | MDATA3 | G1 | RXADDR2 | A18 | SRXDATA3 | A13 |
| MCLK | C10 | MDATA30 | T1 | RXADDR3 | A17 | SRXDATA4 | D12 |
| MDATA0 | F1 | MDATA31 | P4 | RXADDR4 | C15 | SRXDATA5 | C12 |
| MDATA1 | G3 | MDATA4 | H3 | RXDATA0 | E18 | SRXDATA6 | B12 |
| MDATA10 | J1 | MDATA5 | H2 | RXDATA1 | D19 | SRXDATA7 | A12 |
| MDATA11 | K2 | MDATA6 | H1 | RXDATA2 | C20 | $\overline{\text{SRXENB}}$ | B11 |
| MDATA12 | K3 | MDATA7 | J4 | RXDATA3 | E17 | SRXPRTY | B15 |
| MDATA13 | K1 | MDATA8 | J3 | RXDATA4 | D18 | SRXSOC | A15 |
| MDATA14 | L1 | MDATA9 | J2 | RXDATA5 | C19 | STXCLAV | U9 |
| MDATA15 | L2 | $\overline{\text{MDS}}$ | C11 | RXDATA6 | B20 | STXCLK | V9 |

Table 2-2. MC92501 256-Lead GTBGA Package Signal List by Name (Continued)

| Signal Name | Location | Signal Name | Location | Signal Name | Location | Signal Name | Location |
|----------------------------|----------|------------------------------|----------|-------------|----------|-------------|----------|
| STXDATA0 | V6 | TXADDR4 | Y3 | VDD | C4 | VSS | A20 |
| STXDATA1 | U7 | $\overline{\text{TXCCLR}}$ | Y4 | VDD | D11 | VSS | B3 |
| STXDATA2 | W6 | TXDAT5 | W1 | VDD | D15 | VSS | D13 |
| STXDATA3 | Y6 | TXDATA0 | U2 | VDD | D3 | VSS | D17 |
| STXDATA4 | V7 | TXDATA1 | V1 | VDD | D6 | VSS | D4 |
| STXDATA5 | W7 | TXDATA2 | T4 | VDD | F17 | VSS | D8 |
| STXDATA6 | Y7 | TXDATA3 | U3 | VDD | F4 | VSS | E4 |
| STXDATA7 | V8 | TXDATA4 | V2 | VDD | K4 | VSS | H17 |
| $\overline{\text{STXENB}}$ | Y5 | TXDATA6 | V3 | VDD | L17 | VSS | H4 |
| STXPRTY | W8 | TXDATA7 | W4 | VDD | P18 | VSS | N17 |
| STXSOC | Y8 | $\overline{\text{TXENB}}$ | W5 | VDD | R17 | VSS | N4 |
| TCK | Y11 | $\overline{\text{TXFULL}}$ | V5 | VDD | R4 | VSS | T18 |
| TDI | Y9 | TXPHYID0 | R3 | VDD | U10 | VSS | U13 |
| TDO | W10 | TXPHYID1 | T2 | VDD | U15 | VSS | U17 |
| TESTOUT | C3 | TXPHYID2 | U1 | VDD | U6 | VSS | U4 |
| TESTSEL | B2 | TXPHYID3 | T3 | VDD | V14 | VSS | U8 |
| TMS | V10 | $\overline{\text{TXPHYIDV}}$ | Y3 | VDD | V19 | VSS | V16 |
| $\overline{\text{TRST}}$ | Y10 | TXPRTY | U5 | VDD | W19 | VSS | W20 |
| TXADDR0 | R3 | TXSOC | V4 | VDD | W2 | VSS | W3 |
| TXADDR1 | T2 | VCOCTL | D2 | VDD | Y2 | VSS | Y1 |
| TXADDR2 | U1 | VDD | B18 | VSS | A1 | VSS | Y20 |
| TXADDR3 | T3 | VDD | B19 | VSS | A19 | | |

2.3 GTBGA Mechanical Drawing

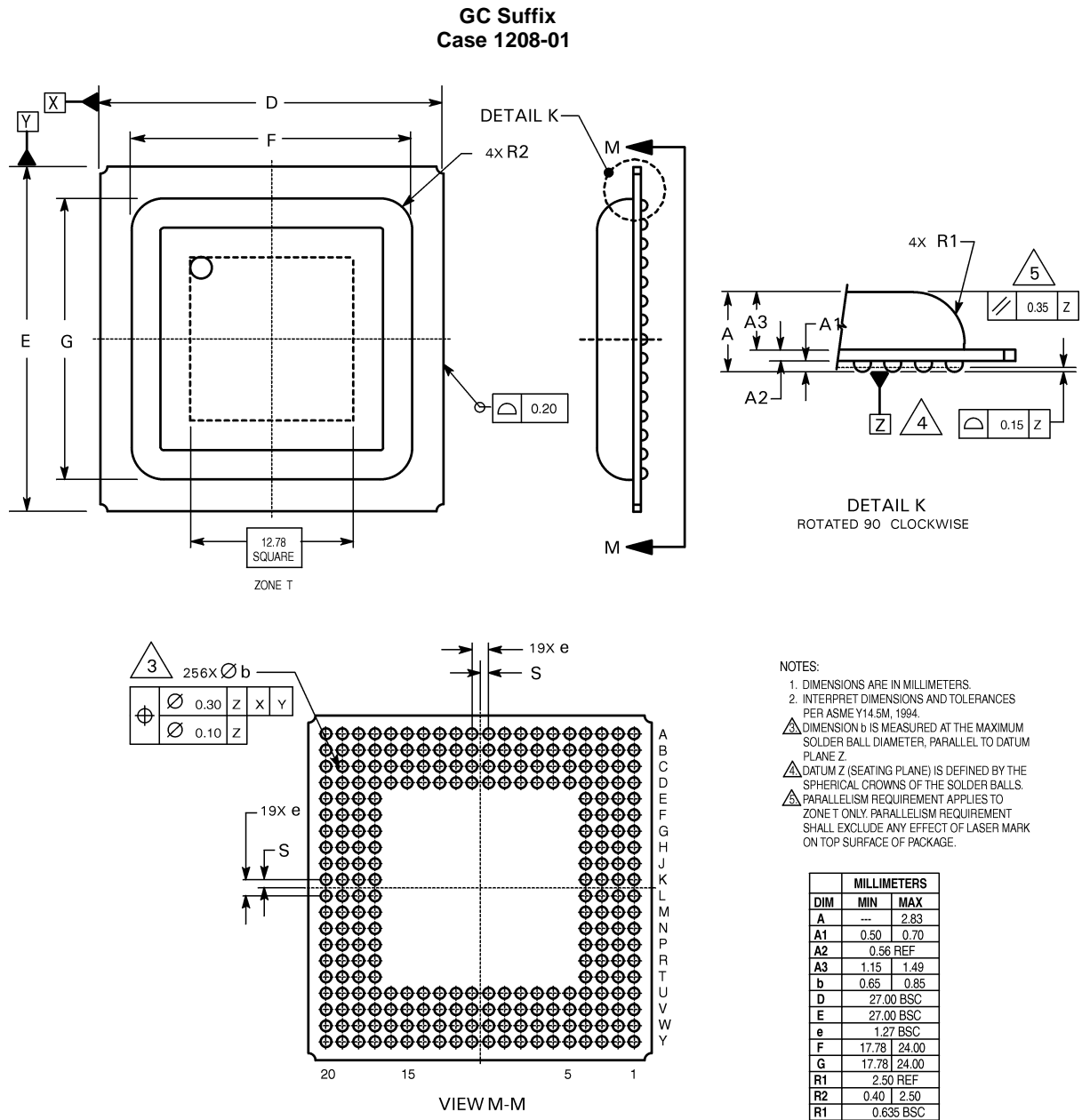


Figure 2-2. Glob-Top Ball Grid Array (GTBGA) Package

Specifications

3.1 Introduction

This section provides the following sets of physical and electrical specifications for the MC92501:

- Absolute Maximum Ratings
- Recommended Operating Conditions
- DC Electrical Characteristics
- Clocks
- Microprocessor Interface Timing
- PHY Interface Timing
- Switch Interface Timing
- External Memory Interface Timing

3.2 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

| Symbol | Parameter | Value/Value Range ¹ | Unit |
|--------------------------|--|--------------------------------|------|
| V_{DD} | DC Supply Voltage | -0.5 to 3.8 | V |
| V_{IN} ² | DC Input Voltage (5 V Tolerant) | -0.5 to 5.8 | V |
| V_{OUT} ^{2,3} | DC Output Voltage | -0.5 to $V_{DD} + 0.5$ | V |
| I | DC Current Drain per Pin, Any Single Input or Output | ±50 | mA |
| I | DC Current Drain VDD and VSS Pins | ±100 | mA |
| T_{STG} | Storage Temperature | -65 to +150 | °C |
| T_L | Lead Temperature (10 s soldering) | 300 | °C |

- Notes:**
1. Maximum ratings are those values beyond which damage to the device may occur.
 2. All input, bidirectional, and MDTACK are 5 V Tolerant. For proper operation it is recommended that V_{in} and V_{out} be constrained to $0 \leq (V_{IN}, V_{OUT}) \leq 5.5$ V.
 3. SRXDATAx, SRXSOC, SRXPRTY, TDO tri-state outputs must be constrained to $0 \leq V_{OUT} \leq V_{DD}$ in the high impedance state.
 4. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3.3 Recommended Operating Conditions

Table 3-2. Recommended Operating Conditions to Guarantee Functionality

| Symbol | Parameter | Min | Max | Unit |
|----------|---|-----|-----|------|
| V_{DD} | DC Supply Voltage, $V_{DD} = 3.3$ V (Nominal) | 3.0 | 3.6 | V |
| V_{in} | Input Voltage (5V Tolerant) | 0 | 5.5 | V |
| T_A | Industrial Operating Temperature | -40 | 85 | °C |

- Notes:**
1. All parameters are characterized for DC conditions after thermal equilibrium has been established.
 2. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
 3. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3.4 DC Electrical Characteristics

Table 3-3. DC Electrical Characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|-----------|---|---|------------------|------|---------------|
| V_{IH} | TTL Inputs (5V Tolerant) | — | 2.2 | 5.5 | V |
| V_{IL} | TTL Inputs (5V Tolerant) | — | -0.3 | 0.8 | V |
| I_{IN} | Input Leakage Current, No Pull Resistor | $V_{IN} = V_{DD}$ or V_{SS} | -5 | 5 | μA |
| | With Pullup Resistor * | | -50 | -5 | |
| | With Pulldown Resistor * | | 5 | 50 | |
| I_{OH} | Output High Current, LVTTL Output Type Outputs: $\overline{\text{EACEN}}$, $\overline{\text{EMWR}}$, $\overline{\text{EMADDx}}$, $\overline{\text{EMBSHx}}$, $\overline{\text{EMBSLx}}$ | $V_{DD} = \text{Min}$, $V_{OH} \text{ Min} = 0.8 V_{DD}$ | -24 | — | mA |
| | Output High Current, LVTTL Output Type Outputs: All other outputs | | -4 | — | |
| I_{OL} | Output Low Current, LVTTL Output Type Outputs: $\overline{\text{EACEN}}$, $\overline{\text{EMWR}}$, $\overline{\text{EMADDx}}$, $\overline{\text{EMBSHx}}$, $\overline{\text{EMBSLx}}$ | $V_{DD} = \text{Min}$, $V_{OL} \text{ Max} = 0.4 V$ | 24 | — | mA |
| | Output Low Current, LVTTL Output Type Outputs: All other outputs | | 4 | — | |
| I_{OZ} | Output Leakage Current, Tri-State Output | Output = High Impedance $V_{OUT} = V_{DD}$ or V_{SS} | -10 | 10 | μA |
| I_{DDQ} | Max Quiescent Supply Current | $I_{OUT} = 0 \text{ mA}$ $V_{IN} = V_{DD}$ or V_{SS} | 10 | | μA |
| I_{DD} | Max Dynamic Supply Current | Nominal Load Capacitance, ACLK = 25.6 Mhz, MCLK = 33 Mhz | 300 ¹ | | mA |
| C_I | Input Capacitance (TTL) | — | — | 8 | pF |

- Notes:**
1. Under Typical Loca, 25 Mhz ACLK/MCLK
 2. $T_A = -40^\circ\text{C}$ to 85°C , $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ Guaranteed
 3. Inputs may be modified to include pullup resistors at any time.
 4. See **Section 1** for pin input/output type.

3.5 Clocks

Table 3-4. Clock Timing

| Num | Characteristics | Min | Max | Unit |
|-----|--------------------------------|-----|-----|------|
| C1 | ACLK Cycle Time | 39 | 80 | ns |
| C2 | ACLK Pulse Width Low | 15 | — | ns |
| C3 | ACLK Pulse Width High | 15 | — | ns |
| C4 | ACLK Rise/Fall Time | — | 5 | ns |
| C5 | MCLK Cycle Time | 30 | — | ns |
| C6 | MCLK Pulse Width Low | 12 | — | ns |
| C7 | MCLK Pulse Width High | 12 | — | ns |
| C8 | MCLK Rise/Fall Time | — | 5 | ns |
| C9 | SRXCLK/STXCLK Cycle Time | 30 | — | ns |
| C10 | SRXCLK/STXCLK Pulse Width Low | 12 | — | ns |
| C11 | SRXCLK/STXCLK Pulse Width High | 12 | — | ns |
| C12 | SRXCLK/STXCLK Rise/Fall Time | — | 5 | ns |

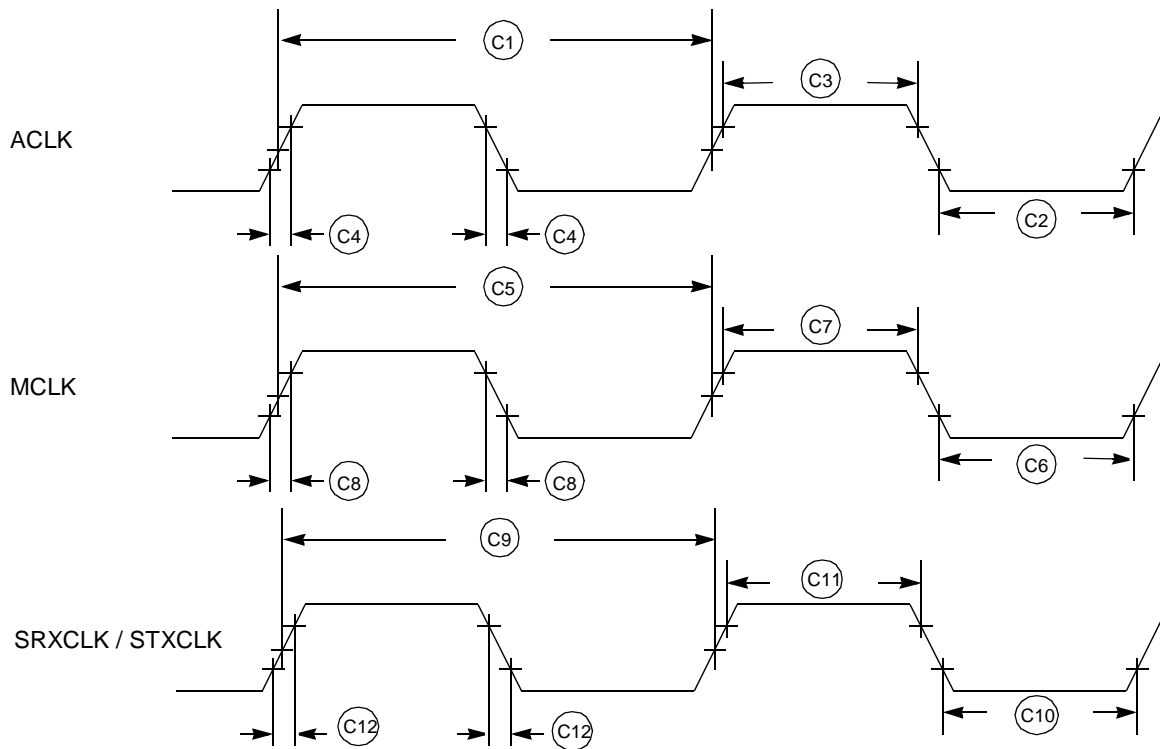


Figure 3-1. Clock Timing Diagrams

3.6 Microprocessor Interface Timing

The timing diagrams in this section are intended to convey setup and hold values for input signals and propagation delay values for output signals. For functional timing diagrams, see Section 4.5 Microprocessor Interface.

Table 3-5. Microprocessor Interface Timings

| Num | Characteristics | Min | Max | Unit |
|-----|--|-----|-------|------|
| 1 | $\overline{\text{MSEL}}$ setup time before MCLK falling edge | 5 | | ns |
| 2 | $\overline{\text{MSEL}}$ hold time after MCLK falling edge | 1 | | ns |
| 3 | MADD/ $\overline{\text{MWR}}$ setup time before $\overline{\text{MSEL}}$ assertion | 5 | | ns |
| 4 | MADD/ $\overline{\text{MWR}}$ hold time after MCLK falling edge ¹ | 3 | | ns |
| 5 | $\overline{\text{MDS}}$ setup time before MCLK falling edge | 5 | | ns |
| 6 | $\overline{\text{MDS}}$ hold time after MCLK falling edge | 1 | | ns |
| 7 | MDATA setup time before MCLK falling edge | 4 | | ns |
| 8 | MDATA hold time after MCLK falling edge | 1 | | ns |
| 9 | $\overline{\text{MSEL}}$ assertion to MDATA active | 0 | | ns |
| 11 | MCLK falling edge to MDATA valid for CER Accesses ² | | 26 | ns |
| 12 | $\overline{\text{MSEL}}$ deassertion to MDATA invalid | 1 | | ns |
| 13 | $\overline{\text{MSEL}}$ deassertion to MDATA inactive | | 11 | ns |
| 14 | $\overline{\text{MWR}}$ assertion to MDATA invalid | 1 | | ns |
| 15 | $\overline{\text{MWR}}$ assertion to MDATA inactive | | 11 | ns |
| 16 | MCLK rising edge to MDATA valid for Maintenance Accesses ^{2,3} | | T_D | ns |
| 17 | MCLK falling edge to MDATA valid for General Register Accesses ^{2,4} | | T_R | ns |
| 19 | $\overline{\text{MSEL}}$ assertion to $\overline{\text{MDTACK}}$ active | 0 | | ns |
| 20 | MCLK falling edge to $\overline{\text{MDTACK}}$ inactive | | 12 | ns |
| 21 | $\overline{\text{MSEL}}$ assertion to $\overline{\text{MDTACK0}}$ asserted ⁵ | | 9 | ns |
| 22 | $\overline{\text{MSEL}}$ deassertion to $\overline{\text{MDTACK}}$ deasserted ⁵ | | 13 | ns |
| 23 | MCLK rising edge to $\overline{\text{MDTACK}}$ asserted ⁵ | | 13 | ns |
| 24 | $\overline{\text{MWSH}}$, $\overline{\text{MWSL}}$ setup time before MCLK falling edge ¹ | 2 | | ns |
| 25 | $\overline{\text{MWSH}}$, $\overline{\text{MWSL}}$ hold time after MCLK falling edge ¹ | 3 | | ns |
| 26 | MCLK falling edge to $\overline{\text{REQ}}$ valid | 0 | 14 | ns |

Table 3-5. Microprocessor Interface Timings (Continued)

| Num | Characteristics | Min | Max | Unit |
|-----|---|-------|----------|------|
| 27 | MCLK falling edge to $\overline{\text{MDTACK}}$ asserted for General Register Read Accesses ^{5,6} | | T_{RD} | ns |
| 28 | MCLK falling edge to $\overline{\text{MDTACK}}$ asserted for General Register Write Accesses ^{5,7} | | T_{WD} | ns |
| 29 | Access width (MCLK falling edge to $\overline{\text{MSEL}}$ deassertion) for General Register Write Accesses ⁸ | T_W | | |
| 30 | $\overline{\text{MSEL}}$ assertion to $\overline{\text{MDTACK1}}$ asserted ⁹ | | 12 | ns |
| 31 | $\overline{\text{MDTACK0}}$ assertion to $\overline{\text{MDTACK1}}$ assertion | 0 | 5 | ns |

- Notes:**
1. This refers only to the first falling edge of MCLK in each access at which $\overline{\text{MSEL}}$ is asserted.
 2. This is for a 150 pF load. Add 0.9 ns for each additional 10 pF. For a 100 pF load, subtract 4 ns.
 3. T_D = External Memory access time + 18 ns
 4. T_R = 4 * ACLK period + 20 ns
 5. This is for a 50 pF load.
 6. T_{RD} = 4 * ACLK period + 11 ns
 7. T_{WD} is measured from the MCLK falling edge at which $\overline{\text{MDS}}$ is sampled as asserted.
 T_{WD} = 4 * ACLK period + 11 ns
 8. T_W is measured from the MCLK falling edge at which MDS is sampled as asserted. T_W = 4 * ACLK period. Note that the setup and hold times with respect to MCLK (timing values 1 and 2) still apply.
 9. This is for a 50 pF load.

Freescale Semiconductor, Inc.

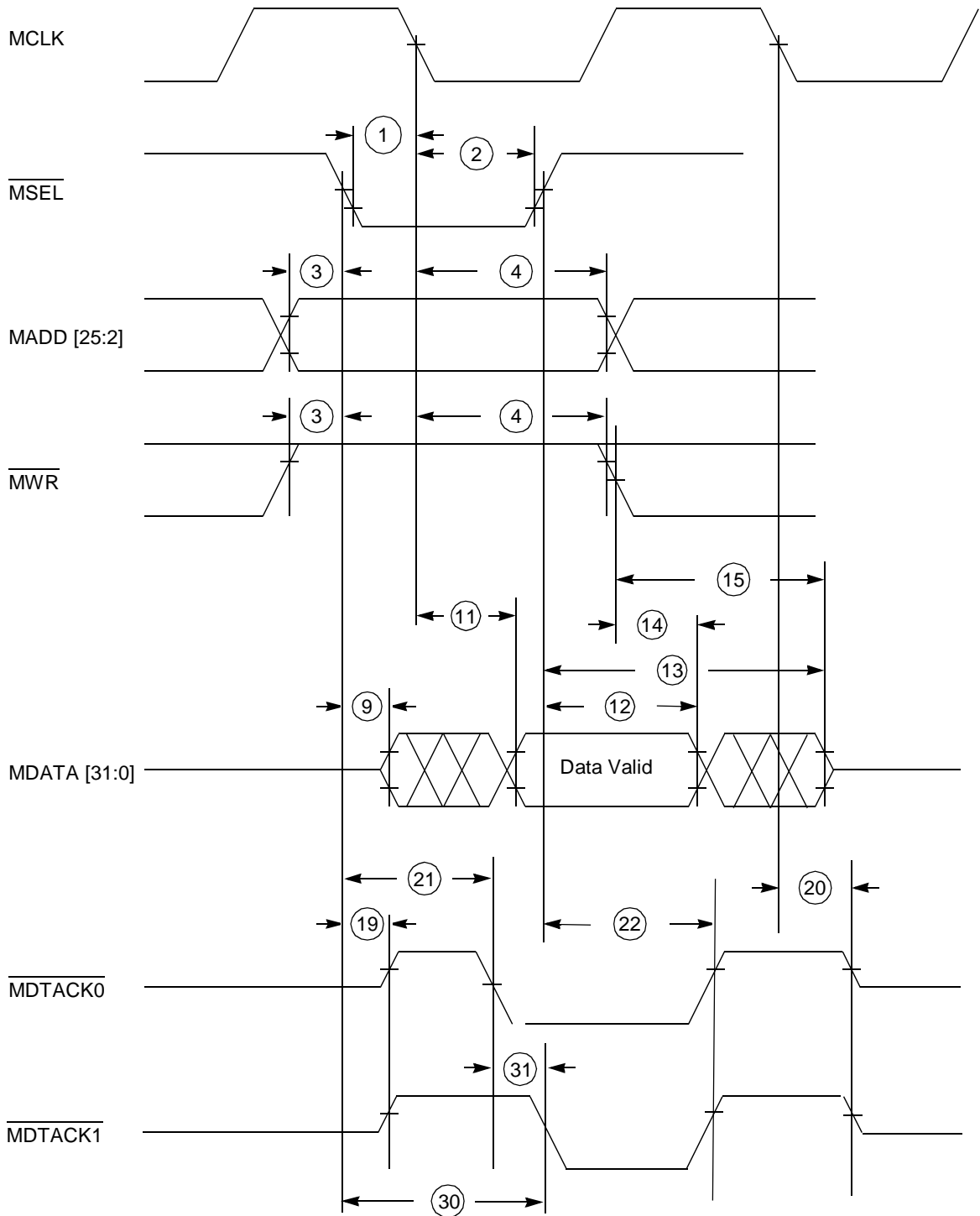


Figure 3-2. Cell Extraction Register Read Access Timing

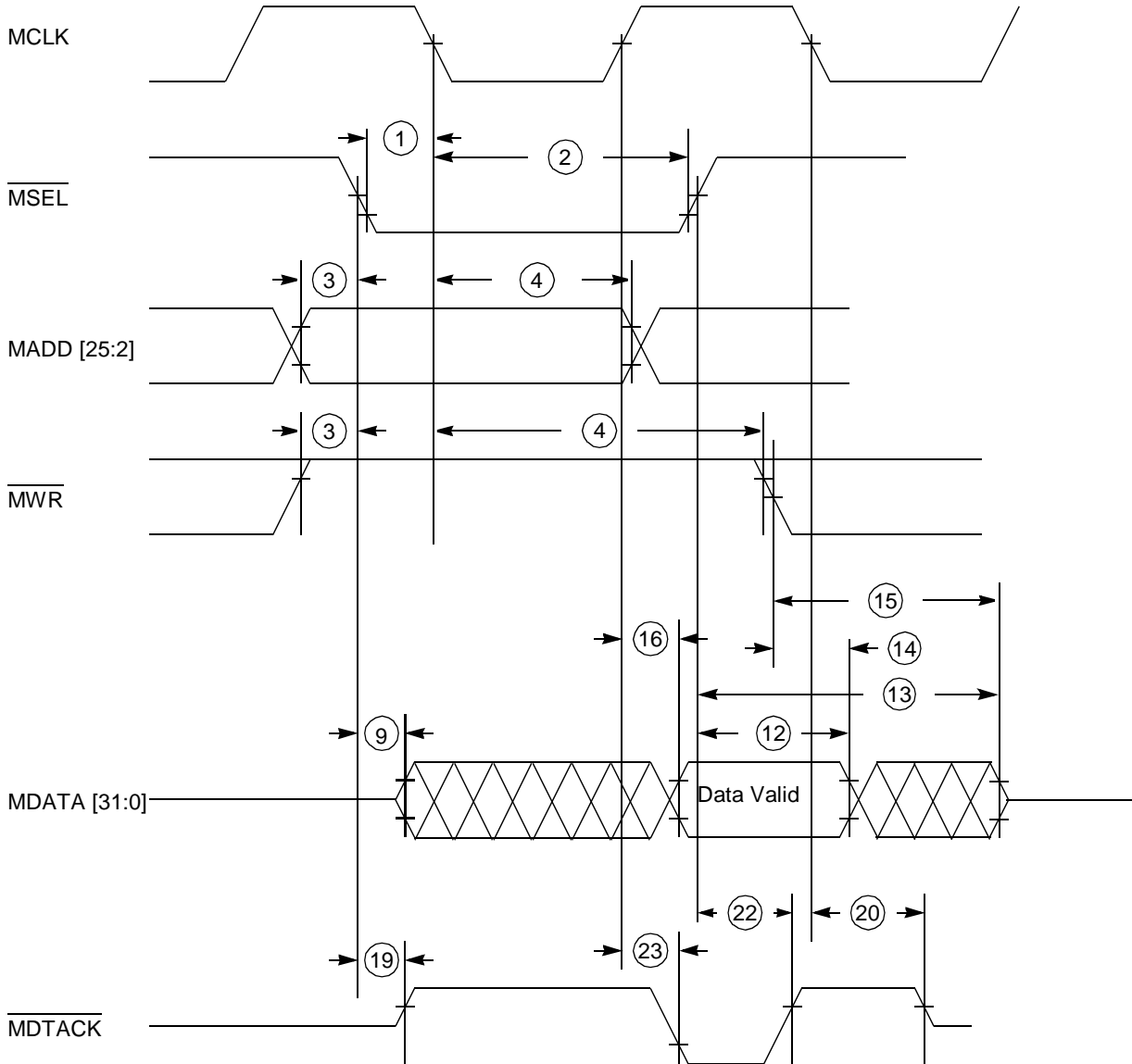


Figure 3-3. Maintenance Read Access Timing

Freescale Semiconductor, Inc.

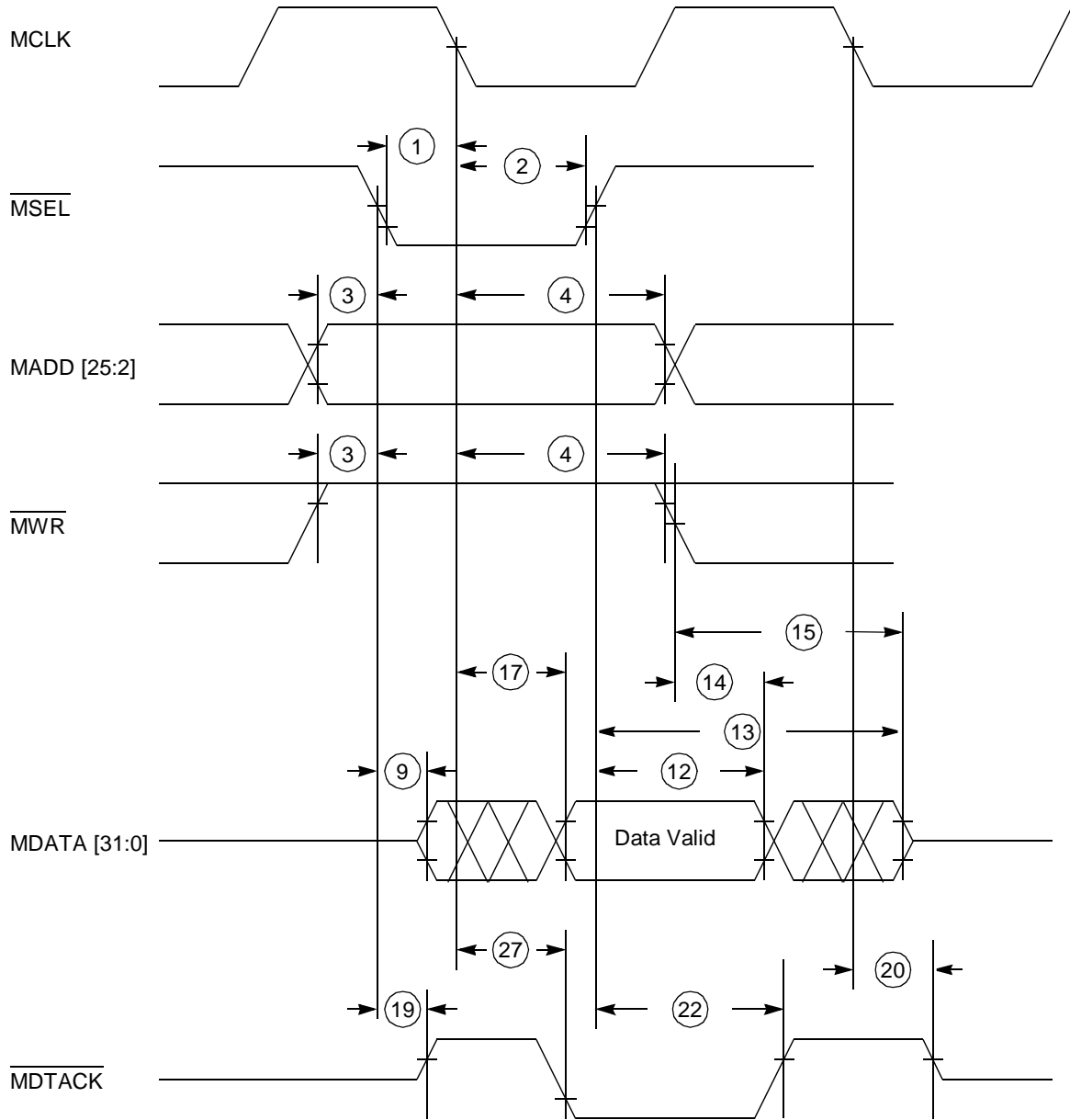


Figure 3-4. General Register Read Access Timing

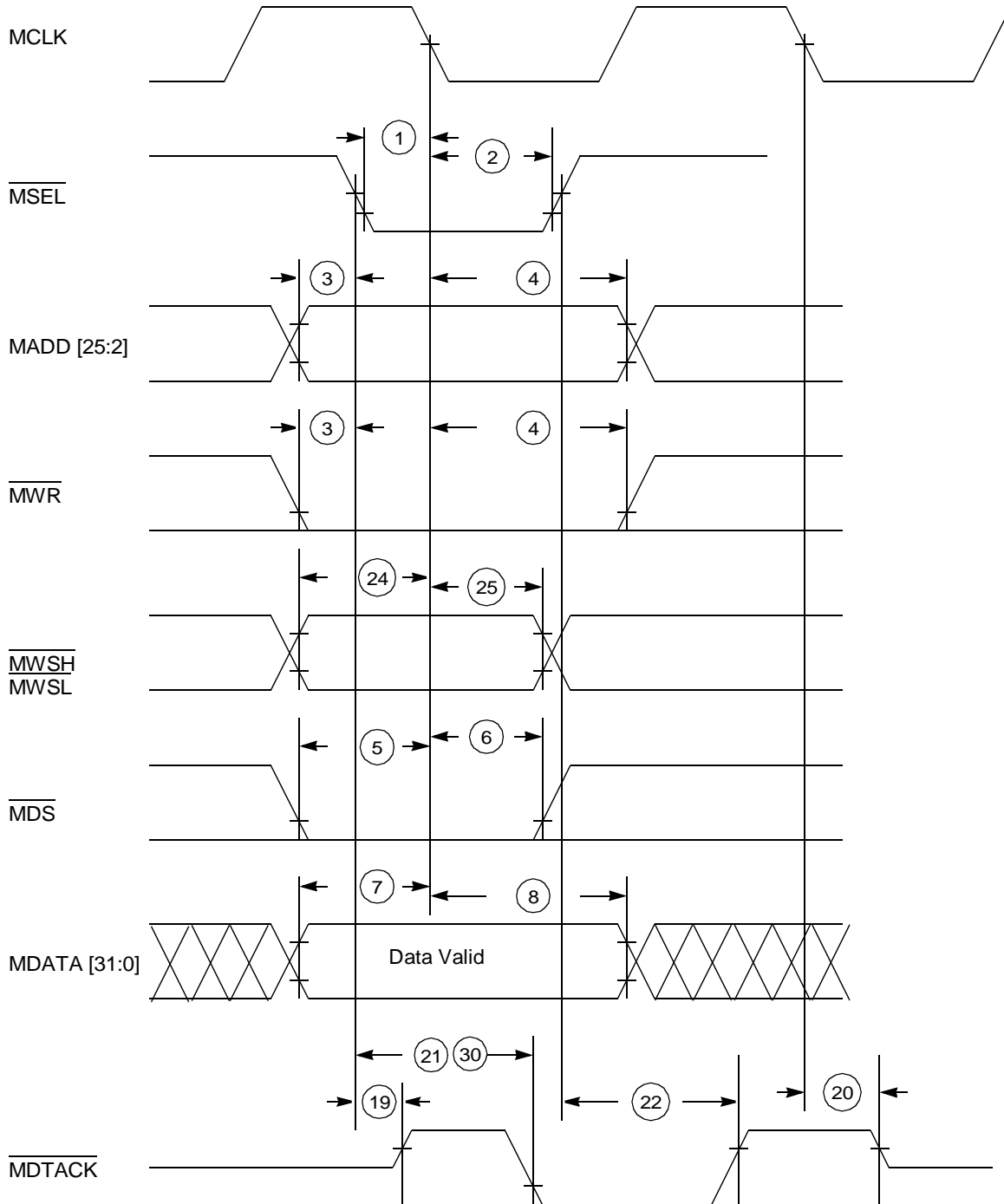


Figure 3-5. Cell Insertion Register Write Access/Maintenance Write Access Timing

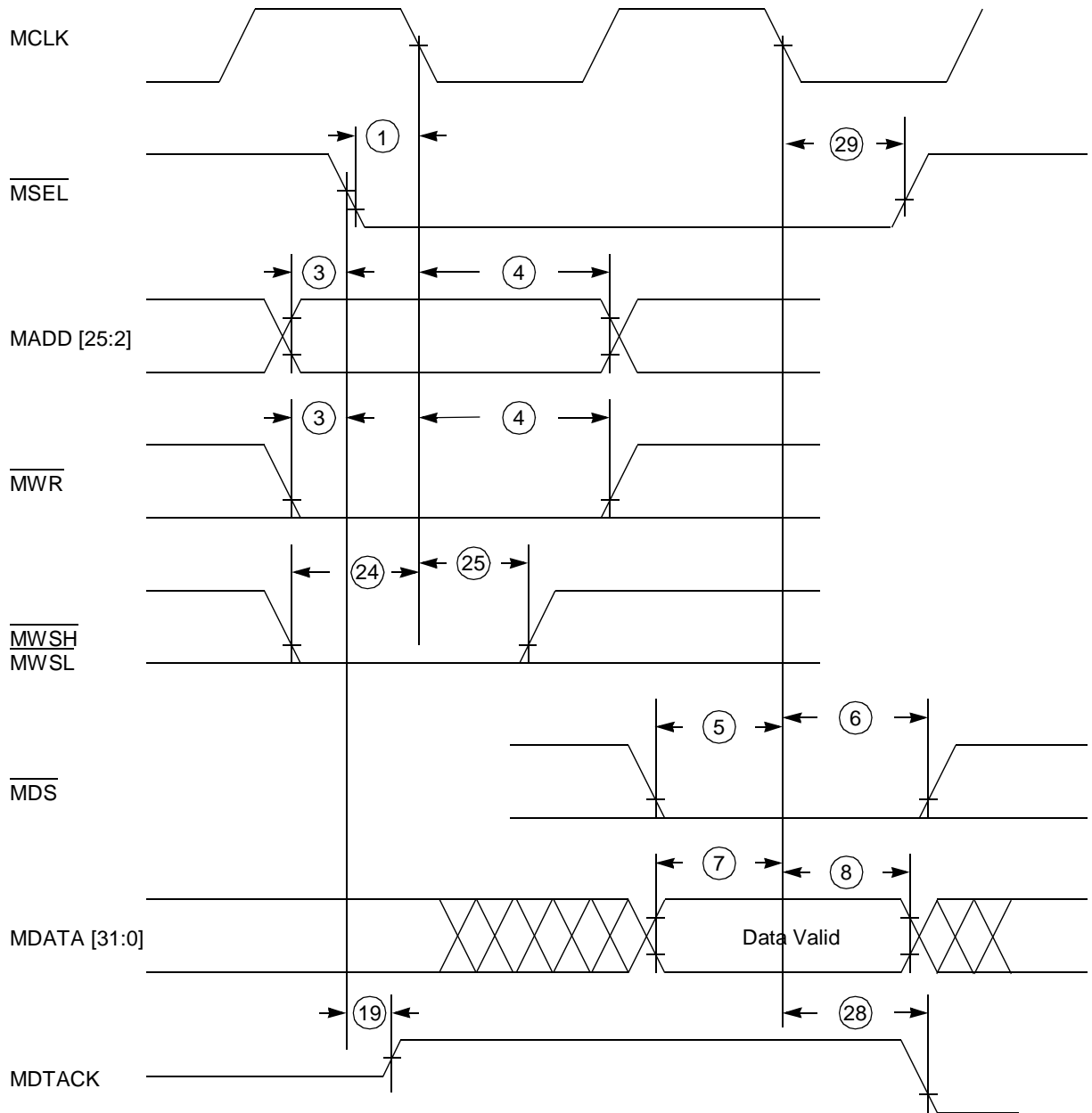


Figure 3-6. General Register Write Access Timing

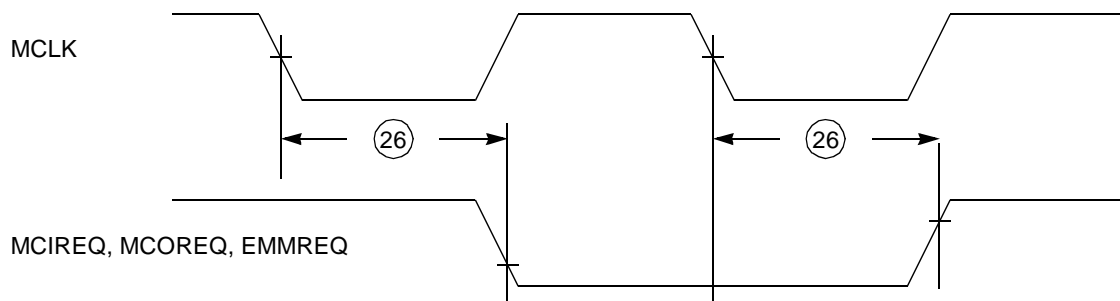


Figure 3-7. DMA Request Signals Timing

3.7 PHY Interface Timing

Table 3-6. PHY Interface Timings

| Num | Characteristics | Min | Max | Unit |
|-----|---|-----|-----------------|------|
| 51 | Setup time before ACLK rising edge | 10 | — | ns |
| 52 | Hold time after ACLK rising edge | 1 | — | ns |
| 53 | Propagation delay from rising edge of ACLK ¹ | 1 | 16 ² | ns |

Notes: 1. For a 200 pF load. Add 0.25 ns for each additional 10 pF. For 100 pF subtract 2.5 ns.
 2. 16 ns for 70°C, 17 ns for 85°C

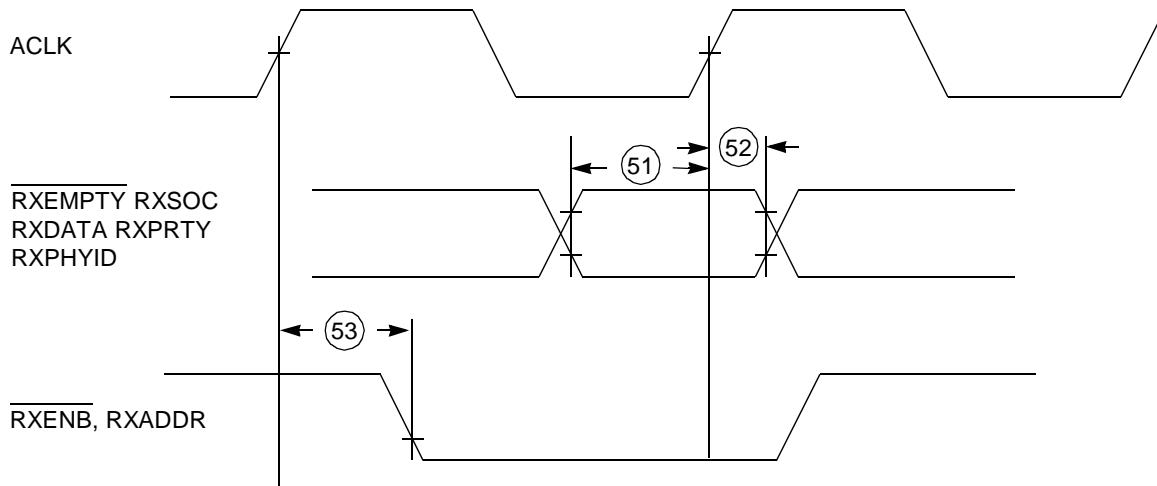


Figure 3-8. Receive PHY Interface Timing

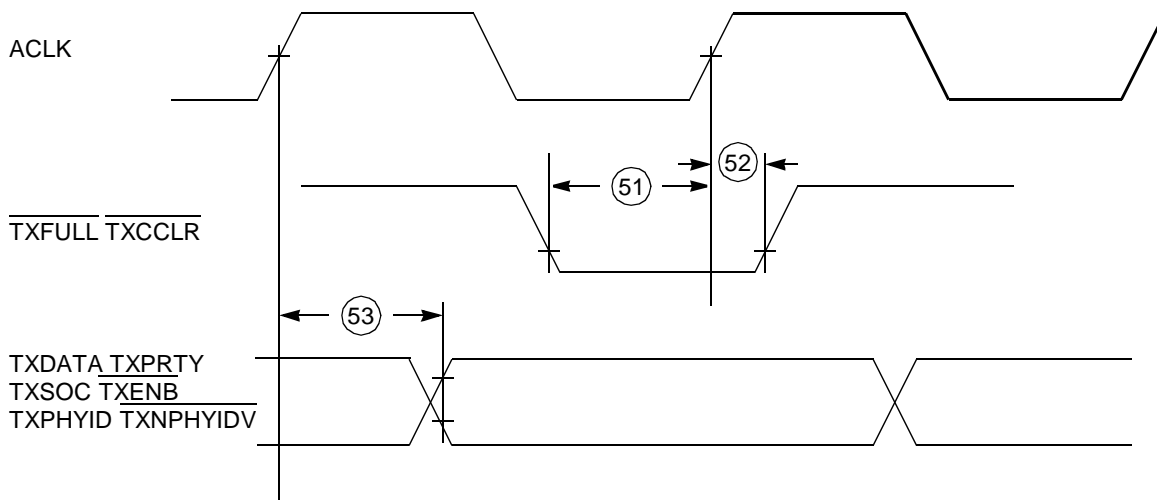


Figure 3-9. Transmit PHY Interface Timing

3.8 Switch Interface Timing

Table 3-7. Switch Interface Timing

| Num | Characteristics | Min | Max | Unit |
|-----|---|-----|-----|------|
| 61 | Setup time before SRXCLK/STXCLK rising edge | 4 | | ns |
| 62 | Hold time after SRXCLK/STXCLK rising edge | 1 | | ns |
| 63 | Propagation delay from rising edge of SRXCLK/STXCLK | 1 | 18 | ns |
| 64 | SRXCLK rising edge to outputs active | 1 | | |
| 65 | SRXCLK rising edge to outputs inactive | 1 | 16 | |

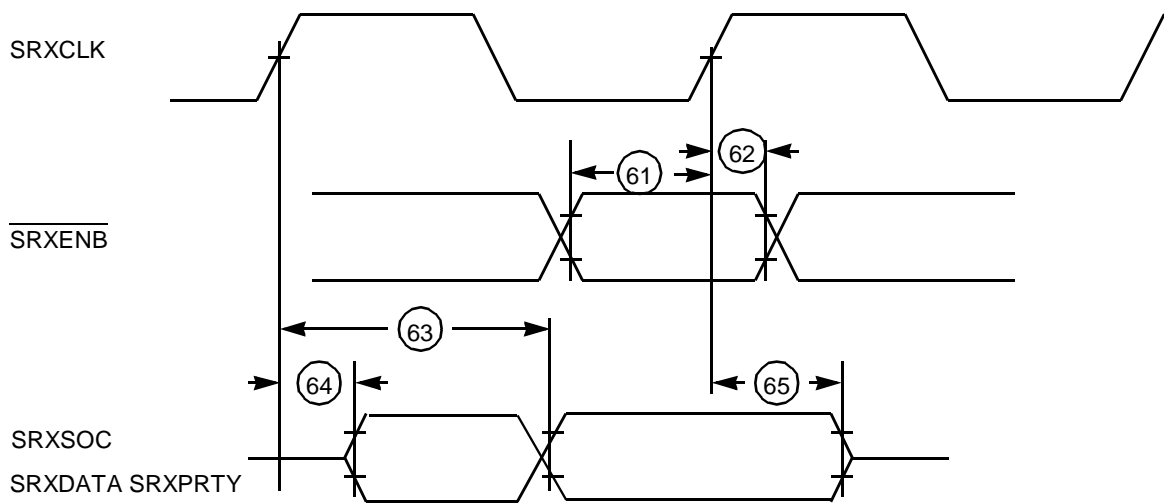


Figure 3-10. Ingress Switch Interface Timing

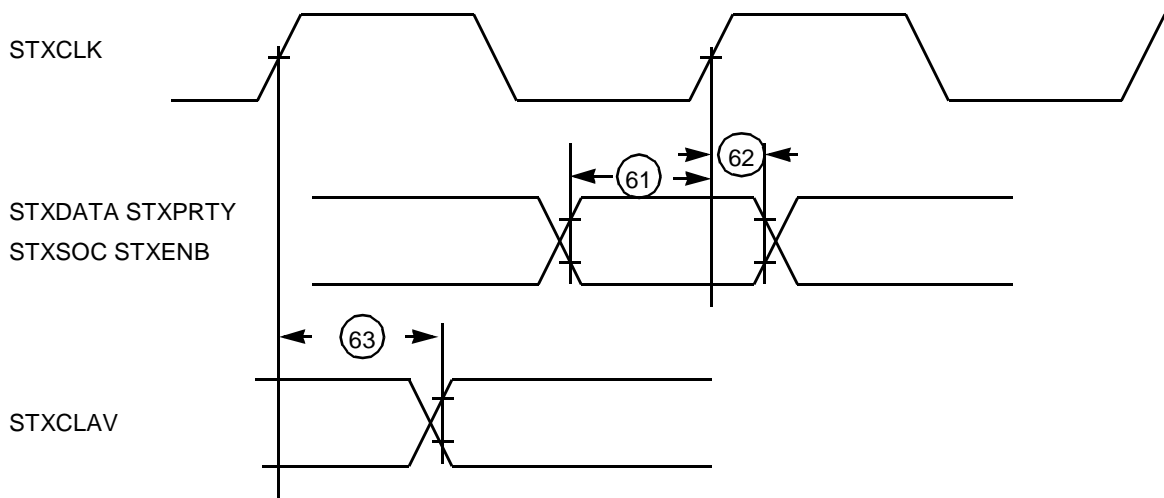


Figure 3-11. Egress Switch Interface Timing

3.9 External Memory Interface Timing

This section represents External Memory timing parameters for the default definition of the External Memory Timing Configuration Register (EMTCR). These values are for a load of up to 50 pF, which is the rated maximum load for the External Memory interface pins.

3.9.1 Write Cycle Timing

Table 3-8. Write Cycle Timing

| Num | Characteristics | Min | Max | Unit |
|---|--|-----|-----|------|
| 81 | Write Pulse Width | 16 | — | ns |
| 82 | $\overline{\text{EMWR}}$ assertion time. $\overline{\text{EMWR}}$ low to end of Write. | 22 | — | ns |
| 83 | Address Setup Time. EMADD Valid to Beginning of Write. | 6 | — | ns |
| 84 | Address Valid Time. During this Time EMADD is Valid. | 32 | — | ns |
| 85 | Address Hold Time. End of Write to EMADD Invalid. | 6 | — | ns |
| 87 | Data Setup Time. EMDATA Valid to End of Write. | 13 | — | ns |
| 88 | Data Hold Time. End of Write to EMDATA Invalid. | 6 | — | ns |
| Note: A write occurs during the overlap of $\overline{\text{EMBSH0-3}}$, $\overline{\text{EMBSL0-3}}$, $\overline{\text{EACEN}}$ low and $\overline{\text{EMWR}}$ low. | | | | |

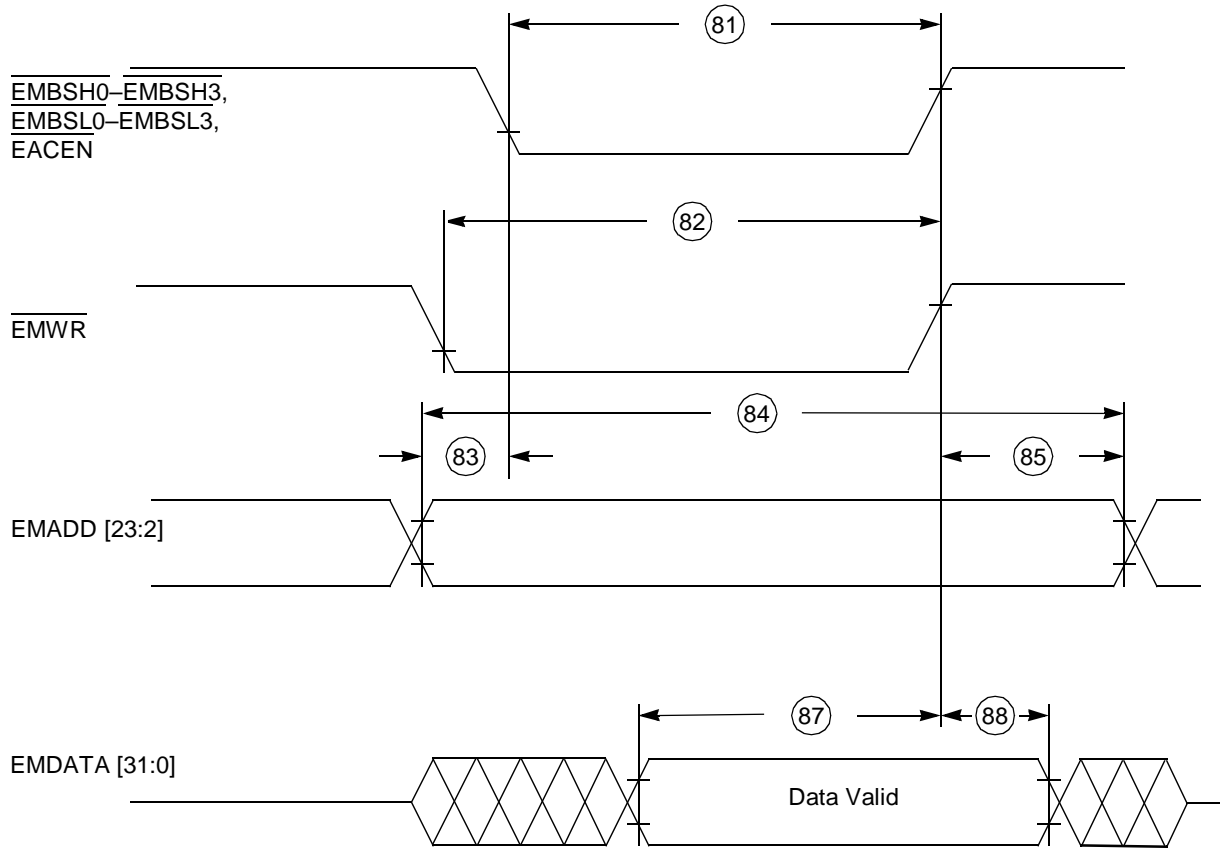


Figure 3-12. External Memory Write Access Timing

3.9.2 Read Cycle Timing

Table 3-9. Read Cycle Timing

| Num | Characteristics | Min | Max | Unit |
|-----|--|-----|----------------|------|
| 90 | Enable Pulse Width. $\overline{\text{EMB}}\text{SH}0\text{--}\overline{\text{EMB}}\text{SH}3$, $\overline{\text{EMB}}\text{SL}0\text{--}\overline{\text{EMB}}\text{SL}3$, $\overline{\text{EAC}}\text{EN}$ Pulse Width. | 28 | — | ns |
| 92 | Address Setup Time. $\overline{\text{EMB}}\text{SH}0\text{--}\overline{\text{EMB}}\text{SH}3$, $\overline{\text{EMB}}\text{SL}0\text{--}\overline{\text{EMB}}\text{SL}3$, $\overline{\text{EAC}}\text{EN}$ High. | 33 | — | ns |
| 93 | Address Hold Time. $\overline{\text{EM}}\text{ADD}$ Invalid to $\overline{\text{EMB}}\text{SH}0\text{--}\overline{\text{EMB}}\text{SH}3$, $\overline{\text{EMB}}\text{SL}0\text{--}\overline{\text{EMB}}\text{SL}3$, $\overline{\text{EAC}}\text{EN}$ High | — | 1 ¹ | ns |
| 94 | Data Driving Start Point. $\overline{\text{EMB}}\text{SH}0\text{--}\overline{\text{EMB}}\text{SH}3$, $\overline{\text{EMB}}\text{SL}0\text{--}\overline{\text{EMB}}\text{SL}3$, $\overline{\text{EAC}}\text{EN}$ Low to $\overline{\text{EM}}\text{DATA}$ Active. | 0 | — | ns |
| 95 | Data Setup Time. $\overline{\text{EM}}\text{DATA}$ Valid to $\overline{\text{EMB}}\text{SH}0\text{--}\overline{\text{EMB}}\text{SH}3$, $\overline{\text{EMB}}\text{SL}0\text{--}\overline{\text{EMB}}\text{SL}3$, $\overline{\text{EAC}}\text{EN}$ High. | 5 | — | ns |
| 96 | Data Hold Time. $\overline{\text{EMB}}\text{SH}0\text{--}\overline{\text{EMB}}\text{SH}3$, $\overline{\text{EMB}}\text{SL}0\text{--}\overline{\text{EMB}}\text{SL}3$, $\overline{\text{EAC}}\text{EN}$ High to $\overline{\text{EM}}\text{DATA}$ Invalid. | 0 | — | ns |
| 97 | Data Driving End Point. $\overline{\text{EMB}}\text{SH}0\text{--}\overline{\text{EMB}}\text{SH}3$, $\overline{\text{EMB}}\text{SL}0\text{--}\overline{\text{EMB}}\text{SL}3$, $\overline{\text{EAC}}\text{EN}$ High to $\overline{\text{EM}}\text{DATA}$ Inactive ² | — | 9 | ns |

- Notes:**
1. A RAM with hold time from address change to data change is required.
 2. Failure to meet this value may result in contention on $\overline{\text{EM}}\text{DATA}$ if a write access follows.

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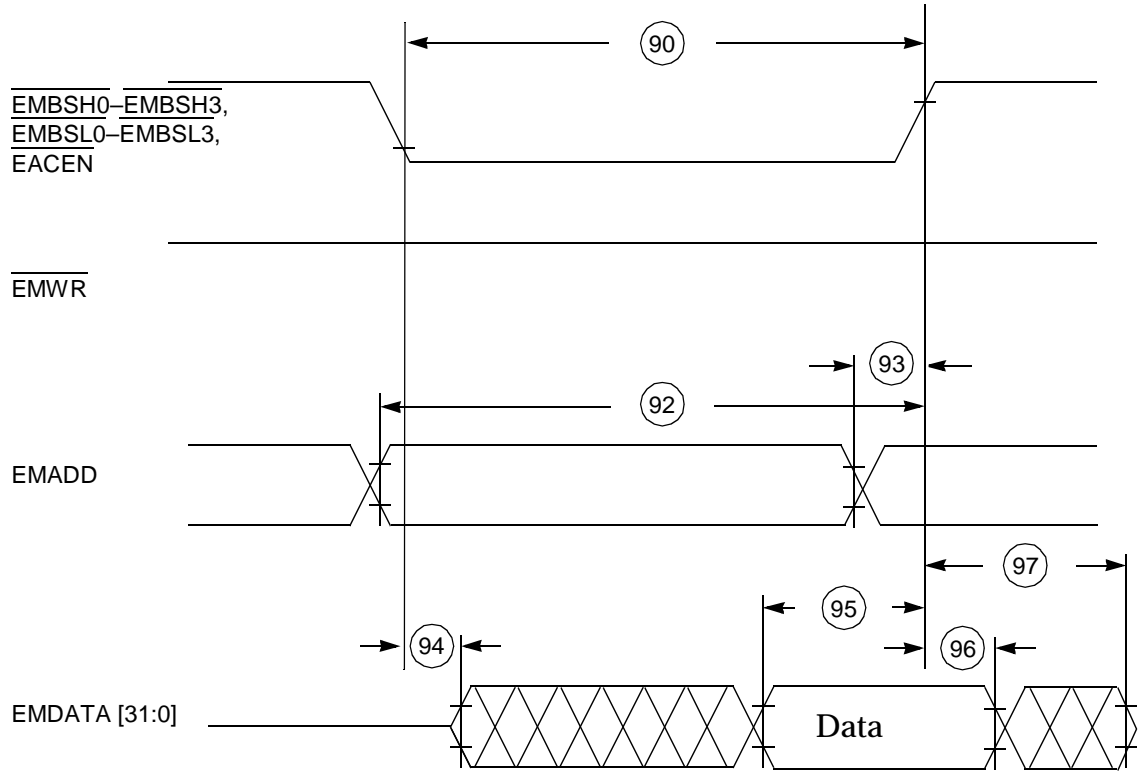


Figure 3-13. External Memory Read Access Timing

Test Information

4.1 Device Identification Register

The code for the MC92501 is 0100_0001_1100_0011_1010_0000_0001_1101.

4.2 Boundary Scan Register

Table 4-1. MC92501 Boundary Scan Bit Definition

| Signal Name | I/O Cell Type | System Mode | Scan Bit # | | Output Enable |
|-------------|---------------|-------------|------------|-----|---------------|
| STXCLK | in | in | 360 | — | — |
| STXCLAV | bidir | out | 359 | 358 | — |
| STXSOC | bidir | in | 357 | 356 | — |
| STXPRTY | bidir | in | 355 | 354 | — |
| STXDATA7 | bidir | in | 353 | 352 | — |
| STXDATA6 | bidir | in | 351 | 350 | — |
| STXDATA5 | bidir | in | 349 | 348 | — |
| STXDATA4 | bidir | in | 347 | 346 | — |
| STXDATA3 | bidir | in | 345 | 344 | — |
| STXDATA2 | bidir | in | 343 | 342 | — |
| STXDATA1 | bidir | in | 341 | 340 | — |
| STXDATA0 | bidir | in | 339 | 338 | — |
| STXENB | bidir | in | 337 | 336 | — |
| TXENB | bidir | out | 335 | 334 | — |
| TXFULL | in | in | 333 | — | — |
| TXCCLR | bidir | in | 332 | 331 | — |

Table 4-1. MC92501 Boundary Scan Bit Definition (Continued)

| Signal Name | I/O Cell Type | System Mode | Scan Bit # | | Output Enable |
|-------------|---------------|-------------|------------|-----|---------------|
| | | | | | |
| TXPHYIDV | tri-state | out | 330 | — | — |
| TXPRTY | bidir | out | 329 | 328 | — |
| TXSOC | bidir | out | 327 | 326 | — |
| TXDATA7 | bidir | out | 325 | 324 | — |
| TXDATA6 | bidir | out | 323 | 322 | — |
| TXDATA5 | bidir | out | 321 | 320 | — |
| TXDATA4 | bidir | out | 319 | 318 | — |
| TXDATA3 | bidir | out | 317 | 316 | — |
| TXDATA2 | bidir | out | 315 | 314 | — |
| TXDATA1 | bidir | out | 313 | 312 | — |
| TXDATA0 | bidir | out | 311 | 310 | — |
| TXPHYID3 | tri-state | out | 309 | — | — |
| TXPHYID2 | tri-state | out | 308 | — | — |
| TXPHYID1 | tri-state | out | 307 | — | — |
| TXPHYID0 | tri-state | out | 306 | — | — |
| MDATA31 | bidir | bidir | 305 | 304 | enscan1 |
| MDATA30 | bidir | bidir | 303 | 302 | enscan1 |
| MDATA29 | bidir | bidir | 301 | 300 | enscan1 |
| MDATA28 | bidir | bidir | 299 | 298 | enscan1 |
| MDATA27 | bidir | bidir | 297 | 296 | enscan1 |
| MDATA26 | bidir | bidir | 295 | 294 | enscan1 |
| MDATA25 | bidir | bidir | 293 | 292 | enscan1 |
| MDATA24 | bidir | bidir | 291 | 290 | enscan1 |
| MDATA23 | bidir | bidir | 289 | 288 | enscan1 |
| MDATA22 | bidir | bidir | 287 | 286 | enscan1 |
| MDATA21 | bidir | bidir | 285 | 284 | enscan1 |
| MDATA20 | bidir | bidir | 283 | 282 | enscan1 |
| MDATA19 | bidir | bidir | 281 | 280 | enscan1 |
| MDATA18 | bidir | bidir | 279 | 278 | enscan1 |

Table 4-1. MC92501 Boundary Scan Bit Definition (Continued)

| Signal Name | I/O Cell Type | System Mode | Scan Bit # | | Output Enable |
|-------------|---------------|-------------|------------|-----|---------------|
| MDATA17 | bidir | bidir | 277 | 276 | enscan1 |
| MDATA16 | bidir | bidir | 275 | 274 | enscan1 |
| MDATA15 | bidir | bidir | 273 | 272 | enscan1 |
| MDATA14 | bidir | bidir | 271 | 270 | enscan1 |
| MDATA13 | bidir | bidir | 269 | 268 | enscan1 |
| MDATA12 | bidir | bidir | 267 | 266 | enscan1 |
| MDATA11 | bidir | bidir | 265 | 264 | enscan1 |
| MDATA10 | bidir | bidir | 263 | 262 | enscan1 |
| MDATA9 | bidir | bidir | 261 | 260 | enscan1 |
| MDATA8 | bidir | bidir | 259 | 258 | enscan1 |
| MDATA7 | bidir | bidir | 257 | 256 | enscan1 |
| MDATA6 | bidir | bidir | 255 | 254 | enscan1 |
| MDATA5 | bidir | bidir | 253 | 252 | enscan1 |
| MDATA4 | bidir | bidir | 251 | 250 | enscan1 |
| MDATA3 | bidir | bidir | 249 | 248 | enscan1 |
| MDATA2 | bidir | bidir | 247 | 246 | enscan1 |
| MDATA1 | bidir | bidir | 245 | 244 | enscan1 |
| MDATA0 | bidir | bidir | 243 | 242 | enscan1 |
| MADD25 | bidir | in | 241 | 240 | — |
| MADD24 | bidir | in | 239 | 238 | — |
| MADD23 | bidir | in | 237 | 236 | — |
| MADD22 | bidir | in | 235 | 234 | — |
| MADD21 | bidir | in | 233 | 232 | — |
| MADD20 | bidir | in | 231 | 230 | — |
| MADD19 | bidir | in | 229 | 228 | — |
| MADD18 | bidir | in | 227 | 226 | — |
| MADD17 | bidir | in | 225 | 224 | — |
| MADD16 | bidir | in | 223 | 222 | — |
| MADD15 | bidir | in | 221 | 220 | — |

Table 4-1. MC92501 Boundary Scan Bit Definition (Continued)

| Signal Name | I/O Cell Type | System Mode | Scan Bit # | | Output Enable |
|-------------|---------------|-------------|------------|---------|---------------|
| | | | | | |
| MADD14 | bidir | in | 219 | 218 | — |
| MADD13 | bidir | in | 217 | 216 | — |
| MADD12 | bidir | in | 215 | 214 | — |
| MADD11 | bidir | in | 213 | 212 | — |
| MADD10 | bidir | in | 211 | 210 | — |
| MADD9 | bidir | in | 209 | 208 | — |
| MADD8 | bidir | in | 207 | 206 | — |
| MADD7 | bidir | in | 205 | 204 | — |
| MADD6 | bidir | in | 203 | 202 | — |
| MADD5 | bidir | in | 201 | 200 | — |
| MADD4 | bidir | in | 199 | 198 | — |
| MADD3 | bidir | in | 197 | 196 | — |
| MADD2 | bidir | in | 195 | 194 | — |
| MSEL | in | in | 193 | — | — |
| MREQ0 | tri-state | out | 192 | — | — |
| MREQ1 | tri-state | out | 191 | — | — |
| MDTACK0 | tri-state | tri-state | 190 | enscan2 | — |
| MINT | tri-state | out | 189 | — | — |
| MREQ2 | tri-state | out | 188 | — | — |
| MCLK | in | in | 187 | — | — |
| MWR | in | in | 186 | — | — |
| MWSH | in | in | 185 | — | — |
| MWSL | in | in | 184 | — | — |
| MDS | in | in | 183can1 | — | — |
| MDATA19 | bid | | | — | — |
| SRXENB | in | in | 182 | — | — |
| SRXDATA7 | bidir | tri-state | 181 | 180 | enscan4 |
| SRXDATA6 | bidir | tri-state | 179 | 178 | enscan4 |
| SRXDATA5 | bidir | tri-state | 177 | 176 | enscan4 |

Table 4-1. MC92501 Boundary Scan Bit Definition (Continued)

| Signal Name | I/O Cell Type | System Mode | Scan Bit # | | Output Enable |
|-------------|---------------|-------------|------------|---------|---------------|
| | | | | | |
| SRXDATA4 | bidir | tri-state | 175 | 174 | enscan4 |
| SRXDATA3 | bidir | tri-state | 173 | 172 | enscan4 |
| SRXDATA2 | bidir | tri-state | 171 | 170 | enscan4 |
| SRXDATA1 | bidir | tri-state | 169 | 168 | enscan4 |
| SRXDATA0 | bidir | tri-state | 167 | 166 | enscan4 |
| SRXCLK | in | in | 165 | enscan4 | — |
| SRXCLAV | bidir | out | 164 | 163 | — |
| SRXSOC | bidir | tri-state | 162 | 161 | enscan4 |
| SRXPRTY | bidir | tri-state | 160 | 159 | enscan4 |
| MDTACK1 | tri-state | tri-state | 158 | enscan6 | — |
| RXADDR4 | tri-state | tri-state | 157 | enscan3 | — |
| RXSOC | bidir | in | 156 | 155 | — |
| RXENB | bidir | out | 154 | 153 | — |
| RXEMPTY | bidir | in | 152 | 151 | — |
| RXPHYID3 | bidir | bidir | 150 | 149 | enscan3 |
| RXPHYID2 | bidir | bidir | 148 | 147 | enscan3 |
| RXPHYID1 | bidir | bidir | 146 | 145 | enscan3 |
| RXPHYID0 | bidir | bidir | 144 | 143 | enscan3 |
| RXPRTY | bidir | in | 142 | 141 | — |
| RXDATA7 | bidir | in | 140 | 139 | — |
| RXDATA6 | bidir | in | 138 | 137 | — |
| RXDATA5 | bidir | in | 136 | 135 | — |
| RXDATA4 | bidir | in | 134 | 133 | — |
| RXDATA3 | bidir | in | 132 | 131 | — |
| RXDATA2 | bidir | in | 130 | 129 | — |
| RXDATA1 | bidir | in | 128 | 127 | — |
| RXDATA0 | bidir | in | 126 | 125 | — |
| EMDATA31 | bidir | bidir | 124 | 123 | enscan5 |
| EMDATA30 | bidir | bidir | 122 | 121 | enscan5 |

Table 4-1. MC92501 Boundary Scan Bit Definition (Continued)

| Signal Name | I/O Cell Type | System Mode | Scan Bit # | | Output Enable |
|-------------|---------------|-------------|------------|-----|---------------|
| EMDATA29 | bidir | bidir | 120 | 119 | enscan5 |
| EMDATA28 | bidir | bidir | 118 | 117 | enscan5 |
| EMDATA27 | bidir | bidir | 116 | 115 | enscan5 |
| EMDATA26 | bidir | bidir | 114 | 113 | enscan5 |
| EMDATA25 | bidir | bidir | 112 | 111 | enscan5 |
| EMDATA24 | bidir | bidir | 110 | 109 | enscan5 |
| EMDATA23 | bidir | bidir | 108 | 107 | enscan5 |
| EMDATA22 | bidir | bidir | 106 | 105 | enscan5 |
| EMDATA21 | bidir | bidir | 104 | 103 | enscan5 |
| EMDATA20 | bidir | bidir | 102 | 101 | enscan5 |
| EMDATA19 | bidir | bidir | 100 | 99 | enscan5 |
| EACEN | tri-state | out | 98 | — | — |
| EMWR | tri-state | out | 97 | — | — |
| EMDATA18 | bidir | bidir | 96 | 95 | enscan5 |
| EMDATA17 | bidir | bidir | 94 | 93 | enscan5 |
| EMDATA16 | bidir | bidir | 92 | 91 | enscan5 |
| EMDATA15 | bidir | bidir | 90 | 89 | enscan5 |
| EMDATA14 | bidir | bidir | 88 | 87 | enscan5 |
| EMDATA13 | bidir | bidir | 86 | 85 | enscan5 |
| EMDATA12 | bidir | bidir | 84 | 83 | enscan5 |
| EMDATA11 | bidir | bidir | 82 | 81 | enscan5 |
| EMDATA10 | bidir | bidir | 80 | 79 | enscan5 |
| EMDATA9 | bidir | bidir | 78 | 77 | enscan5 |
| EMDATA8 | bidir | bidir | 76 | 75 | enscan5 |
| EMDATA7 | bidir | bidir | 74 | 73 | enscan5 |
| EMDATA6 | bidir | bidir | 72 | 71 | enscan5 |
| EMDATA5 | bidir | bidir | 70 | 69 | enscan5 |
| EMDATA4 | bidir | bidir | 68 | 67 | enscan5 |
| EMDATA3 | bidir | bidir | 66 | 65 | enscan5 |

Table 4-1. MC92501 Boundary Scan Bit Definition (Continued)

| Signal Name | I/O Cell Type | System Mode | Scan Bit # | | Output Enable |
|-------------|---------------|-------------|------------|----|---------------|
| EMDATA2 | bidir | bidir | 64 | 63 | enscan5 |
| EMDATA1 | bidir | bidir | 62 | 61 | enscan5 |
| EMDATA0 | bidir | bidir | 60 | 59 | enscan5 |
| EMADD23 | bidir | out | 58 | 57 | — |
| EMADD22 | bidir | out | 56 | 55 | — |
| EMADD21 | bidir | out | 54 | 53 | — |
| EMADD20 | bidir | out | 52 | 51 | — |
| EMADD19 | bidir | out | 50 | 49 | — |
| EMADD18 | bidir | out | 48 | 47 | — |
| EMADD17 | bidir | out | 46 | 45 | — |
| EMADD16 | bidir | out | 44 | 43 | — |
| EMADD15 | bidir | out | 42 | 41 | — |
| EMADD14 | bidir | out | 40 | 39 | — |
| EMADD13 | bidir | out | 38 | 37 | — |
| EMADD12 | bidir | out | 36 | 35 | — |
| EMADD11 | bidir | out | 34 | 33 | — |
| EMADD10 | bidir | out | 32 | 31 | — |
| EMADD9 | bidir | out | 30 | 29 | — |
| EMADD8 | bidir | out | 28 | 27 | — |
| EMADD7 | bidir | out | 26 | 25 | — |
| EMADD6 | bidir | out | 24 | 23 | — |
| EMADD5 | bidir | out | 22 | 21 | — |
| EMADD4 | bidir | out | 20 | 19 | — |
| EMADD3 | bidir | out | 18 | 17 | — |
| EMADD2 | bidir | out | 16 | 15 | — |
| EMBSH0 | tri-state | out | 14 | — | — |
| EMBSH1 | tri-state | out | 13 | — | — |
| EMBSH2 | tri-state | out | 12 | — | — |
| EMBSH3 | tri-state | out | 11 | — | — |

Table 4-1. MC92501 Boundary Scan Bit Definition (Continued)

| Signal Name | I/O Cell Type | System Mode | Scan Bit # | | Output Enable |
|--------------------|----------------------|--------------------|-------------------|---|----------------------|
| EMBSL0 | tri-state | out | 10 | — | — |
| EMBSL1 | tri-state | out | 9 | — | — |
| EMBSL2 | tri-state | out | 8 | — | — |
| EMBSL3 | tri-state | out | 7 | — | — |
| ARST | in | in | 6 | — | — |
| enscan1 | (core macro) | — | 5 | — | — |
| enscan2 | (core macro) | — | 4 | — | — |
| enscan3 | (core macro) | — | 3 | — | — |
| enscan4 | (core macro) | — | 2 | — | — |
| enscan5 | (core macro) | — | 1 | — | — |
| enscan6 | (core macro) | — | 0 | — | — |

Ordering Information


Table 5-1. Ordering Information

| Part | Supply Voltage | Package Type | Pin Count | Order Number |
|-------------|-----------------------|----------------------------------|------------------|---------------------|
| MC92501 | 3.3 V | Glob-Top Ball Grid Array (GTBGA) | 256 | MC92501GC |

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