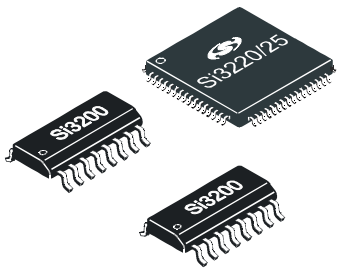
Si3220/Si3225

PRELIMINARY DATA SHEET

DUAL PROSLIC™ PROGRAMMABLE CMOS SLIC/CODEC

Features

- Performs all BORSCHT functions
- Ideal for applications up to 18 kft
- Internal balanced ringing to 65 V_{rms} (Si3220)
- External bulk ringer support (Si3225)
- Low standby power consumption: <65 mW per channel
- Software programmable parameters:
  - Ringing frequency, amplitude, cadence, and waveshape (Si3220)
  - Two-wire ac impedance
  - Transhybrid balance
  - DC current loop feed (18–45 mA)
  - Loop closure and ring trip thresholds
  - Ground key detect threshold
- Automatic switching of up to three battery supplies
- On-hook transmission
- Loop or ground start operation with smooth/abrupt polarity reversal
- Modem/fax tone detection
- DTMF generation/decoding
- Dual tone generators
- A-Law/μ-Law, linear PCM companding
- PCM and SPI bus digital interfaces with programmable interrupts
- GCI/IOM-2 mode support
- 3.3 or 5 V operation
- GR-909 loop diagnostics
- Audio diagnostics with loopback
- 12 kHz/16 kHz pulse metering (Si3220)
- FSK caller ID generation



Part Number	Ringing Method
Si3220	Internal
Si3225	External Ringer

Ordering Information

See page 105.

Patents pending

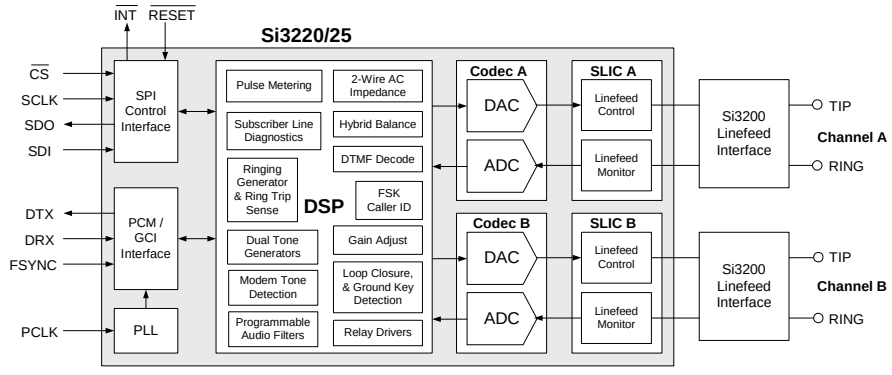
Applications

- Digital loop carriers
- Central Office telephony
- Pair gain remote terminals
- Wireless local loop
- Public Branch Exchange (PBX) systems
- Cable telephony
- Voice over IP/voice over DSL
- ISDN terminal adapters

Description

The Dual ProSLIC is a series of low-voltage CMOS devices that integrate both SLIC and codec functionality into a single IC to provide a complete dual-channel analog telephone interface in accordance with all relevant LSSGR, ITU, and ETSI specifications. The Si3220 includes internal ringing generation to eliminate centralized ringers and ringing relays, and the Si3225 supports centralized ringing for long loop and legacy applications. On-chip subscriber loop and audio testing allows remote diagnostics and fault detection with no external test equipment or relays. The Si3220 and Si3225 operate from a single 3.3 V or 5 V supply and interface to standard PCM/SPI or GCI bus digital interfaces. The Si3200 linefeed interface IC performs all high voltage functions and operates from a 3.3 V or 5 V supply as well as single or dual battery supplies up to 100 V. The Si3220 and Si3225 are available in a 64-pin thin quad flat package (TQFP), and the Si3200 is available in a thermally enhanced 16-pin small outline (SOIC) package.

Functional Block Diagram



Dual ProSLIC Selection Guide

Part Number	Description	On-Chip Ringing	External Ringing Support	Pulse Metering	Temp Range	Package
Si3200-KS	Linefeed interface				0 to 70 °C	SOIC-16
Si3200-BS	Linefeed interface				–40 to 85 °C	SOIC-16
Si3220-KQ	Dual ProSLIC	•		•	0 to 70 °C	TQFP-64
Si3220-BQ	Dual ProSLIC	•		•	–40 to 85 °C	TQFP-64
Si3225-KQ	Dual ProSLIC		•		0 to 70 °C	TQFP-64
Si3225-BQ	Dual ProSLIC		•		–40 to 85 °C	TQFP-64

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Electrical Specifications

Table 1. Absolute Maximum Ratings and Thermal Information[1]

Parameter	Symbol	Test Condition	Value	Unit
Supply Voltage, Si3200 and Si3220/ Si3225	V_{DD}, V_{DD1}–V_{DD4}		–0.5 to 6.0	V
High Battery Supply Voltage, Si3200[2]	V_{BATH}	Continuous	0.4 to –104	V
		10 ms	0.4 to –109	
Low Battery Supply Voltage, Si3200	V_{BAT},V_{BATL}	Continuous	V_{BATH}	V
TIP or RING Voltage, Si3205	V_{TIP},V_{RING}	Continuous Pulse < 10 µs Pulse < 4 µs	–104 V_{BATH} –15 V_{BATH} –35	
TIP, RING Current, Si3200	I_{TIP}, I_{RING}		±100	mA
STIPAC, STIPDC, SRINGAC, SRINGDC Current, Si3220/Si3225			±20	mA
Input Current, Digital Input Pins	I_{IN}	Continuous	±10	mA
Digital Input Voltage	V_{IND}		–0.3 to (V_{DDD} + 0.3)	V
Operating Temperature Range	T_A		–40 to 100	°C
Storage Temperature Range	T_{STG}		–40 to 150	°C
Si3220/Si3225 Thermal Resistance, Typical[3] (TQFP-64 ePad)	θ_{JA}		25	°C/W
Si3200 Thermal Resistance, Typical[3] (SOIC-16 ePad)	θ_{JA}		65	°C/W
Continuous Power Dissipation, Si3200[4]	P_D	T_A = 85 °C, SOIC-16	0.85	W
Continuous Power Dissipation, Si3220/25	P_D	T_A = 85 °C, TQFP-64	1.6	W

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The dv/dt of the voltage applied to the VBAT, VBATH, and VBATL pins must be limited to 10 V/µs.
3. Thermal resistance assumes a multi-layer PCB with the exposed pad soldered to a topside PCB pad.
4. On-chip thermal limiting circuitry will shut down the circuit at a junction temperature of approximately 150 °C. For optimal reliability, operation above 140 °C junction temperature should be avoided.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min*	Typ	Max*	Unit
Ambient Temperature	T_A	K-grade	0	25	70	°C
Ambient Temperature	T_A	B-grade	–40	25	85	°C
Supply Voltage, Si3220/Si3225	V_{DD1}–V_{DD4}		3.13	3.3/5.0	5.25	V
Supply Voltage, Si3200	V_{DD}		3.13	3.3/5.0	5.25	V
High Battery Supply Voltage, Si3200	V_{BATH}		–15	—	–99	V
Low Battery Supply Voltage, Si3200	V_{BATL}		–15	—	V_{BATH}	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.

Table 3. 3.3 V Power Supply Characteristics*

(V_{DD}, V_{DD1}–V_{DD4} = 3.3 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD1}–V_{DD4} Supply Current (Si3220/Si3225)	I_{VDD1}–I_{VDD4}	Sleep mode, RESET = 0	—	1	—	mA
		Open (high-impedance)	—	15	—	mA
		Active on-hook standby	—	15	—	mA
		Forward/reverse active off-hook no I_{LOOP}, ABIAS = 4 mA	—	40	—	mA
		Forward/reverse active OHT OBIAS = 4 mA	—	44	—	mA
		Ringing, V_{RING} = 45 V_{rms}, V_{BAT} = –70 V, Sine Wave, 1 REN load	—	28	—	mA
V_{DD} Supply Current (Si3200)	I_{VDD}	Sleep mode, RESET = 0	—	110	—	µA
		Open (high-impedance)	—	110	—	µA
		Active on-hook standby	—	110	—	µA
		Forward/reverse active off-hook, no I_{LOOP}, ABIAS = 4 mA, V_{BAT} = –24 V	—	110	—	µA
		Forward/reverse OHT, OBIAS = 4 mA, V_{BAT} = –70 V	—	110	—	µA
		Ringing, V_{RING} = 45 V_{rms}, V_{BAT} = –70 V, Sine Wave, 1 REN load	—	110	—	µA

***Note:** All specifications are for a single channel based on measurements with both channels in the same operating state.

Table 3. 3.3 V Power Supply Characteristics* (Continued)

(V_{DD}, V_{DD1}–V_{DD4} = 3.3 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{BAT} Supply Current (Si3200)	I_{VBAT}	Sleep mode, RESET=0, V_{BAT} = –70 V	—	100	—	µA
		Open (high-impedance), V_{BAT} = –70 V	—	225	—	µA
		Active on-hook standby, V_{BAT} = –70 V	—	400	—	µA
		Forward/reverse active off-hook no I_{LOOP}, ABIAS = 4 mA, V_{BAT} = –24 V	—	4.4	—	mA
		Forward/reverse OHT, OBIAS = 4 mA, V_{BAT} = –70 V	—	8.4	—	mA
		Ringing, V_{RING} = 45 V_{rms}, V_{BAT} = –70 V, Sine Wave, 1 REN load	—	6	—	mA
Power Consumption	P_{SLEEP}	Sleep mode, RESET = 0, V_{BAT} = –70 V	—	8	—	mW
	P_{OPEN}	Open (high-impedance), V_{BAT} = –70 V	—	65	—	mW
	P_{STBY}	Active on-hook standby, V_{BAT} = –48 V	—	70	—	mW
	P_{STBY}	Active on-hook standby, V_{BAT} = –70 V	—	80	—	mW
	P_{ACTIVE}	Forward/reverse active off-hook no I_{LOOP}, ABIAS = 4 mA, V_{BAT} = –24 V	—	240	—	mW
	P_{ACTIVE}	Forward/reverse active off-hook, no I_{LOOP}, ABIAS = 4 mA, V_{BAT} = –48 V	—	345	—	mW
	P_{OHT}	Forward/reverse OHT, OBIAS = 4 mA, V_{BAT} = –48 V	—	550	—	mW
	P_{OHT}	Forward/reverse OHT, OBIAS = 4 mA, V_{BAT} = –70 V	—	735	—	mW
	P_{RING}	Ringing, V_{RING} = 45 v_{rms}, V_{BAT} = –70 V, 1 REN load	—	516	—	mW

***Note:** All specifications are for a single channel based on measurements with both channels in the same operating state.

Table 4. 5 V Power Supply Characteristics*

(V_{DD}, V_{DD1}–V_{DD4} = 5 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD1}–V_{DD4} Supply Current (Si3220/Si3225)	I_{VDD1}–I_{VDD4}	Sleep mode, RESET = 0	—	1	—	mA
		Open (high-impedance)	—	20	—	mA
		Active on-hook standby	—	20	—	mA
		Forward/reverse active off-hook no I_{LOOP}, ABIAS = 4 mA	—	56	—	mA
		Forward/reverse active OHT OBIAS = 4 mA	—	60	—	mA
		Ringing, V_{RING} = 45 V_{rms}, V_{BAT} = –70 V, 1 REN load	—	32	—	mA
V_{DD} Supply Current (Si3200)	I_{VDD}	Sleep mode, RESET = 0	—	110	—	µA
		Open (high-impedance)	—	110	—	µA
		Active on-hook standby	—	110	—	µA
		Forward/reverse active off-hook, no I_{LOOP}, ABIAS = 4 mA, V_{BAT} = –24 V	—	110	—	mA
		Forward/reverse OHT, OBIAS = 4 mA, V_{BAT} = –70 V	—	110	—	mA
		Ringing, V_{RING} = 45 V_{rms}, V_{BAT} = –70 V, 1 REN load	—	110	—	mA
V_{BAT} Supply Current (Si3200)	I_{VBAT}	Sleep mode, RESET=0, V_{BAT} = –70 V	—	100	—	µA
		Open (high-impedance), V_{BAT} = –70 V	—	225	—	µA
		Active on-hook standby, V_{BAT} = –70 V	—	400	—	µA
		Forward/reverse active off-hook no I_{LOOP}, ABIAS = 4 mA, V_{BAT} = –24 V	—	4.4	—	mA
		Forward/reverse OHT, OBIAS = 4 mA, V_{BAT} = –70 V	—	8.4	—	mA
		Ringing, V_{RING} = 45 V_{rms}, V_{BAT} = –70 V, 1 REN load	—	6	—	mA

***Note:** All specifications are for a single channel based on measurements with both channels in the same operating state.

Table 4. 5 V Power Supply Characteristics* (Continued)

(V_{DD}, V_{DD1}–V_{DD4} = 5 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Consumption	P_{SLEEP}	Sleep mode, RESET = 0, V_{BAT} = –70 V	—	12	—	mW
	P_{OPEN}	Open (high-impedance), V_{BAT} = –70 V	—	115	—	mW
	P_{STBY}	Active on-hook standby, V_{BAT} = –48 V	—	120	—	mW
	P_{STBY}	Active on-hook standby, V_{BAT} = –70 V	—	130	—	mW
	P_{ACTIVE}	Forward/reverse active off-hook no I_{LOOP}, ABIAS = 4 mA, V_{BAT} = –24 V	—	385	—	mW
	P_{ACTIVE}	Forward/reverse active off-hook, no I_{LOOP}, ABIAS = 4 mA, V_{BAT} = –48 V	—	490	—	mW
	P_{OHT}	Forward/reverse OHT, OBIAS = 4 mA, V_{BAT} = –48 V	—	700	—	mW
	P_{OHT}	Forward/reverse OHT, OBIAS = 4 mA, V_{BAT} = –70 V	—	890	—	mW
	P_{RING}	Ringing, V_{RING} = 45 V_{rms}, V_{BAT} = –70 V, 1 REN load	—	585	—	mW

***Note:** All specifications are for a single channel based on measurements with both channels in the same operating state.

Table 5. AC Characteristics

(V_{DD}, V_{DD1}–V_{DD4} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Level		2.5	—	—	V_{PK}
Overload Compression	2-Wire – PCM	Figure 6	—	—	
Single Frequency Distortion[1]	2-Wire – PCM or PCM – 2-Wire: 200 Hz to 3.4 kHz	—	—	–65	dB
	PCM – 2-Wire – PCM: 200 Hz – 3.4 kHz, 16-bit Linear mode	—	—	–65	dB
Signal-to-(Noise + Distortion) Ratio[2]	200 Hz to 3.4 kHz D/A or A/D 8-bit Active off-hook, and OHT, any Z_T	Figure 5	—	—	
Audio Tone Generator Signal-to-Distortion Ratio[2]	0 dBm0, Active off-hook, and OHT, any Z_T	46	—	—	dB
Intermodulation Distortion		—	—	–41	dB
Gain Accuracy[2]	2-Wire to PCM or PCM to 2-Wire 1014 Hz, Any gain setting				
	$V_{DD1} – V_{DD4}$ = 3.3 V ± 5%	–0.25	—	+0.25	dB
	$V_{DD1} – V_{DD4}$ = 5 V ± 5%	–0.1	—	+ 0.4	dB
Attenuation Distortion vs. Freq.	0 dBm 0	Figure 7,8	—	—	—
Group Delay vs. Frequency		Figure 9	—	—	—
Gain Tracking[3]	1014 Hz sine wave, reference level –10 dBm Signal level:	—	—	—	—
	3 dB to –37 dB	—	—	± 0.25	dB
	–37 dB to –50 dB	—	—	± 0.5	dB
	–50 dB to –60 dB	—	—	± 1.0	dB
Round-Trip Group Delay	1014 Hz, Within same time-slot	—	450	500	µs
Crosstalk between channels TX or RX to TX TX or RX to RX	0 dBm0, 300 Hz to 3.4 kHz 300 Hz to 3.4 kHz	— —	— —	–75 –75	dB dB
Gain Step Increment[4]	Step size around 0 dB	—	±0.0005	—	dB
2-Wire Return Loss[5]	200 Hz to 3.4 kHz	26	30	—	dB

Notes:

1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency will be smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. The digital gain block is a linear multiplier that is programmable from –∞ to +6 dB. The step size in dB varies over the complete range. See “Audio Path Processing”.
5. V_{DD1}–V_{DD4} = 3.3 V, V_{BAT} = –52 V, no fuse resistors, R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
6. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
7. The OBIAS and ABIAS registers program the dc bias current through the SLIC in the on-hook transmission and off-hook active conditions, respectively. This per-pin total current setting should be selected so it can accommodate the sum of the metallic and longitudinal currents through each of the TIP and RING leads for a given application.

Table 5. AC Characteristics (Continued)

(V_{DD}, V_{DD1}–V_{DD4} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
Transhybrid Balance[5]	300 Hz to 3.4 kHz	34	40	—	dB
Noise Performance					
Idle Channel Noise[6]	C-Message weighted	—	12	15	dBrnC
	Psophometric weighted	—	–78	–75	dBmP
	3 kHz flat	—	—	18	dBrn
PSRR from V_{DD1}–V_{DD4}	RX and TX, dc to 3.4 kHz	40	—	—	dB
Longitudinal Performance					
Longitudinal to Metallic/PCM Balance (forward or reverse)	200 Hz to 1 kHz	58	63	—	dB
	1 kHz to 3.4 kHz	53	58	—	dB
Metallic/PCM to Longitudinal Balance	200 Hz to 3.4 kHz	40	—	—	dB
Longitudinal Impedance[7]	200 Hz to 3.4 kHz at TIP or RING Register-dependent OBIAS/ABIAS				
	00 = 4 mA	—	50	—	Ω
	01 = 8 mA	—	25	—	Ω
	10 = 12 mA	—	25	—	Ω
	11 = 16 mA	—	20	—	Ω
Longitudinal Current per Pin[7]	Active off-hook 200 Hz to 3.4 kHz Register-dependent OBIAS/ABIAS				
	00 = 4 mA	—	4	—	mA
	01 = 8 mA	—	8	—	mA
	10 = 12 mA	—	8	—	mA
	11 = 16 mA	—	10	—	mA

Notes:

1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency will be smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} - V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the μ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. The digital gain block is a linear multiplier that is programmable from –∞ to +6 dB. The step size in dB varies over the complete range. See “Audio Path Processing”.
5. V_{DD1}–V_{DD4} = 3.3 V, V_{BAT} = –52 V, no fuse resistors, R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
6. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
7. The OBIAS and ABIAS registers program the dc bias current through the SLIC in the on-hook transmission and off-hook active conditions, respectively. This per-pin total current setting should be selected so it can accommodate the sum of the metallic and longitudinal currents through each of the TIP and RING leads for a given application.

Table 6. Linefeed Characteristics

(V_{DD}, V_{DD1}–V_{DD4} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Loop Resistance	R_{LOOP}	$R_{DC,MAX}$ = 430 Ω, I_{LOOP} = 18 mA, V_{BAT} = –52 V, ABIAS = 8 mA	1600	—	—	Ω
DC Loop Current Accuracy		I_{LIM} = 18 mA	—	—	±10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} – V_{RING}$	—	—	±4	V
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	—	320	—	Ω
DC On-Hook Voltage Accuracy—Ground Start	V_{OHTO}	$I_{RING}<I_{LIM}$; V_{RING} wrt ground, V_{RING} = –51 V	—	—	±4	V
DC Output Resistance—Ground Start	R_{ROTO}	$I_{RING}<I_{LIM}$; RING to ground	—	320	—	Ω
DC Output Resistance—Ground Start	R_{TOTO}	TIP to ground	300	—	—	kΩ
Loop Closure Detect Threshold Accuracy		I_{THR} = 13 mA	—	±10	±15	%
Ground Key Detect Threshold Accuracy		I_{THR} = 13 mA	—	±10	±15	%
Ring Trip Threshold Accuracy		Si3220, ac detection, VRING = 70 Vpk, no offset, I_{TH} = 80mA	—	±4	±5	mA
		Si3220, dc detection, 20 V dc offset, I_{TH} = 13 mA	—	±1.5	±2	mA
		Si3225, dc Detection, 48 V dc offset, R_{loop} = 1500 Ω	—	—	±4.5	mA
Ringing Amplitude, Si3220*	V_{RING}	Open circuit, V_{BATH} = 100 V	93	—	—	V_{PK}
		5 REN load, R_{LOOP} = 0 Ω, V_{BATH} = 100 V	82	—	—	V_{PK}
Sinusoidal Ringing Total Harmonic Distortion	R_{THD}		—	2	—	%
Ringing Frequency Accuracy		f = 16 Hz to 100 Hz	—	—	±1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF times	—	—	±50	ms
Calibration Time		↑CAL to ↓CAL bit	—	—	600	ms
Loop Voltage Sense Accuracy		Accuracy of boundaries for each output code; $V_{TIP} – V_{RING}$ = 48 V	—	±2	±4	%

Table 6. Linefeed Characteristics (Continued)

(V_{DD}, V_{DD1}–V_{DD4} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Loop Current Sense Accuracy		Accuracy of boundaries for each output code; I_{LOOP} = 18 mA	—	±7	±10	%
Power Alarm Threshold Accuracy		Power Threshold = 300 mW	—	—	±25	%
***Note:** Ringing amplitude is set for 93 V peak using the RINGAMP RAM address and measured at TIP-RING using no series protection resistance.						

Table 7. Monitor ADC Characteristics

(V_{DD}, V_{DD1}–V_{DD4} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity (8-bit resolution)	DNLE		—	—	±1	LSB
Integral Nonlinearity (8-bit resolution)	INLE		—	—	±1	LSB
Gain Error			—	—	10	%

Table 8. Si3200 Characteristics

(V_{DD} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TIP/RING Pulldown Transistor Saturation Voltage	V_{OV}	$V_{RING} – V_{BAT}$ (Forward) $V_{TIP} – V_{BAT}$ (Reverse) I_{LIM} = 22 mA, I_{ABIAS} = 4 mA* I_{LIM} = 45 mA, I_{ABIAS} = 16 mA*	 — —	 3 4	 — —	 V V
TIP/RING Pullup Transistor Saturation Voltage	V_{CM}	GND – V_{TIP} (Forward) GND – V_{RING} (Reverse) I_{LIM} = 22 mA* I_{LIM} = 45 mA*	 — —	 3 4	 — —	 V V
Battery Switch Saturation Impedance	R_{SAT}	$V_{BAT} – V_{BATH}$, I_{OUT} = 60 mA	—	15	—	Ω
OPEN State TIP/RING Leakage Current	I_{LKG}	R_L = 0Ω	—	—	100	µA
Internal Blocking Diode Forward Voltage	V_F	$V_{BAT} – V_{BATL}$, I_{OUT} = 60 mA	—	0.8	—	V
***Note:** V_{BATL} = –24 V, V_{TIP} = –4 V, V_{RING} = –15 V, V_{AC} = 2.5 V_{PK}, R_{LOAD} = 600 Ω.						

Table 9. DC Characteristics (V_{DD}, V_{DD1}–V_{DD4} = 5 V)

(V_{DD}, V_{DD1}–V_{DD4} = 4.75 V to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		0.7 x V_{DD}	—	5.25	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{DD}	V
High Level Output Voltage	V_{OH}	I_O = 8 mA	V_{DD} – 0.6	—	—	V
Low Level Output Voltage	V_{OL}	DTX, SDO, $\overline{INT}$, SDITHRU: I_O = –8 mA	—	—	0.4	V
		BATSELa/b, RRDa/b, GPOa/b, TRD1a/b,TRD2a/b: I_O = –40 mA	—	—	0.72	V
SDITHRU Internal Pullup Resistance			20	30	—	kΩ
Relay Driver Source Impedance	R_{OUT}	V_{DD1}–V_{DD4} = 4.75 V I_O < 28 mA	—	63	—	Ω
Relay Driver Sink Impedance	R_{IN}	V_{DD1}–V_{DD4} = 4.75 V I_O < 85 mA	—	11	—	Ω
Input Leakage Current	I_L		—	—	±10	µA

Table 10. DC Characteristics (V_{DD}, V_{DD1}–V_{DD4} = 3.3 V)

(V_{DD}, V_{DD1}–V_{DD4} = 3.13 V to 3.47 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		0.7 x V_{DD}	—	5.25	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{DD}	V
High Level Output Voltage	V_{OH}	I_O = 4 mA	V_{DD} – 0.6	—	—	V
Low Level Output Voltage	V_{OL}	DTX, SDO, $\overline{INT}$, SDITHRU: I_O = –4 mA	—	—	0.4	V
		BATSELa/b, RRDa/b, GPOa/b, TRD1a/b, TRD2a/b: I_O = –40 mA	—	—	0.72	
SDITHRU internal pullup resistance			35	50	—	kΩ
Relay Driver Source Impedance	R_{OUT}	V_{DD1}–V_{DD4} = 3.13 V IO < 28 mA	—	63	—	Ω
Relay Driver Sink Impedance	R_{IN}	V_{DD1}–V_{DD4} = 3.13 V IO < 85 mA	—	11	—	Ω
Input Leakage Current	I_L		—	—	±10	µA

Table 11. Switching Characteristics—General Inputs[1]

(V_{DD}, V_{DD1}–V_{DD4} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time, $\overline{\text{RESET}}$	t_r	—	—	5	ns
$\overline{\text{RESET}}$ Pulse Width, GCI Mode[2]	t_{rl}	500	—	—	ns
$\overline{\text{RESET}}$ Pulse Width, SPI Daisy Chain Mode	t_{rl}	6	—	—	µs

Notes:
1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DD} – 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
2. The minimum $\overline{\text{RESET}}$ pulse width assumes the SDITHRU pin is tied to ground via a pulldown resistor no greater than 10 kΩ per device.

Table 12. Switching Characteristics—SPI

(V_{DD}, V_{DD1}–V_{DD4} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade, C_L = 20 pF)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time SCLK	t_c		0.062	—	—	µs
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	20	ns
Delay Time, $\overline{\text{CS}}$ Rise to SDO Tristate	t_{d3}		—	—	20	ns
Setup Time, $\overline{\text{CS}}$ to SCLK Rise	t_{su1}		15	—	—	ns
Hold Time, SCLK Rise to $\overline{\text{CS}}$ Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SCLK Rise to SDI Rise	t_{h2}		20	—	—	ns
SDI to SDITHRU Propagation Delay			—	6	—	ns

Note: All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} – V_{DD} –0.4 V, V_{IL} = 0.4 V

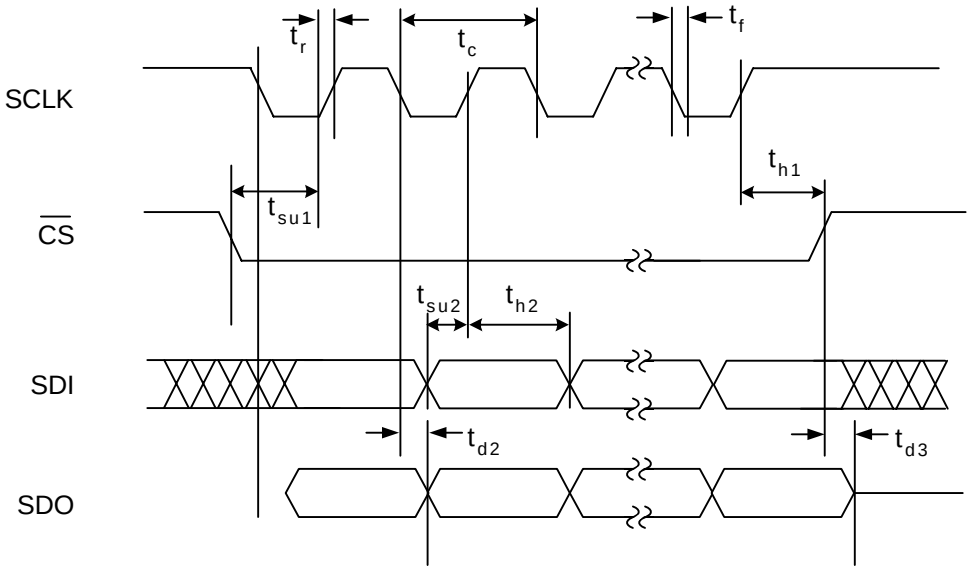


Figure 1. SPI Timing Diagram

Table 13. Switching Characteristics—PCM Highway Interface

(V_{DD}, V_{DD1}–V_{DD4} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade, C_L = 20 pF)

Parameter	Symbol	Test Conditions	Min[1]	Typ[1]	Max[1]	Units
PCLK Period	t_p		122	—	3906	ns
Valid PCLK Inputs			— — — — — — — — —	256 512 768 1.024 1.536 1.544 2.048 4.096 8.192	— — — — — — — — —	kHz kHz kHz MHz MHz MHz MHz MHz MHz
FSYNC Period[2]	t_{fs}		—	125	—	µs
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
FSYNC Jitter Tolerance	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns

Table 13. Switching Characteristics—PCM Highway Interface (Continued)
(V_{DD}, V_{DD1}–V_{DD4} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade, C_L = 20 pF)

Parameter	Symbol	Test Conditions	Min[1]	Typ[1]	Max[1]	Units
Delay Time, PCLK Rise to DTX Tristate[3]	t_{d3}		—	—	20	ns
Setup Time, FSYNC to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, FSYNC to PCLK Fall	t_{h1}		20	—	—	ns
Setup Time, DRX to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, DRX to PCLK Fall	t_{h2}		20	—	—	ns
FSYNC Pulse Width	t_{wfs}		t_p	—	125 µs–t_p	

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} _ $V_{I/O}$ _0.4 V, V_{IL} = 0.4 V.
2. FSYNC source is assumed to be 8 kHz under all operating conditions.
3. Spec applies to PCLK fall to DTX tristate when that mode is selected.

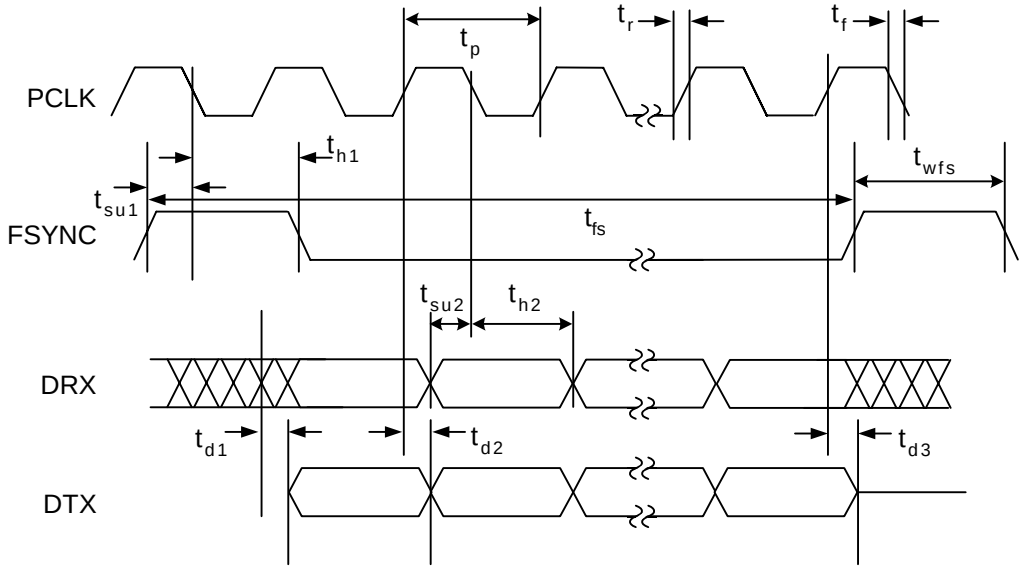


Figure 2. PCM Highway Interface Timing Diagram

Table 14. Switching Characteristics—GCI Highway Serial Interface

(V_{DD}, V_{DD1}–V_{DD4} = 3.13 to 5.25 V, T_A = 0 to 70 °C for K-Grade, –40 to 85 °C for B-Grade)

Parameter[1]	Symbol	Test Conditions	Min	Typ	Max	Units
PCLK Period (2.048 MHz PCLK Mode)	t_p		—	488	—	ns
PCLK Period (4.096 MHz PCLK Mode)	t_p		—	244	—	ns
FSYNC Period[2]	t_{fs}		—	125	—	µs
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
FSYNC Jitter Tolerance	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tristate[3]	t_{d3}		—	—	20	ns
Setup Time, $\overline{\text{FSYNC}}$ Rise to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, PCLK Fall to FSYNC Fall	t_{h1}		20	—	—	ns
Setup Time, DRX Transition to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, PCLK Falling to DRX Transition	t_{h2}		20	—	—	ns
FSYNC Pulse Width	t_{wfs}		t_p	—	—	ns

Notes:

1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_O – 0.4$ V, V_{IL} = 0.4 V, rise and fall times are referenced to the 20% and 80% levels of the waveform.
2. FSYNC source is assumed to be 8 kHz under all operating conditions.
3. Specification applies to PCLK fall to DTX tristate when that mode is selected.

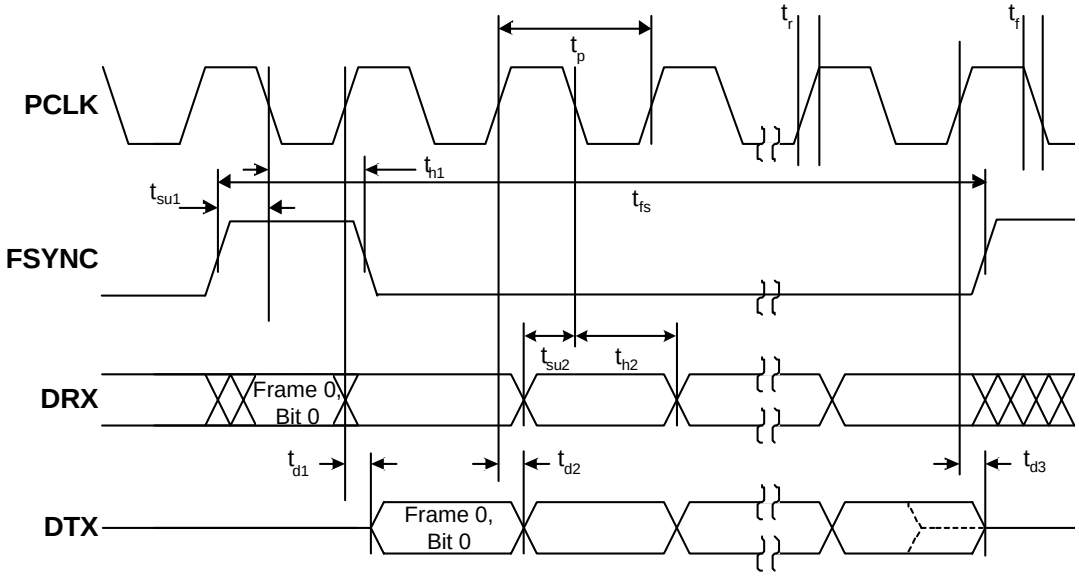


Figure 3. GCI Highway Interface Timing Diagram (2.048 MHz PCLK Mode)

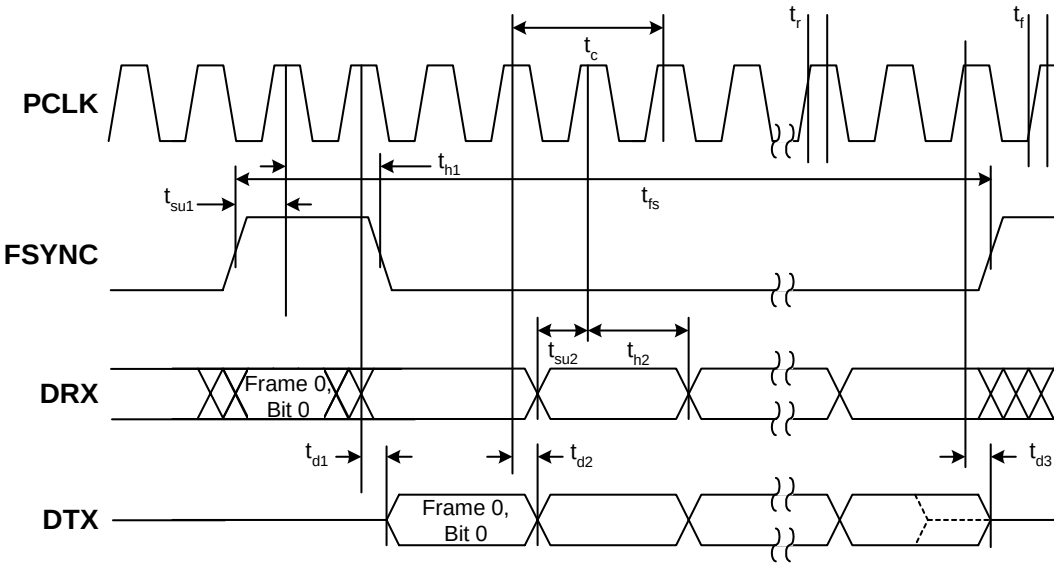


Figure 4. GCI Highway Interface Timing Diagram (4.096 MHz PCLK Mode)

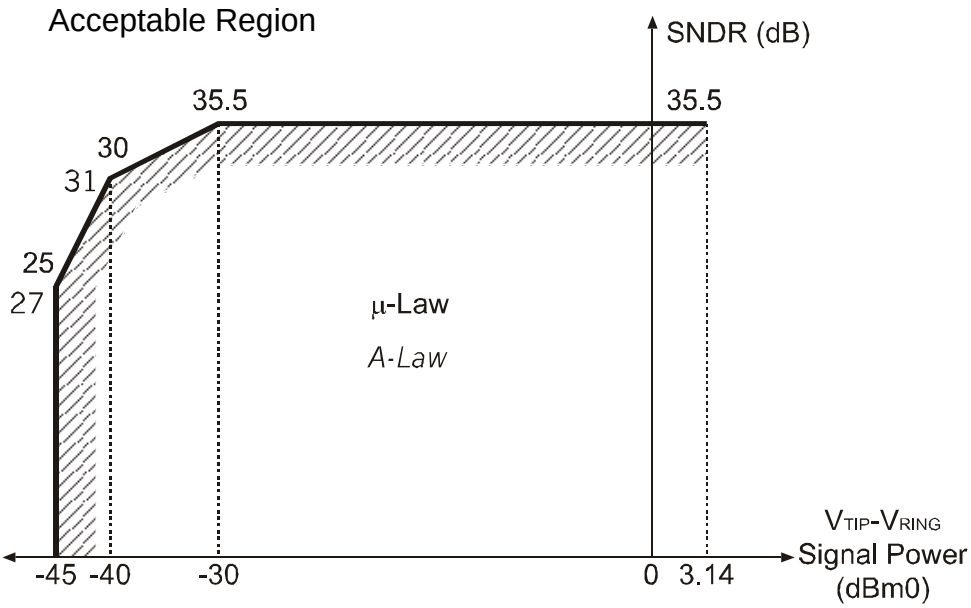


Figure 5. Transmit and Receive Path SNDR

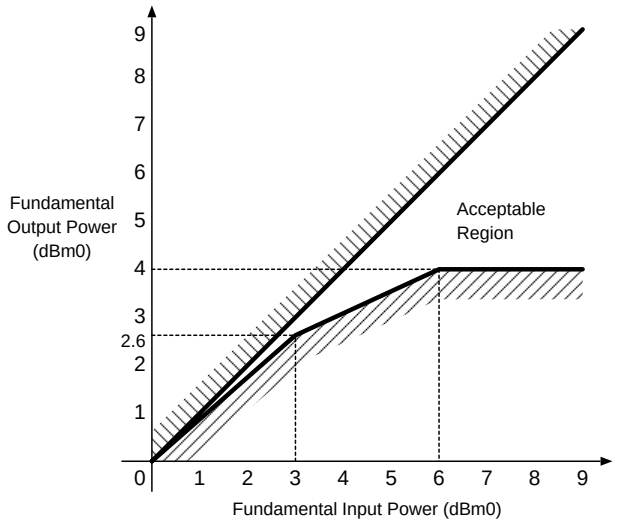


Figure 6. Overload Compression Performance

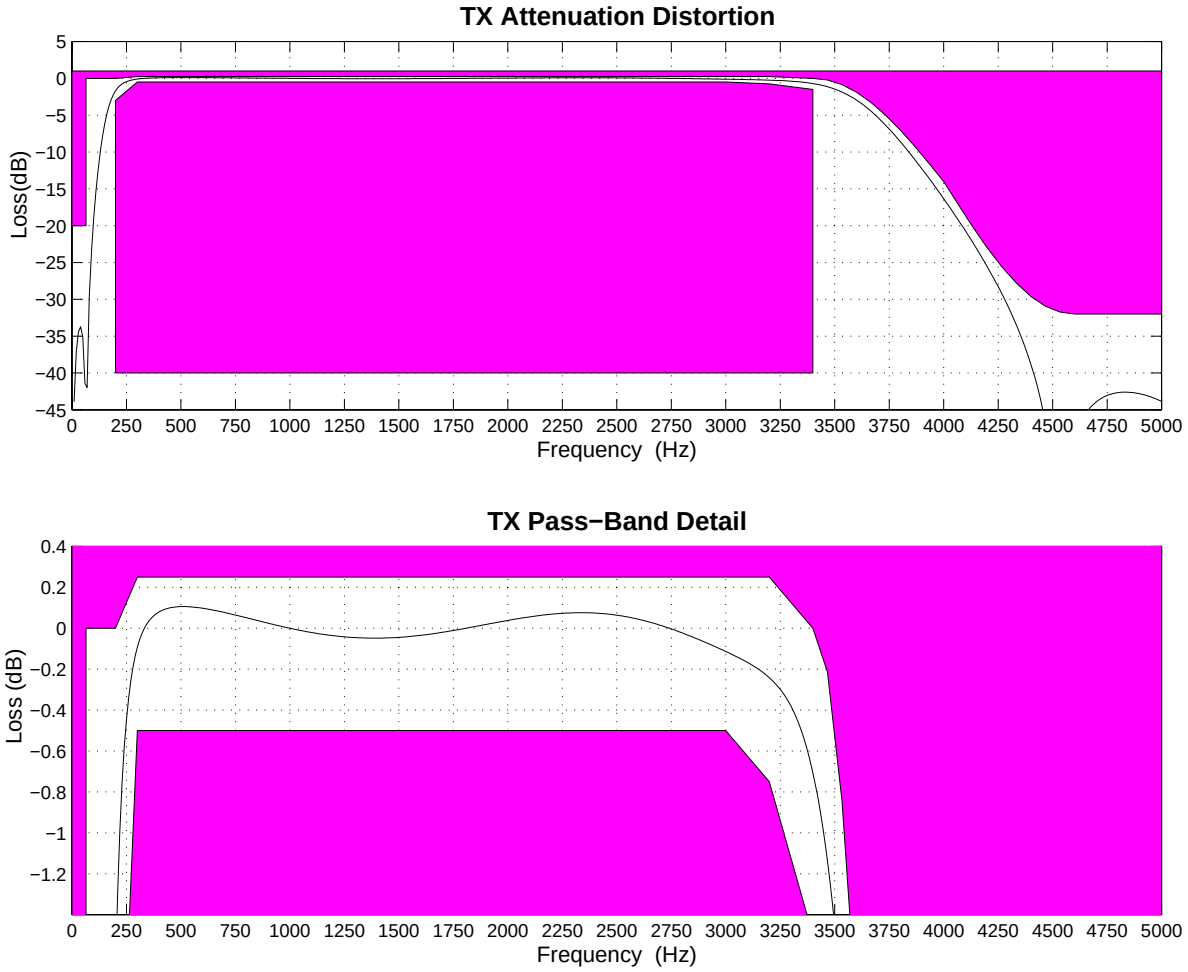


Figure 7. Transmit Path Frequency Response

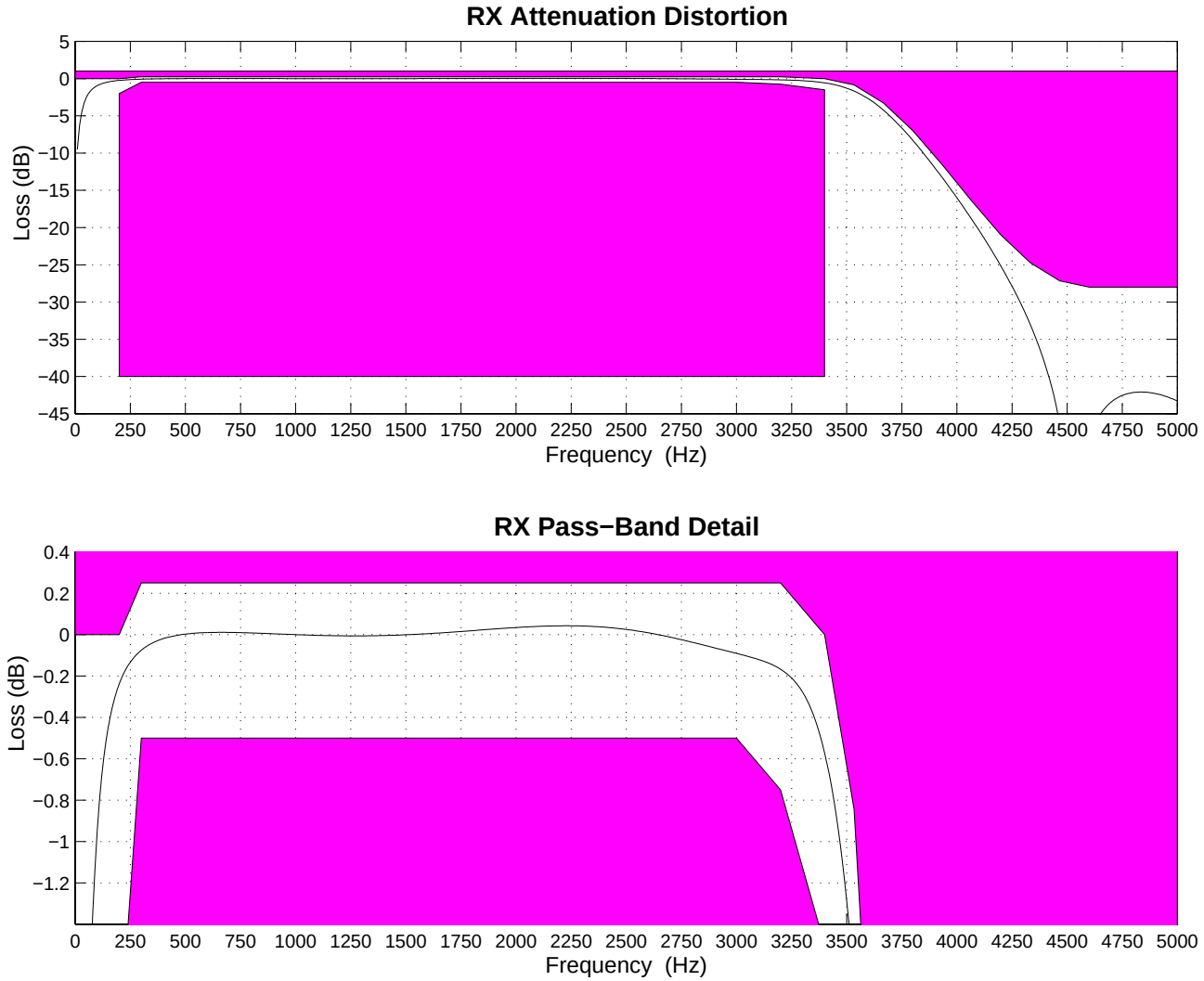


Figure 8. Receive Path Frequency Response

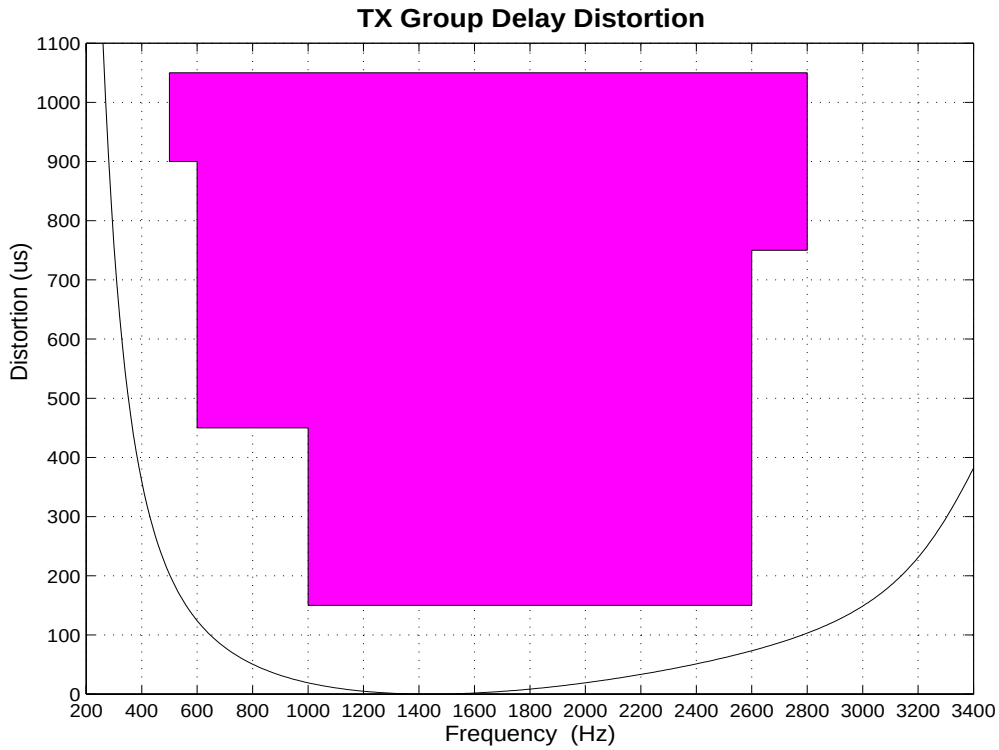


Figure 9. Transmit Group Delay Distortion

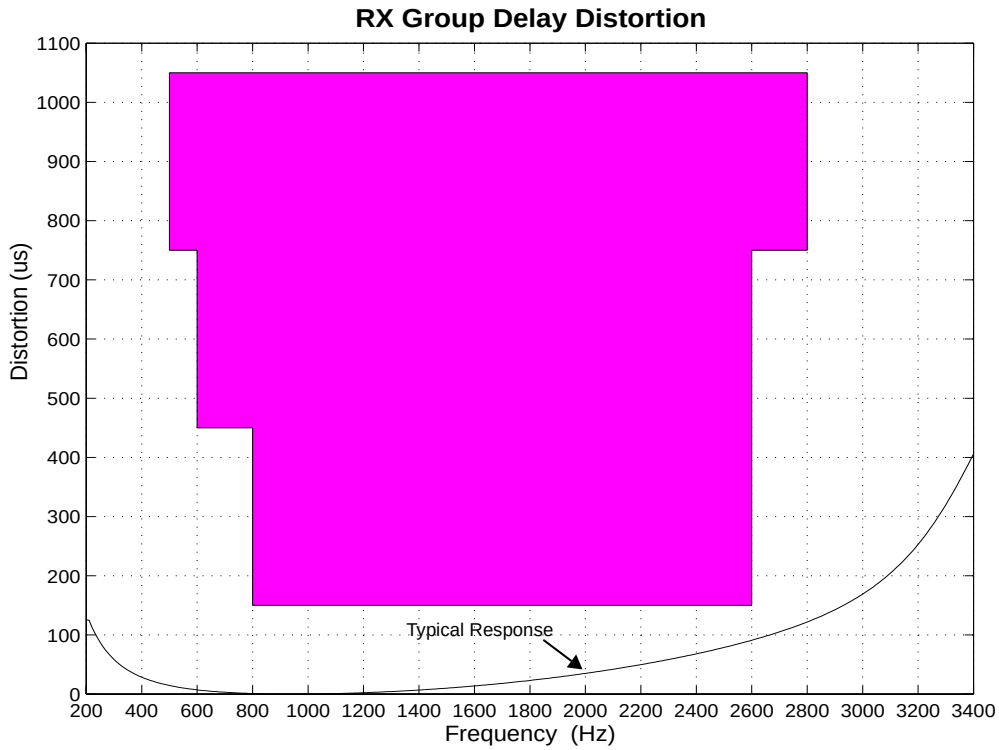


Figure 10. Receive Group Delay Distortion

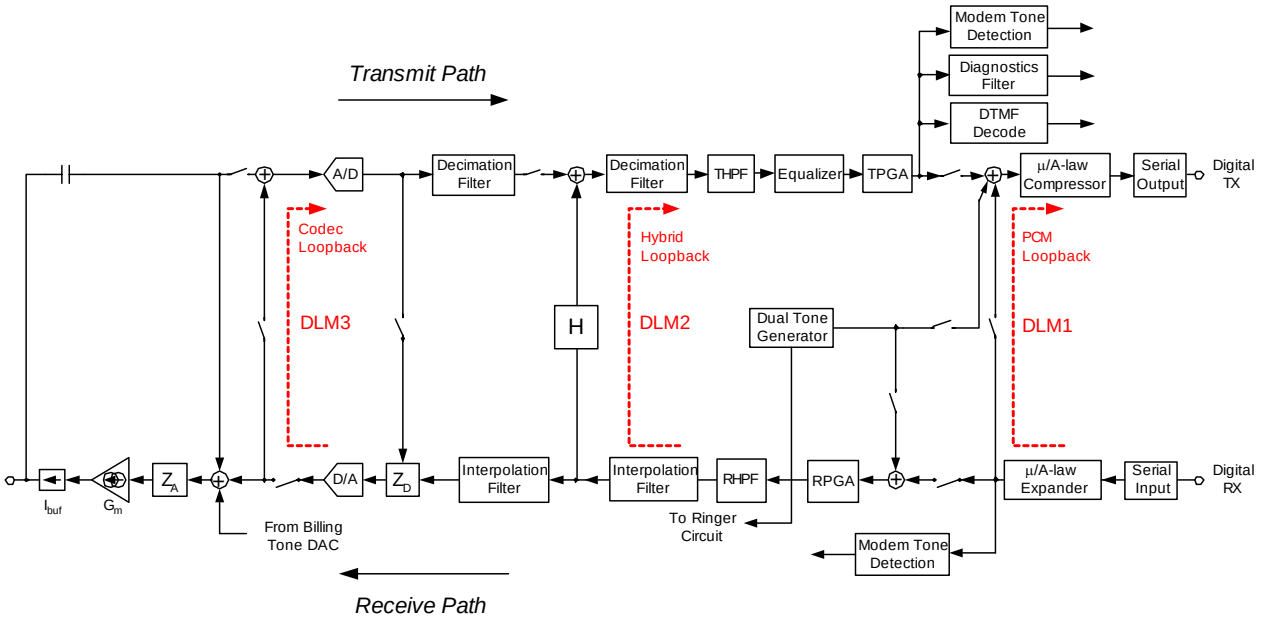


Figure 11. AC Signal Path Block Diagram for a Single Channel

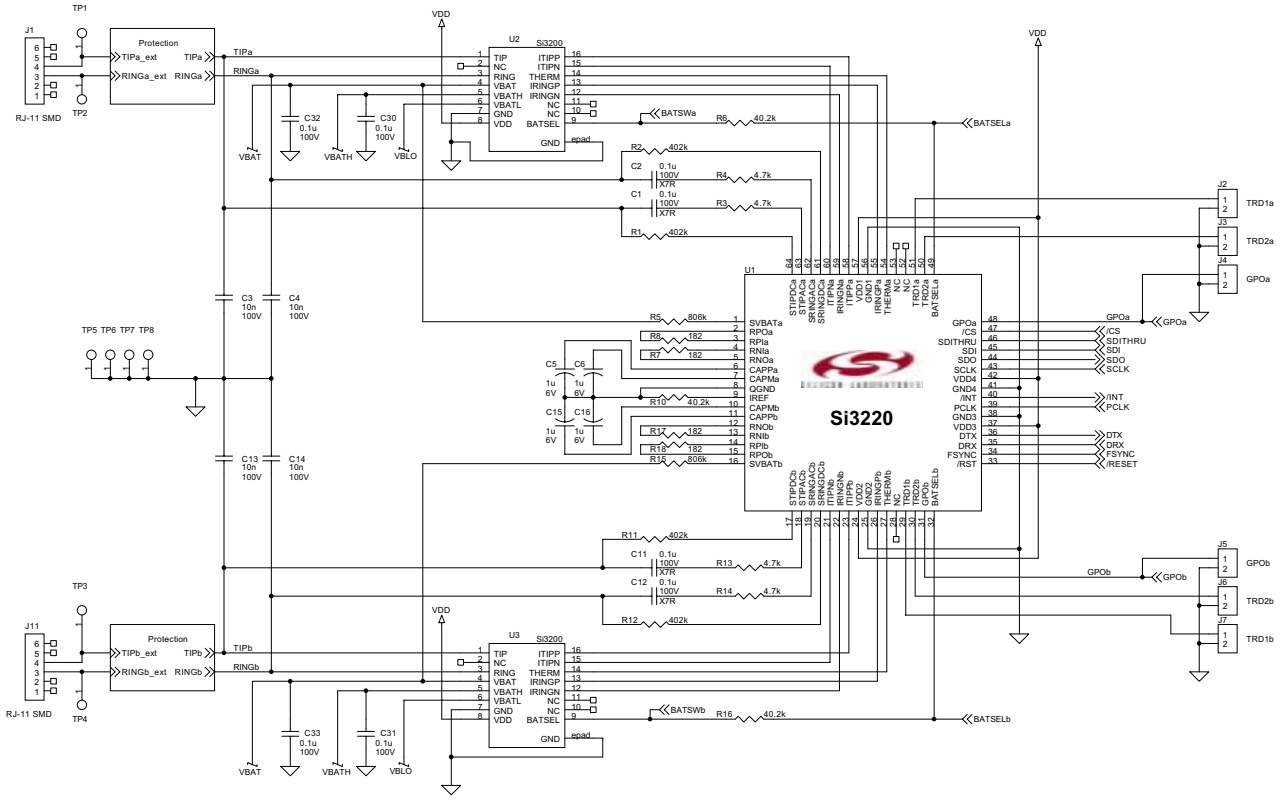


Figure 12. Si3220 Application Circuit Using Dual Battery Supply

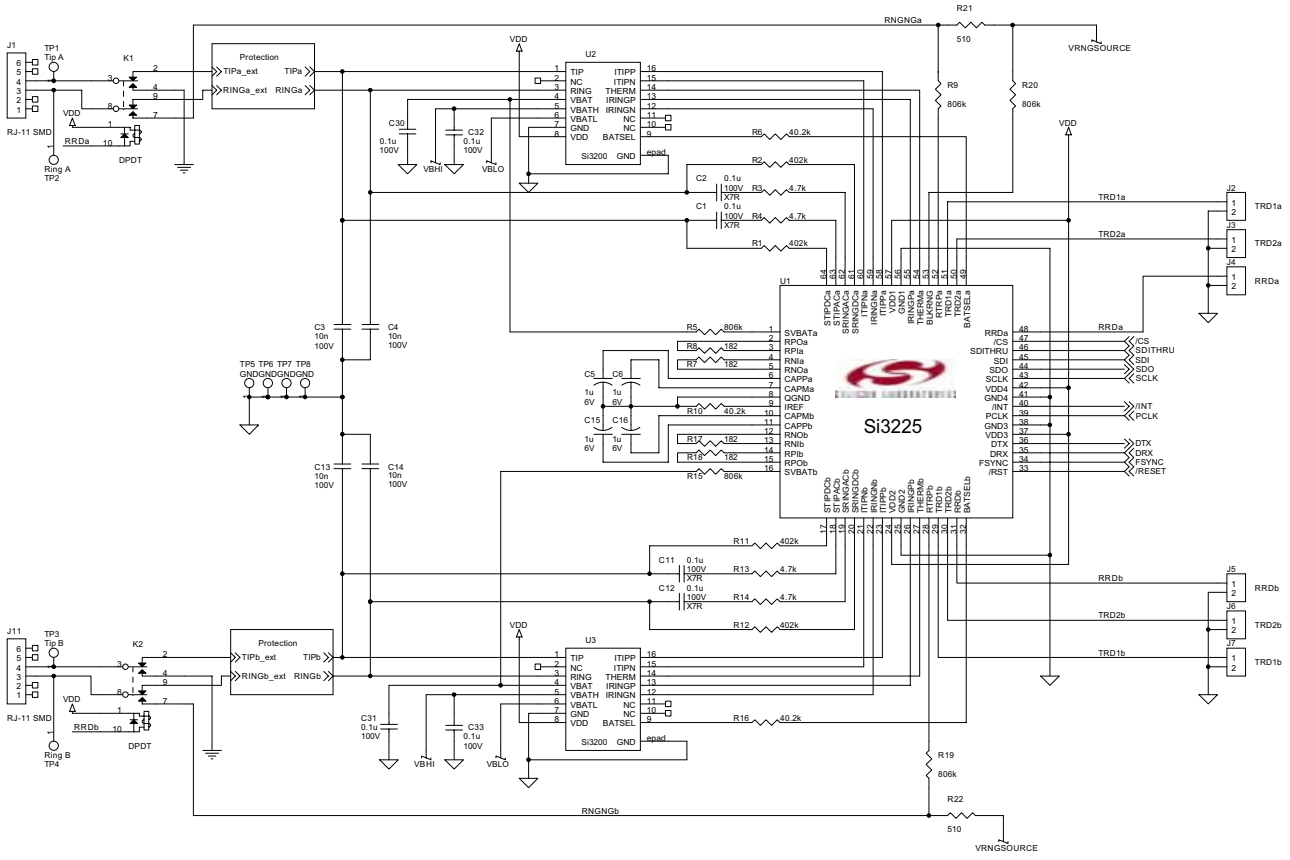


Figure 13. Si3225 Application Circuit Using Centralized Ringer and Secondary Battery Supply

Bill of Materials

Table 15. Si3220 + Si3200 External Component Values

Component	Value	Function
C1, C2, C11, C12	100 nF, 100 V, X7R, ±20%	Filter capacitors for TIP, RING ac sensing inputs.
C3, C4, C13, C14	10 nF, 100 V, X7R, ±20%	TIP/RING compensation capacitors.
C5, C6, C15, C16	1 μF, 6.3 V, X7R, ±20%	Low pass filter capacitors to stabilize differential and common mode SLIC feedback loops.
C30–C33	0.1 μF, 100 V, Y5V	Decoupling for battery voltage supply pins.
C20–C25	0.1 μF, 10 V, Y5V	Decoupling for analog and digital chip supply pins.
R1, R2, R11, R12	402 kΩ, 1/10 W, ±1%	Sense resistors for TIP, RING voltage sensing nodes.
R3, R4, R13, R14	4.7 kΩ, 1/10 W, ±1%	Current limiting resistors for TIP, RING ac sensing inputs.
R5, R15	806 kΩ, 1/10 W, ±1%	Sense resistor for battery dc sensing nodes.
R6, R16	40.2 kΩ, 1/10 W, ±5%	Sets bias current for battery switching circuit.
R7, R8, R17, R18	182 Ω, 1/10 W, ±1%	Reference resistors for internal transconductance amplifier.
R10	40.2 kΩ, 1/10 W, ±1%	Generates a high accuracy reference current.

Table 16. Si3225 + Si3200 External Component Values

Component	Value	Function
C1, C2, C11, C12	100 nF, 100 V, X7R, ±20%	Filter capacitors for TIP, RING ac sensing inputs.
C3, C4, C13, C14	10 nF, 100 V, X7R, ±20%	TIP/RING compensation capacitors.
C5, C6, C15, C16	1 μF, 6.3 V, X7R, ±20%	Low pass filter capacitors to stabilize differential and common mode SLIC feedback loops.
C30[1], C31[1], C32, C33	0.1 μF, 100 V, Y5V	Decoupling for battery voltage supply pins.
C20–C25	0.1 μF, 10 V, Y5V	Decoupling for analog and digital chip supply pins.
R1, R2, R11, R12	402 kΩ, 1/10 W, ±1%	Sense resistors for TIP, RING dc sensing nodes.
R5, R15	806 kΩ, 1/10 W, ±1%	Sense resistors for battery voltage sensing nodes.
R3, R4, R13, R14	4.7 kΩ, 1/10 W, ±1%	Current limiting resistors for TIP, RING ac sensing inputs.
R6[1], R16[1]	40.2 kΩ, 1/10 W, ±5%	Sets bias current for battery switching circuit.
R7, R8, R17, R18	182 Ω, 1/10 W, ±1%	Reference resistors for internal transconductance amplifier.
R9, R19, R20	806 kΩ, 1/10 W, ±1%	Sense registers for ringing generator feed.
R10	40.2 kΩ, 1/10 W, ±1%	Generates a high accuracy reference current.
R_{RING}	510 Ω, 2W, ±2%[2]	Feed resistor for ringing generator source.

Notes:
1. Optional. Only required when using dual battery architecture.
2. Example power rating.

Functional Description

The Dual ProSLIC chipset is a three-chip integrated solution that provides all SLIC, codec, and DTMF detection/decoding functions needed for a complete dual-channel analog telephone interface. Intended for multiple channel long loop (up to 18 kft) applications requiring high-density line card designs, the Dual ProSLIC chipset provides high integration and low-power operation for applications such as Central Office (CO) and digital loop carrier (DLC) enclosures. The Dual ProSLIC chipset is also ideal for short-loop applications requiring a space-effective solution such as terminal adapters, integrated access devices (IADs), PBX/key systems, and voice over IP systems. The chipset meets all relevant Bellcore LSSGR, ITU and ETSI standards.

The Si3220/Si3225 ICs perform all battery, overvoltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions on-chip in a low-power, small footprint solution. DTMF decoding and generation, phase continuous FSK (caller ID) signaling, and pulse metering are also integrated. All high-voltage functions are implemented using the Si3200 Linefeed Interface IC allowing a highly programmable integrated solution that offers the lowest total system cost.

The internal linefeed circuitry provides programmable on-hook voltage and off-current loop current, reverse battery operation, loop or ground start operation, and on-hook transmission. Loop current and voltage are continuously monitored using an integrated 8-bit monitor A/D converter. The Si3220 provides on-chip balanced 5 REN ringing with or without a programmable dc offset, eliminating the need for an external bulk ring generator and per-channel ringing relay. Both sinusoidal and trapezoidal ringing waveshapes are available. Ringing parameters such as frequency, waveshape, cadence, and offset are available in registers to reduce external controller requirements. The Si3225 supports external ringing generation with ring relay driver and external ring trip sensing to address legacy systems that implement a centralized ringing architecture. All ringing options are software programmable over a wide range of parameters to address a wide variety of application requirements.

The Si3220/Si3225 ICs also provide a variety of line monitoring and subscriber loop testing functions. All versions have the ability to generate specific dc and audio signals and continuously monitor and store all line voltage and current parameters. This combination of signal generation and measurement tools allows remote line card and loop diagnostics without requiring additional test equipment. These diagnostic functions are intended to comply with relevant LSSGR and ITU requirements for line-fault detection and reporting, and measured values are stored in registers for later use or further calculations. The Si3220 and Si3225 also include two per-channel relay drivers to support legacy systems implementing centralized test equipment.

A complete audio transmit and receive path is integrated, including DTMF generation and decoding, tone generation, modem/fax tone detection, programmable ac impedance synthesis, and programmable transhybrid balance and programmable gain attenuation. These features are software programmable, providing a single hardware design to meet international requirements. Digital voice data transfer occurs over a standard PCM bus and control data is transferred using a standard 4-wire serial peripheral interface (SPI). The Si3220 and Si3225 can also be configured to support a 4-wire general circuit interface (GCI). The Si3220 and Si3225 are available in a 64-lead TQFP and the Si3200 is available in a 16-lead SOIC.

Dual ProSLIC Architecture

The Dual ProSLIC chipset is comprised of a low-voltage CMOS device that uses a low-cost integrated linefeed interface IC to control the high voltages needed for operating the terminal equipment connected to the telephone line. Figure 15 on page 28 presents a simplified diagram of the linefeed control loop circuit for controlling the TIP and RING leads. The diagram shows a single-ended model for simplicity, showing either the TIP or the RING lead.

The Dual ProSLIC chipset produces line voltages and currents on the TIP/RING pair using register programmable settings in the Si3220 and Si3225 as well as direct ac and dc voltage/current sensing from the line. The Si3200 LFIC provides a low-cost interface for bridging the low-voltage CMOS devices to the high voltage TIP/RING pair. Sense resistors allow the voltage and current to be measured on each lead or across T-R using the low voltage circuitry inside the Si3220 and Si3225, eliminating expensive analog sensing circuitry inside the high-voltage Si3200. In addition, the total power inside the Si3200 is constantly monitored and controlled to provide optimal reliability under all operating conditions. The sensing circuitry is calibrated for environmental and process variations to guarantee accuracy with standard external resistor tolerances.

DC Feed Characteristics

The Si3220 and Si3225 offer programmable constant voltage and constant current operating regions as illustrated in Figure 14 and Figure 16. The constant voltage region (defined by the open-circuit voltage, V_{OC}) is programmable from 0 to 63.3 V in 1 V steps. The constant current region (defined by the loop current limit, I_{LIM}) is programmable from 18 to 45 mA in 0.87 mA steps. The Si3220 and Si3225 exhibit a characteristic dc impedance of 320 Ω during Active mode.

The TIP-RING voltage (V_{OC}) is offset from ground by a programmable voltage (V_{CM}) to provide sufficient voltage headroom to the most positive terminal (typically the TIP lead in normal polarity or the RING lead in reverse polarity) for carrying audio signals. A similar programmable voltage (V_{OV}) is an offset between the most negative terminal and the battery supply rail for carrying audio signals. (See Figure 14.) The user-supplied battery voltage must have sufficient amplitude under all operating states to ensure sufficient headroom. The Si3200 may be powered by a lower secondary battery supply (V_{BATL}) to reduce total power dissipation when driving short-loop lengths.

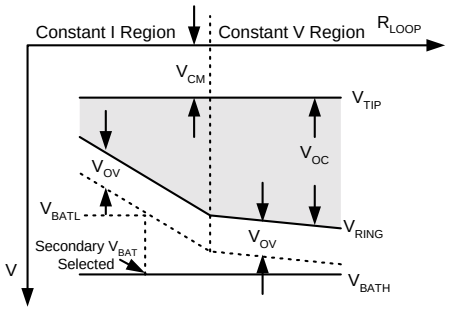


Figure 14. DC Linefeed Overhead Voltages (Forward State)

Calculating Overhead Voltages

The two programmable overhead voltages (V_{OV} and V_{CM}) represent one portion of the total voltage between V_{BAT} and ground as illustrated in Figure 14. In normal operating conditions, these overhead voltages are sufficiently low enough to maintain the desired TIP-RING voltage (V_{OC}). However, there are certain conditions under which the user must exercise care in providing a battery supply with enough amplitude to supply the required TIP-RING voltage and enough margin to accommodate these overhead voltages. The V_{CM} voltage is programmed for a given operating condition. Therefore, the open-circuit voltage (V_{OC}) varies according to the required overhead voltage (V_{OV}) and the supplied battery voltage (V_{BAT}). The user should pay attention to the maximum V_{OV} and V_{CM} that might be required for each operating state.

In the off-hook active state, sufficient V_{OC} must be maintained to correctly power the phone from the battery supply that is provided. Because the battery supply depends on the state of the input supply (i.e., Charging, Discharging, or Battery Backup mode), the user must decide how much loop current is required and then determine the maximum loop impedance that can be driven based on the battery supply provided. The minimum battery supply required can be calculated with the following equation:

$$V_{BAT} \geq V_{OC} + V_{CM} + V_{OV}$$

where V_{CM} and V_{OV} are provided in Table 8. The default V_{CM} value of 3 V provides sufficient overhead for a 3.1 dBm signal into a 600 Ω loop impedance with an I_{LIM} setting of 22 mA and an ABIAS setting of 4 mA. A V_{OV} value of 4 V provides sufficient headroom to source a maximum I_{LOOP} of 45 mA with a 3.1 dBm audio signal and an ABIAS setting of 16 mA. For a typical operating condition of V_{BAT} = –56 V and I_{LIM} = 22 mA:

$$V_{OC,MAX} = 56\ V - (3\ V + 4\ V) = 49\ V$$

These conditions apply when the dc sensing inputs (STIPDCa/b and SRINGDCa/b) are placed on the SLIC side of any protection resistance placed in series with the TIP and RING leads. If line-side sensing is desired, both V_{OV} and V_{CM} must be increased by a voltage equal to R_{PROT} x I_{LIM} where R_{PROT} is the value of each protection resistor. Other safety precautions may also apply.

See the "Linefeed Overhead Voltage Considerations During Ringing" on page 43 for details on calculating the overhead voltage during the ringing state.

The Dual ProSLIC chipset uses both voltage and current information to control TIP and RING. Sense resistor R_{DC} measures dc line voltages on TIP and RING; Capacitor C_{AC} couples the ac line voltages on the TIP and RING leads to be measured. The Si3220 and Si3225 both use the Si3200 to drive TIP and RING and isolate the high-voltage line from the low-voltage CMOS devices.

The Si3220 and Si3225 measure voltage at various nodes to monitor the linefeed current. R_{DC} and R_{BAT} provide these measuring points. The sense circuitry is calibrated on-chip to guarantee measurement accuracy. See "Linefeed Calibration" on page 31 for details.

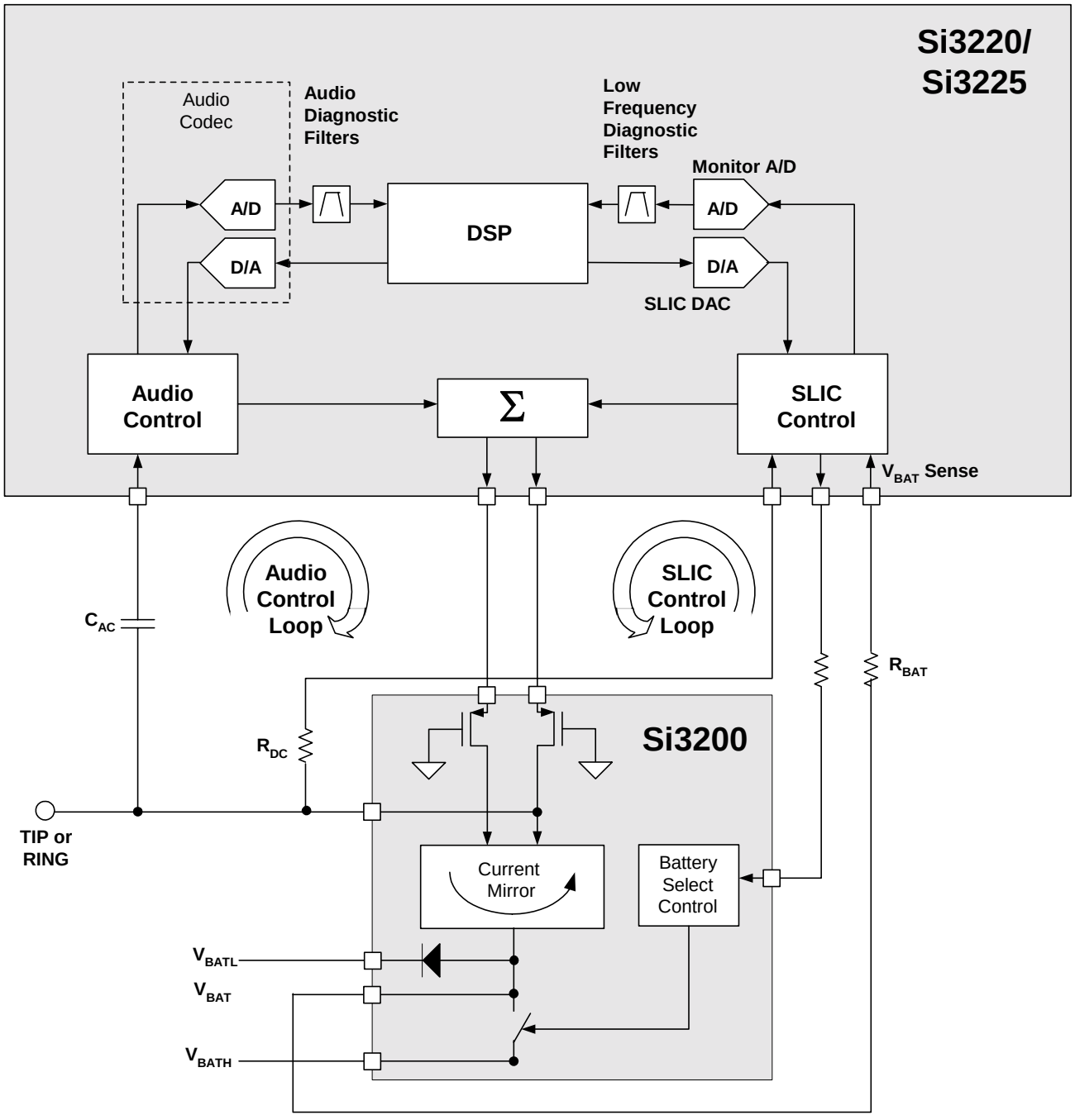


Figure 15. Simplified Dual ProSLIC Linefeed Architecture for TIP and RING Leads (diagram illustrates either TIP or RING lead of a single channel)

Linefeed Operation States

The linefeed interface includes eight different operating states. (See Table 17.) The linefeed register settings (LF[2:0], Linefeed register) are also listed. The Open state is the default condition in the absence of any pre-loaded register settings. The device may also automatically enter the Open state if excess power consumption is detected in the Si3200. See "Power Monitoring and Power Fault Detection" on page 33 for more details. The register and RAM locations used for programming the linefeed parameters are provided in Table 18. See “Loop Voltage and Current Monitoring,” “Power Monitoring and Power Fault Detection,” and “Power Dissipation Considerations” for detailed descriptions and register/RAM locations for these functions.

Table 17. Linefeed States

Open (LF[2:0] = 000). The Si3200 output is high-impedance. This mode can be used in the presence of line fault conditions and to generate open switch intervals (OSIs). The device also can automatically enter the Open state if excess power consumption is detected in the Si3200.
Forward Active (LF[2:0] = 001). Linefeed is active, but audio paths are powered down until an off-hook condition is detected. The Si3220 and Si3225 automatically enter a low power state to reduce power consumption during on-hook standby periods.
Forward On-Hook Transmission (LF[2:0] = 010). Provides data transmission during an on-hook loop condition (e.g., transmitting FSK caller ID information between ringing bursts).
Tip Open (LF[2:0] = 011). Sets the portion of the linefeed interface connected to the TIP side of the subscriber loop to high-impedance and provides an active linefeed on the RING side of the loop for ground start operation.
Ringing (LF[2:0] = 100). Drives programmable ringing waveforms onto the subscriber loop (Si3220) or switches in a centralized ringing generator by driving an external relay (Si3225).
Reverse Active (LF[2:0] = 101). Linefeed circuitry is active, but audio paths are powered down until an off-hook condition is detected. The Si3220 and Si3225 automatically enter a low power state to reduce power consumption during on-hook standby periods.
Reverse On-Hook Transmission (LF[2:0] = 110). Provide data transmission during an on-hook loop condition.
Ring Open (LF[2:0] = 111). Sets the portion of the linefeed interface connected to the RING side of the subscriber loop to high-impedance and provides an active linefeed on the TIP side of the loop for ground start operation.

Table 18. Register and RAM Locations for Linefeed Control

Parameter	Register/RAM Mnemonic	Register/RAM Bits	Programmable Range	LSB Size	Effective Resolution
Linefeed	LINEFEED	LF[2:0]	See Table 17	N/A	N/A
Linefeed Shadow	LINEFEED	LFS[2:0]	Monitor Only	N/A	N/A
Battery Feed Control	RELAYCON	BATSEL	VBATH/VBATL	N/A	N/A
Loop Current Limit	ILIM	ILIM[4:0]	18–45 mA	0.875 mA	0.875 mA
On-Hook Line Voltage	VOC	VOC[14:0]	0 to 63.3 V	4.907 mV	1.005 V
Common Mode Voltage	VCM	VCM[14:0]	0 to 63.3 V	4.907 mV	1.005 V
V_{OC} Delta for Off-Hook	VOCDELTA	VOCDELTA[14:0]	0 to 63.3 V	4.907 mV	1.005 V
V_{OC} Delta Threshold, Low	VOCLTH	VOCLTH[15:0]	0 to 63.3 V	4.907 mV	1.005 V
V_{OC} Delta Threshold, High	VOCHTH	VOCHTH[15:0]	0 to 63.3 V	4.907 mV	1.005 V
Overhead Voltage	VOV	VOV[14:0]	0 to 63.3 V	4.907 mV	1.005 V
Ringing Overhead Voltage	VOVRING	VOVRING[14:0]	0 to 63.3 V	4.907 mV	1.005 V
V_{OC} During Battery Tracking	VOCTRACK	VOCTRACK[15:0]	0 to 63.3 V	4.907 mV	1.005 V

The dc linefeed circuitry generates the necessary TIP/RING I/V characteristics along with loop closure and ring trip detection. For loop start applications, V_{TIP}-V_{RING} is programmable. The loop current limit (I_{LIM}) is software programmable with a range from 18–45 mA.

Figure 16 illustrates the linefeed characteristics for a typical application using an I_{LOOP} setting of 24 mA and a TIP-RING open circuit voltage (V_{OC}) of 48 V. The VOC and VOCTRACK RAM locations are used to program the TIP-RING voltage, and these two values are equal when $V_{BAT} > V_{OC} + V_{OV} + V_{CM}$. When the battery voltage drops below that point, VOCTRACK decreases at the same rate as V_{BAT} decreases to provide sufficient headroom to accommodate both V_{OV} and V_{CM} levels below VBAT.

The equation for calculating the RAM address value for VOC, VCM, VOCDELTA, VOV, VOVRING, RINGOF, VOCLTH, and VOCHTH is shown below. The CEILING function rounds up the result to the next integer.

$$\text{RAM VALUE} = 2 \times \text{CEILING}\left(\text{ROUND}\left(\frac{\text{desired voltage}}{1.005\text{V}}\right) \times \frac{512}{5}\right)$$

For example, to program a VOC value of 51 V:

$$\text{VOC} = 2 \times \text{CEILING}\left(\text{ROUND}\left(\frac{51V}{1.005\text{V}}\right) \times \frac{512}{5}\right) = 28\text{CEh}$$

During the on-hook state, the Si3220/Si3225 is in the constant voltage operating area and typically presents a 640 Ω output impedance (Figure 16). The Si3220 and Si3225 include a special modified linefeed scheme called Modfeed™, which adjusts the ProSLIC's output impedance based on the linefeed voltage level in order to ensure the ability to source extended loop lengths. When the terminal equipment transitions to the off-hook state, the linefeed voltage typically collapses and transitions through the preset Modfeed threshold voltage causing the Si3220/Si3225 to reduce its output impedance to 320 Ω. The TIP-RING voltage will then continue decreasing until the preset loop current limit (I_{LIM}) setting is reached. Loop closure and ring trip detection thresholds are programmable and include internal debouncing. A high-gain common mode loop generates a low-impedance from TIP or RING to ground, effectively reducing the effects of longitudinal interference.

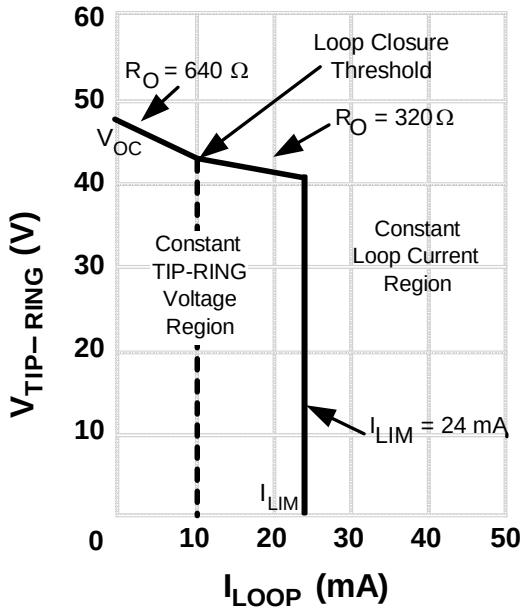


Figure 16. $V_{TIP-RING}$ vs. I_{LOOP} Characteristic for Loop Start Operation

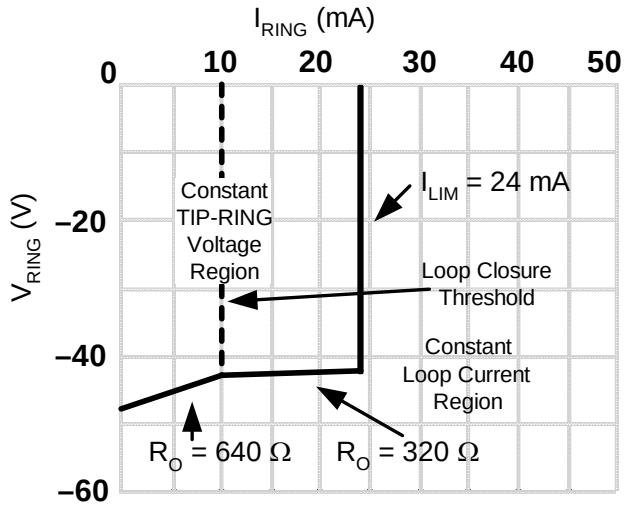


Figure 17. V_{RING} vs. I_{RING} Characteristic for Ground Start Operation

For ground start operation, the active lead presents a 640 Ω output impedance during the on-hook state and a 320 Ω output impedance in the off-hook state. The "open" lead presents a high-impedance feed (>150 kΩ). Figure 17 illustrates a typical ground start application using V_{OC} = 48 V and I_{LIM} = 24 mA in the TIP OPEN state. The ring ground detection threshold and debouncing interval are both programmable.

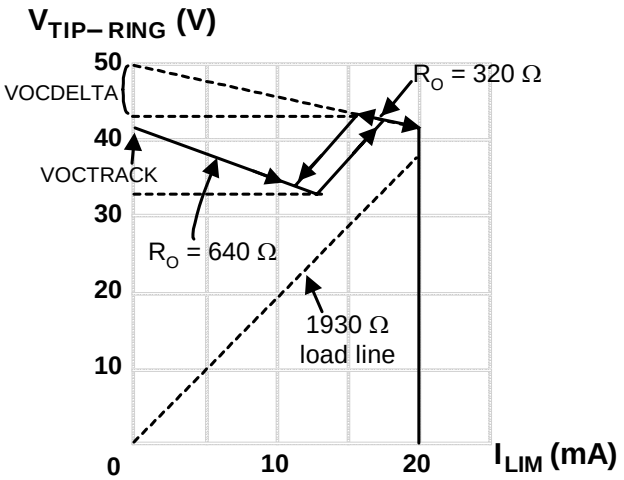


Figure 18. $V_{TIP-RING}$ vs. I_{LOOP} Characteristics using Modfeed™

The Modfeed scheme also allows the user to modify the apparent VOC voltage as a means of boosting the linefeed voltage when the battery voltage drops below a certain level. Figure 18 illustrates a typical Si3225 application using Modfeed while sourcing a 1930 Ω subscriber loop (1500 Ω loop impedance with a 430 Ω phone connected) from a 48 V battery. For V_{OV} and V_{CM} values of 3 V, the VOCTRACK RAM location is set to 42 V given a programmed value of 42 V for the VOC RAM location. When a loop closure event occurs, the TIP-RING voltage decreases linearly until it reaches a preset voltage threshold that is lower than VOCTRACK by an amount programmed into the VOCLTH RAM location. Exceeding this threshold causes the Si3220/Si3225 to increase its "target" V_{OC} level by an amount programmed into the VOCDELTA RAM location to provide additional overhead for driving the higher impedance loop. In the on-hook condition, the TIP-RING voltage increases linearly until it rises above a second preprogrammed voltage threshold, which is higher than VOCTRACK by an amount programmed into the VOCHTH RAM location. This offers the ability to drive very long loop lengths while using the lowest possible battery voltage. Consult the factory for optimal register and RAM location settings for specific applications.

Linefeed Calibration

An internal calibration algorithm corrects for internal and external component errors. The calibration is initiated by setting the CAL register bit. This bit automatically resets on completion of the calibration cycle.

A calibration should be executed following system powerup. Upon release of the chip reset, the chipset will be in the Open state and calibration may be initiated.

Only one calibration should be necessary if the system remains powered up.

To optimize performance, it is recommended that the user perform the following steps when running the CAL routines:

1. Set CALR1 = 0x3F and CALR2 = 0x3E. This enables all calibration routines except the AC longitudinal balance (CALCMBAL) routine.
2. Set the CAL bit in the CALR1 register. This runs the first set of calibration routines.
3. Set the ProSLIC to the ACTIVE state (set LINEFEED = 0x01)
4. Set CALR2 = 0x01. This enables only the AC longitudinal balance calibration routine.
5. Set the CAL bit in the CALR1 register.

There is an initial settling period of approximately 300 ms that is required prior to running the first set of calibration routines. Each calibration routine requires approximately 1 ms to complete, except for the ac longitudinal balance routine, which requires up to 100 ms. An additional 300 ms settling period is also required after going to the ACTIVE state and prior to running the ac longitudinal balance routine.

During calibration, V_{TIP} and V_{RING} are controlled by the calibration engine to provide the correct external voltage conditions for the algorithm. Calibration should always be performed in the on-hook active state. The TIP and RING leads must not be connected to ground during calibration.

Loop Voltage and Current Monitoring

The Dual ProSLIC chipset continuously monitors the TIP and RING voltages and currents. These values are available in registers. An internal 8-bit A/D converter samples the measured voltages and currents from the analog sense circuitry and translates them into the digital domain. The A/D updates the samples at an 800 Hz rate for all inputs except VRNGNG and IRNGNG, which are sampled at 8 kHz to provide higher resolution for zero crossing detection in external ringing applications. Two derived values, the loop voltage ($V_{TIP} - V_{RING}$) and the loop current also are reported. For ground start operation, the values reported are V_{RING} and the current flowing in the RING lead. Table 19 lists the register set associated with the loop monitoring functions.

The Dual ProSLIC chipsets also include the ability to perform loop diagnostics functions as outlined in "Line Test and Diagnostics" on page 85.

Table 19. Register and RAM Locations Used for Loop Monitoring

Parameter	Register/RAM Mnemonic	Register/ RAM Bits	Measurement Range	LSB Size	Effective Resolution
Loop Voltage Sense ($V_{TIP} - V_{RING}$)	VLOOP	VLOOP[15:0]	0 to 64.07 V 64.07 to 160.173 V	4.907 mV	251 mV 628 mV
TIP Voltage Sense	VTIP	VTIP[15:0]	0 to 64.07 V 64.07 to 160.173 V	4.907 mV	251 mV 628 mV
RING Voltage Sense	VRING	VRING[15:0]	0 to 64.07 V 64.07 to 160.173 V	4.907 mV	251 mV 628 mV
Loop Current Sense	ILOOP	ILOOP[15:0]	0 to 101.09 mA	3.097 µA	500 µA*
Battery Voltage Sense	VBAT	VBAT[15:0]	0 to 63.3 V 0 to 160.173 V	4.907 mV	251 mV 628 mV
Longitudinal Current Sense	ILONG	ILONG[15:0]	0 to 101.09 mA	3.097 µA	500 µA*
External Ringing Generator Voltage Sense	VRNGNG	VRNGNG[15:0]	332.04 V	10.172 mV	1.302 V
External Ringing Generator Current Sense	IRNGNG	IRNGNG[15:0]	662.83 mA	20.3 µA	2.6 mA

***Note:** I_{LOOP} and I_{LONG} are calculated values based on measured I_{Q1}–I_{Q4} currents. The resulting effective resolution is approximately 500 µA.

Power Monitoring and Power Fault Detection

The Dual ProSLIC line monitoring functions can be used to protect the high-voltage circuitry against excessive power dissipation and thermal overload conditions. This protection scheme can be implemented in a number of different ways depending on the application circuit used. When the Si3200 linefeed interface chip is used, an on-chip thermal monitor diode provides realtime Si3200 die temperature data to the Si3220/3225. The Dual ProSLIC devices also have the ability to prevent thermal overloads by regulating the total power inside the Si3200 or in each of the external bipolar transistors (if using a discrete linefeed circuit). The DSP engine performs all power calculations and provides the ability to automatically transition the device into the OPEN state and generate a power alarm interrupt when excessive power is detected. Table 20 on page 35 describes the register and RAM locations used for power monitoring.

Thermometer-Based Si3200 Power Monitor

The Si3200 includes an on-chip analog thermal sensing diode that provides realtime die temperature data to the Si3220/3225 provided the THERMSEL bit is set to 1. The analog thermometer has a built in temperature threshold which, when exceeded, turns off the Si3200 and asserts the STAT bit of the THERM register. The internal temperature threshold is set to approximately 140 °C to maintain optimal device reliability.

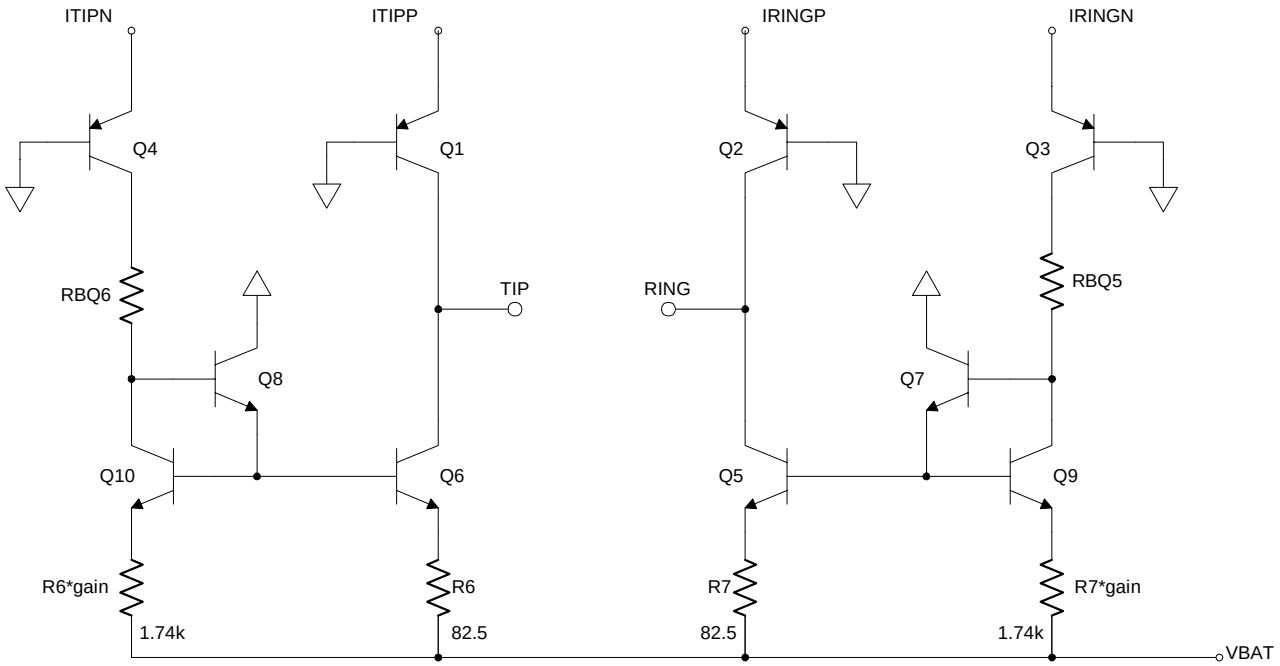


Figure 19. Discrete Linefeed Circuit for Power Monitoring

Transistor Power Equations (Using Discrete Transistors)

When using the Si3220 or Si3225 along with discrete bipolar transistors, it is possible to control the total power of the solution by regulating the power in each discrete transistor individually. Figure 19 illustrates the basic transistor-based linefeed circuit for one channel. The power dissipation of each external transistor is estimated based on the A/D sample values. The approximate power equations for each external BJT are as follows:

$P_{Q1} \cong V_{CE1} \times I_{Q1} \cong (V_{TIP} + 0.75\ V) \times (I_{Q1})$

$P_{Q2} \cong V_{CE2} \times I_{Q2} \cong (V_{RING} + 0.75\ V) \times (I_{Q2})$

$P_{Q3} \cong V_{CE3} \times I_{Q3} \cong (V_{BAT} - R106 \times I_{Q5}) \times (I_{Q3})$

$P_{Q4} \cong V_{CE4} \times I_{Q4} \cong (V_{BAT} - R103 \times I_{Q6}) \times (I_{Q4})$

$P_{Q5} \cong V_{CE5} \times I_{Q5} \cong (V_{BAT} - V_{RING} - R106 \times I_{Q5}) \times (I_{Q5})$

$P_{Q6} \cong V_{CE6} \times I_{Q6} \cong (V_{BAT} - V_{TIP} - R103 \times I_{Q6}) \times (I_{Q6})$

The maximum power threshold for each device is software programmable and should be set based on the characteristics of the transistor package, PCB design, and available airflow. If the peak power exceeds the programmed threshold for any device, the power alarm bit is set for that device. Each external bipolar has its own register bit (PQ1S–PQ6S bits of the IRQVEC3 register) which goes high on a rising edge of the

comparator output and remains high until the user clears it. Each transistor power alarm bit is also maskable by setting the PQ1E–PQ6E bits in the IRQEN3 register.

Si3200 Power Calculation

When using the Si3200, it is also possible to control thermal temperature rise by calculating the total power dissipated within the IC. This case is similar to the Transistor Power Equations case, with the exception that the total power from all transistor devices is dissipated within the same package enclosure and the total power result is placed in the PSUM RAM location. The power calculation is derived using the following set of equations:

$P_{Q1} \cong (V_{TIP} + 0.75\ V) \times I_{Q1}$
$P_{Q2} \cong (V_{RING} + 0.75\ V) \times I_{Q2}$
$P_{Q3} \cong (V_{BAT} + 0.75\ V) \times I_{Q3}$
$P_{Q4} \cong (V_{BAT} + 0.75\ V) \times I_{Q4}$
$P_{Q5} \cong (V_{BAT} - V_{RING}) \times I_{Q5}$
$P_{Q6} \cong (V_{BAT} - V_{TIP}) \times I_{Q6}$

PSUM = total dissipated power = $P_{Q1} + P_{Q2} + P_{Q3} + P_{Q4} + P_{Q5} + P_{Q6}$

Power Filter and Alarms

The power calculated during each A/D sample period must be filtered before being compared to a user programmable maximum power threshold. A simple digital low pass filter is used to approximate the transient thermal behavior of the package, with the output of the filter representing the effective peak power within the package or, equivalently, the peak junction temperature.

For Q1, Q2, Q3, Q4 in SOT23 and Q5, Q6 in SOT223 packages, the settings for thermal low pass filter poles and power threshold settings are (for an ambient temperature of 70 °C) calculated as follows. If the thermal time constant of the package is $\tau_{thermal}$, the decimal values of RAM locations PLPF12, PLPF34, and PLPF56 are given by rounding to the next integer the value given by the equation:

$$\text{PLPFxx (decimal value)} = \frac{4096}{800 \times \tau_{thermal}}$$

Where 4096 is the maximum value of the 12-bit plus sign RAM locations PLPF12, PLPF34, and PLPF56, and 800 is the power calculation clock rate in Hz. The equation is an excellent approximation of the exact equation for $\tau_{thermal}$ = 1.25 ms … 5.12 s. With the above equations in mind, the values of the RAM locations PLPF12, PLPF34, and PLPF56 are presented below:

PTH12 = power threshold for Q1, Q2 = 0.21 W (0x0480)

PTH34 = power threshold for Q3, Q4 = 0.21 W (0x2600)

PTH56 = power threshold for Q5, Q6 = 1.28 W (0x1B80)

PLPF12 = thermal LPF pole for Q1, Q2 (0x0100 for M = 128)

PLPF34 = thermal LPF pole for Q3, Q4 (0x0100 for M = 128)

PLPF56 = thermal LPF pole for Q5, Q6 (0x0010 for M = 2048)

In the case where the Si3200 is used, the thermal filtering needs only to be performed only on the total power reflected in the PSUM RAM location. When the filter output exceeds the total power threshold, an interrupt is issued. The PTH12 RAM location is used to preset the total power threshold for the Si3200, and the PLPF12 RAM location is used to preset the thermal low pass filter pole.

Automatic State Change Based on Power Alarm

If any of the following situations occurs, the device will automatically transition to the OPEN state:

- The thermometer based power alarm in the Si3200 is asserted.
- Any of the transistor power alarm thresholds is exceeded, in the case of the discrete transistor circuit.
- The total power threshold is exceeded, when using the power calculator method along with the Si3200.

To provide optimal reliability, the device automatically transitions into the open state until the user changes the state manually, independent of whether or not the power alarm interrupt has been masked. The PQ1E–PQ6E bits of the IRQEN3 register enable the interrupts for each transistor power alarm and the PQ1S to PQ6S bits of the IRQVEC3 register are set when a power alarm is triggered in the respective transistor. When using the Si3200, the PQ1E bit enables the power alarm interrupt, and the PQ1S bit is set when a Si3200 power alarm is triggered.

Table 20. Register and RAM Locations Used for Power Monitoring and Power Fault Detection

Parameter	Register/RAM Mnemonic	Register/RAM Bits	Measurement Range	Resolution
Si3200 Total Power Output Monitor	PSUM	PSUM[15:0]	0 to 16.319 W	498 µW
Si3200 Power Alarm Interrupt Pending	IRQVEC3	PQ1S	N/A	N/A
Si3200 Power Alarm Interrupt Enable	IRQEN3	PQ1E	N/A	N/A
Q1/Q2 Power Alarm Threshold	PTH12	PTH12[15:0]	0 to 16.319 W	498 µW
Q3/Q4 Power Alarm Threshold	PTH34	PTH34[15:0]	0 to 1.03 W	31.4 µW
Q5/Q6 Power Alarm Threshold	PTH56	PTH56[15:0]	0 to 16.319 W	498 µW
Q1/Q2 Thermal LPF Pole	PLPF12	PLPF12[15:0]	See “Power Filter and Alarms”	
Q3/Q4 Thermal LPF Pole	PLPF34	PLPF34[15:0]	See “Power Filter and Alarms”	
Q5/Q6 Thermal LPF Pole	PLPF56	PLPF56[15:0]	See “Power Filter and Alarms”	
Q1–Q6 Power Alarm Interrupt Pending	IRQVEC3	PQ1S–PQ6S	N/A	N/A
Q1–Q6 Power Alarm Interrupt Enable	IRQEN3	PQ1E–PQ6E	N/A	N/A

Power Dissipation Considerations

The Dual ProSLIC chipset is designed with the ability to source long loop lengths in excess of 18 kft, but can also accommodate short loop configurations. For example, the Si3220 can operate from one of two battery supplies depending on the operating state. When in the on-hook state, the on-hook loop feed is generated from the ringing battery supply, generally –70 V or more. Once the SLIC transitions to the off-hook state, a lower off-hook battery supply (typically –24 V) supplies the required current to power the loop if the loop length is sufficiently short to accommodate the lower battery supply. This battery switching method allows the SLIC chipset to dissipate less power than is possible if operating from a –70 V battery supply. See "Automatic Dual Battery Switching" on page 38 for more details.

In long loop applications, there is generally a single battery supply (e.g., –48 V) available for powering the loop in the off-hook state. When sourcing loop lengths similar to the maximum specified service distance (e.g., 18 kft.), most of the power is dissipated in the impedance of the line. SLICs used in long-loop applications must also be able to provide phone service to customers who are located much closer to the line card than the maximum loop length specified for the system. This situation may cause substantial power to be dissipated inside the SLIC chipset, often resulting in thermal shutdown or destruction of the device due to thermal runaway.

The Dual ProSLIC devices rely on the Si3200 to power the line from the battery supply. The PCB layout and enclosure conditions should be designed to allow sufficient thermal dissipation out of the Si3200, and a programmable power alarm threshold ensures product safety under all operating conditions. See "Power Monitoring and Power Fault Detection" on page 33 for more details on power alarm considerations.

The Si3200’s thermally enhanced SOIC-16 package offers an exposed pad that improves thermal dissipation out of the package when soldered to a topside PCB pad connected to inner power planes. Using appropriate layout practices, the Si3200 can provide a thermal performance of 65 °C/W. The exposed path should be connected to a low-impedance ground plane via a topside PCB pad directly under the part. See package outlines for PCB pad dimensions. In addition, an opposite-side PCB pad with multiple vias connecting it to the topside pad directly under the exposed pad will further improve the overall thermal performance of the system. Contact the factory for layout guidelines for optimal thermal dissipation.

Loop Closure Detection

Loop closure detection is required to accurately signal a terminal device going off-hook during the Active or On-Hook Transmission linefeed states (forward or reverse polarity). The functional blocks required to implement a loop closure detector are shown in Figure 20, and the register set for detecting a loop closure event is

provided in Table 21. The primary input to the system is the loop current sense value from the voltage/current/power monitoring circuitry and reported in the ILOOP RAM address. The LCS value is processed in the input signal processor (ISP) provided the LFS bits in the Linefeed register indicate the device is in an Active or On-Hook Transmission state. The output of the ISP is the input to a programmable digital low pass filter, which removes unwanted ac signal components before threshold detection.

The low-pass filter coefficient is calculated using the equation below and is entered into the LCRLPF RAM location.

LCRLPF = [(2πf x 4096)/800]

Where f = the desired cutoff frequency of the filter.

The programmable range of the filter is from 0 (blocks all signals) to 4000 (unfiltered). A typical value of 10 Hz (0A10h) is sufficient to filter out any unwanted ac artifacts while allowing the dc information to pass through the filter.

The output of the low pass filter is compared to a programmable threshold, LCROFFHK. Hysteresis is enabled by programming a second threshold, LCRONHK, to detect the loop going to an open or on-hook state. The threshold comparator output feeds a programmable debounce filter. The output of the debounce filter remains in its present state unless the input remains in the opposite state for the entire period of time programmed by the Loop closure debounce interval, LCRDBI. There is also a loop closure mask interval (LCRMASK) that is used to mask transients caused when an internal ringing burst (with no offset) ends in the presence of a high REN load. If the debounce interval has been satisfied, the LCR bit is set to indicate that a valid loop closure has occurred.

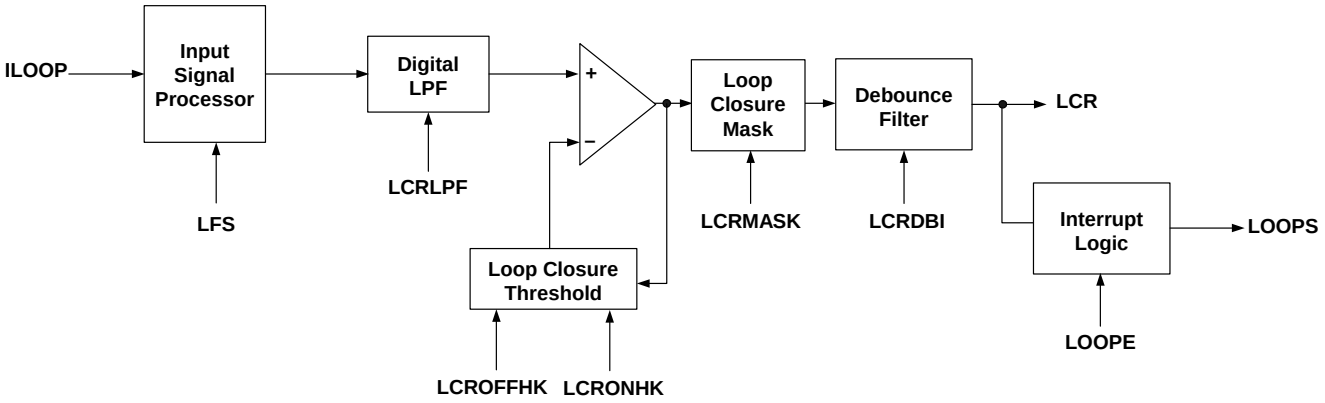


Figure 20. Discrete Linefeed Circuit for Power Monitoring

Table 21. Register and RAM Locations Used for Loop Closure Detection

Parameter	Register/RAM Mnemonic	Register/RAM Bits	Programmable Range	LSB Size	Effective Resolution
Loop Closure Interrupt Pending	IRQVEC2	LOOPS	Yes/No	N/A	N/A
Loop Closure Interrupt Enable	IRQEN2	LOOPE	Yes/No	N/A	N/A
Linefeed Shadow	LINEFEED	LFS[2:0]	Monitor only	N/A	N/A
Loop Closure Detect Status	LCRRTP	LCR	Monitor only	N/A	N/A
Loop Closure Detect Debounce Interval	LCRDBI	LCRDBI[15:0]	0 to 40.96 s	1.25 ms	1.25 ms
Loop Current Sense	ILOOP	ILOOP[15:0]	50.54 to 101.09 mA	3.097 μA	500 μA[1]

Table 21. Register and RAM Locations Used for Loop Closure Detection (Continued)

Loop Closure Threshold (on-hook to off-hook)	LCROFFHK	LCROFFHK[15:0]	0 to 101.09 mA[2]	3.097 µA	396.4 µA
Loop Closure Threshold (off-hook to on-hook)	LCRONHK	LCRONHK[15:0]	0 to 101.09 mA[2]	3.097 µA	396.4 µA
Loop Closure Filter Coefficient	LCRLPF	LCRLPF[15:3]	0 to 4000h	N/A	N/A
Loop Closure Mask Interval	LCRMASK	LCRMASK[15:0]	0 to 40.96s	1.25 ms	1.25 ms

Notes:
1. I_{LOOP} is a calculated value based on measured I_{Q1}–I_{Q4} increments. The resulting effective resolution is approximately 500 µA.
2. The usable range for LCRONHK and LCROFFHK is limited to 61 mA. Entering a value > 61 mA will disable threshold detection.

Ground Key Detection

Ground Key detection detects an alerting signal from the terminal equipment during the Active linefeed state (forward or reverse polarity). The functional blocks required to implement a Ground Key detector are shown in Figure 21, and the register set for detecting a ground key event is provided in Table 22. The primary input to the system is the Longitudinal Current Sense value provided by the voltage/current/power monitoring circuitry and reported in the ILONG RAM address. The ILONG value is processed in the ISP provided the LFS bits in the Linefeed register indicate the device is in an Active state. The output of the ISP is the input to a programmable digital low-pass filter, which removes unwanted ac signal components before threshold detection.

The low-pass filter coefficient is calculated using the equation below and is entered into the LONGLPF RAM location.

LONGLPF = [(2πf x 4096)/800]

Where f = the desired cutoff frequency of the filter.

The programmable range of the filter is from 0 (blocks all signals) to 4000h (unfiltered). A typical value of 10 Hz (0A10h) is sufficient to filter out any unwanted ac artifacts while allowing the dc information to pass through the filter.

The output of the low-pass filter is compared to the programmable threshold, LONGHITH. Hysteresis is enabled by programming a second threshold, LONGLOTH, to detect when the ground key is released. The threshold comparator output feeds a programmable debounce filter. The output of the debounce filter remains in its present state unless the input remains in the opposite state for the entire period of time programmed by the loop closure debounce interval, LONGDBI. If the debounce interval is satisfied, the LONGHI bit is set to indicate that a valid loop closure has occurred.

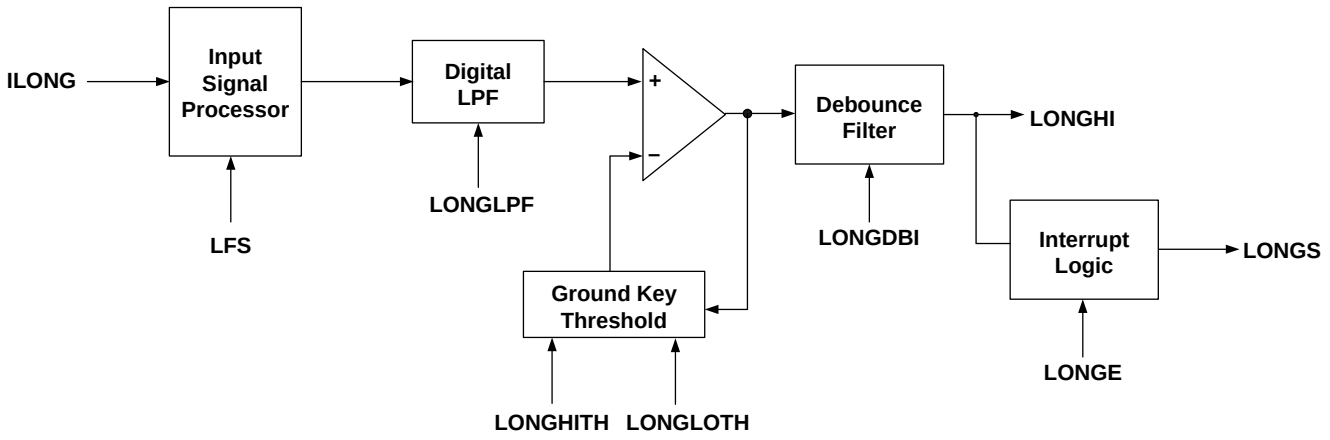


Figure 21. Ground Key Detection Circuitry

Table 22. Register and RAM Locations Used for Ground Key Detection

Parameter	Register/ RAM Mnemonics	Register/RAM Bits	Programmable Range	LSB Size	Resolution
Ground Key Interrupt Pending	IRQVEC2	LONGS	Yes/No	N/A	N/A
Ground Key Interrupt Enable	IRQEN2	LONGE	Yes/No	N/A	N/A
Ground Key Linefeed Shadow	LINEFEED	LFS[2:0]	Monitor only	N/A	N/A
Ground Key Detect Status	LCRRTP	LONGHI	Monitor only	N/A	N/A
Ground Key Detect Debounce Interval	LONGDBI	LONGDBI[15:0]	0 to 40.96 s	1.25 ms	1.25 ms
Longitudinal Current Sense	ILONG	ILONG[15:0]	Monitor only		See Table 19
Ground Key Threshold (enabled)	LONGHITH	LONG-HITH[15:0]	0 to 101.09 mA*	3.097 µA	396.4 µA
Ground Key Threshold (released)	LONGLOTH	LON-GLOTH[15:0]	0 to 101.09 mA*	3.097 µA	396.4 µA
Ground Key Filter Coeffi-cient	LONGLPF	LONGLPF[15:3]	0 to 4000h	N/A	N/A

***Note:** The usable range for LONGHITH and LONGLOTH is limited to 16 mA. Setting a value > 16 mA will disable threshold detection.

Automatic Dual Battery Switching

The Dual ProSLIC chipsets provide the ability to switch between several user-provided battery supplies to aid thermal management. Two specific scenarios where this method may be required are as follows:

- **Ringing to off-hook state transition (Si3220):** During the on-hook operating state, the Dual ProSLIC chipset must operate from the ringing battery supply to provide the desired ringing signal when required. Once an off-hook condition is detected, the Dual ProSLIC chipset must transition to the lower battery supply, typically –24 V, to reduce power dissipation during the active state. The low current consumed by the Dual ProSLIC chipset during the on-hook state results in very little power dissipation while being powered from the ringing battery supply, which can have an amplitude as high as –100 V depending on the desired ringing amplitude.
- **On-hook to off-hook state, short loop feed (Si3225):** When sourcing both long and short loop lengths, the Dual ProSLIC chipset can automatically switch from the typical –48 V off-hook battery supply to a lower off-hook battery supply (e.g., –24 V) to reduce the total off-hook power dissipation. The Dual ProSLIC chipset continuously monitors the TIP-RING voltage and selects the lowest battery voltage required to power the loop when transitioning from the on-hook to the off-hook state, thus assuring the lowest power dissipation.

The BATSELa and BATSELb pins switch between the two battery voltages based on the operating state and the TIP-RING voltage. Figure 22 illustrates the chip connections required to implement an automatic dual battery switching scheme. When BATSEL is pulled LOW, the desired channel is powered from the V_{BATL} supply. When BATSEL is pulled HIGH, the V_{BATH} source supplies power to the desired channel.

The BATSEL pins for both channels are controlled using the BATSEL bit of the RLYCON register and can be programmed to automatically switch to the lower battery supply (V_{BATL}) when the off-hook TIP-RING voltage is low enough to allow proper operation from the lower supply. When using the Si3220, this mode should always be enabled to allow seamless switching between the ringing and off-hook states. The same switching scheme is used with the Si3225 to reduce power by switching to a lower off-hook battery when sourcing a short loop.

Two thresholds are provided to enable battery switching with hysteresis. The BATHTH RAM location specifies the threshold at which the Dual ProSLIC device switches from the low battery (V_{BATL}) to the high battery (V_{BATH}) due to an off-hook to on-hook transition. The BATLTH RAM location specifies the threshold at which the Si3220/Si3225 switches from V_{BATH} to V_{BATL} due to a transition from the on-hook or ringing state to the off-hook state or because the overhead during active Off-Hook mode is sufficient to feed the subscriber loop using a lower battery voltage.

The low pass filter coefficient is calculated using the equation below and is entered into the BATLPF RAM location.

BATLPF = [(2πf x 4096)/800]

Where f = the desired cutoff frequency of the filter

The programmable range of the filter is from 0 (blocks all signals) to 4000h (unfiltered). A typical value of 10 Hz (0A10h) is sufficient to filter out any unwanted ac artifacts while allowing the dc information to pass through the filter.

Table 23 provides the register and RAM locations used for programming the battery switching functions.

Table 23. Register and RAM Locations Used for Battery Switching

Parameter	Register/RAM Mnemonic	Register/RAM Bits	Programmable Range	Resolution (LSB Size)
Battery Select Switch	RLYCON	BATSEL	Toggle	N/A
High Battery Detect Threshold	BATHTH	BATHTH[14:7]	0 to 160.173 V*	628 mV (4.907 mV)
Low Battery Detect Threshold	BATLTH	BATLTH[14:7]	0 to 160.173 V*	628 mV (4.907 mV)
Ringing Battery Switch (Si3220 only)	RLYCON	GPO	Toggle	N/A
Battery Select Indicator	RLYCON	BSEL	Toggle	N/A
Battery Switching LPF	BATLPF	BATLPF[15:3]	0 to 4000h	N/A
***Note:** Usable range for BATHTH and BATLTH is limited to VBATH.				

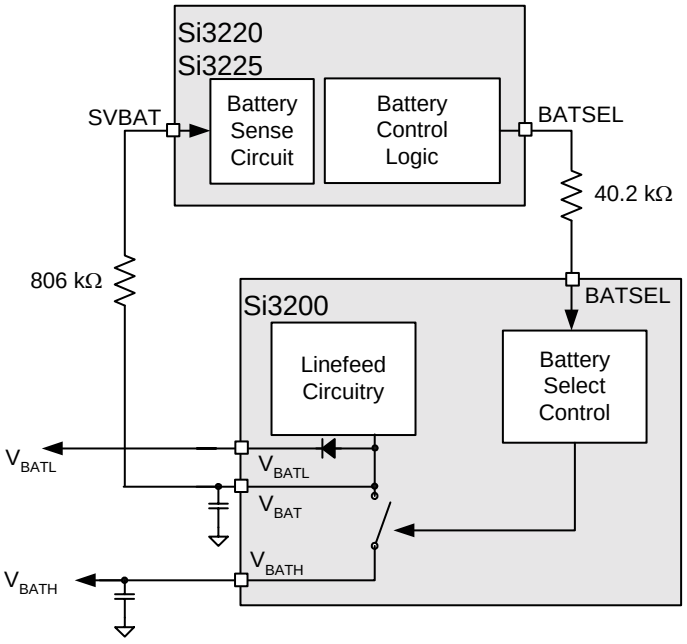


Figure 22. External Battery Switching Using the Si3220/Si3225

When generating a high-voltage ringing amplitude using the Si3220, the power dissipated during the OHT state typically increases due to operating from the ringing battery supply in this mode. To reduce power, the Si3220/Si3200 chipset provides the ability to accommodate up to three separate battery supplies by implementing a secondary battery switch using a few low-cost external components as illustrated in Figure 22. The Si3220's BATSEL pin is used to switch between the VBATH (typically –48 V) and VBATL (typically –24 V) rails using the switch internal to the Si3200. The Si3220's GPO pin is used along with the external transistor circuit to switch the VRING rail (the ringing voltage battery rail) onto the Si3200's VBAT pin when ringing is enabled. The GPO signal is driven automatically by the ringing cadence provided that the RRAIL bit of the RLYCON register is set to 1 (signifying that a third battery rail is present).

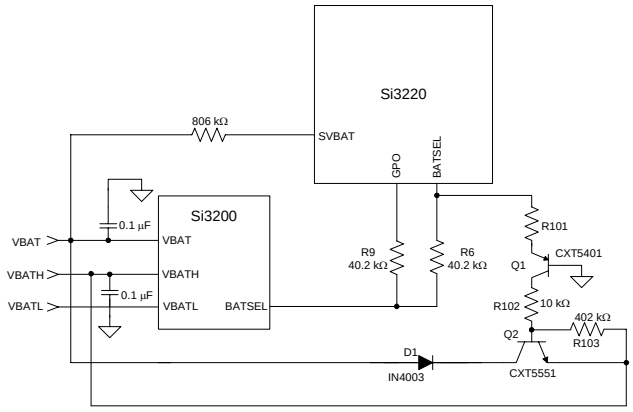


Figure 23. 3-Battery Switching with Si3220/ Si3200

Table 24. 3-Battery Switching Components

Component	Value	Comments
D1	200 V, 200 mA	1N4003 or similar
Q1	100 V PNP	CXT5401 or similar
Q2	100 V NPN	CXT5551 or similar
R101	1/10 W, ± 5%	2.4 kΩ for V_{DD}=3.3 V 3.9 kΩ for V_{DD}=5 V

Table 24. 3-Battery Switching Components

Component	Value	Comments
R102	10 kΩ,1/10 W, ± 5%	
R103	402 kΩ,1/10 W,± 1%	

Ringing Generation

The Si3220-based Dual ProSLIC chipset provides a balanced ringing waveform, with or without dc offset. The ringing frequency, cadence, waveshape, and dc offset are register programmable.

Using a balanced ringing scheme, the ringing signal is applied to both the TIP and the RING lines using ringing waveforms that are 180° out of phase with each other. The resulting ringing signal seen across TIP-RING is twice the amplitude of the ringing waveform on either the TIP or the RING line, which allows the ringing circuitry to withstand half the total ringing amplitude seen across TIP-RING.

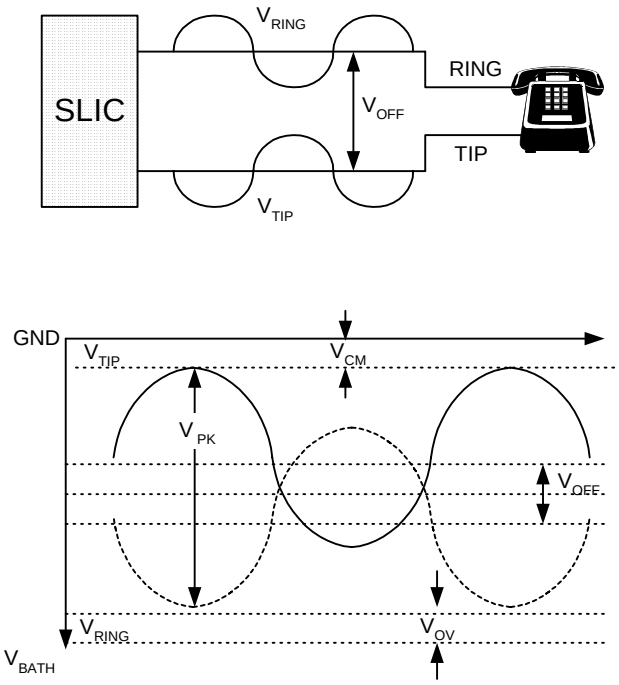


Figure 24. Balanced Ringing

An internal ringing scheme provides >40 Vrms into a 5REN load at the terminal equipment using a user-provided ringing battery supply. The specific ringing supply voltage required depends on the ringing voltage desired. The ringing amplitude at the terminal equipment depends on the loop impedance as well and

the load impedance in REN. The following equation can be used to determine the TIP-RING ringing amplitude required for a specific load and loop condition.

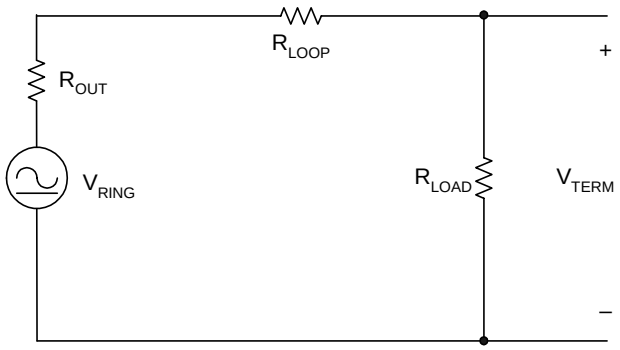


Figure 25. Simplified Loop Circuit During Ringing

$$V_{TERM} = V_{RING} \times \left[\frac{R_{LOAD}}{(R_{LOAD} + R_{LOOP} + R_{OUT})}\right]$$

where

R_{LOOP} = (0.09Ω per foot for 26AWG wire)

$$R_{OUT} = 320\Omega$$

$$R_{LOAD} = \frac{7000\Omega}{\#REN}$$

When ringing longer loop lengths, adding a dc offset voltage is necessary to reliably detect a ring trip condition (off-hook phone). Adding dc offset to the ringing signal decreases the maximum possible ringing amplitude. Adding significant dc offset also increases the power dissipation in the Si3200 and may require additional airflow or modified PCB layout to maintain acceptable operating temperatures in the line feed circuitry. The Dual ProSLIC chipset automatically applies and removes the ringing signal during V_{OC}-crossing periods to reduce noise and crosstalk to adjacent lines. Table 25 provides a list of registers required for internal ringing generation

Table 25. Register and RAM Locations Used for Ringing Generation

Parameter	Register/ RAM Mnemonic	Register/RAM Bits	Programmable Range	Resolution (LSB Size)
Ringing Waveform	RINGCON	TRAP	Sinusoid/Trapezoid	N/A
Ringing Active Timer Enable	RINGCON	TAEN	Enabled/Disabled	N/A
Ringing Inactive Timer Enable	RINGCON	TIEN	Enabled/Disabled	N/A
Ringing Oscillator Enable Monitor	RINGCON	RINGEN	Enabled/Disabled	N/A
Ringing Oscillator Active Timer	RINGTALO/ RINGTAHI	RINGTA[15:0]	0 to 8.19 s	125 µs
Ringing Oscillator Inactive Timer	RINGTILO/ RINGTIHI	RINGTI[15:0]	0 to 8.19 s	125 µs
Linefeed Control (Initiates Ringing State)	LINEFEED	LF[2:0]	000 to 111	N/A
On-Hook Line Voltage	VOC	VOC[15:0]	0 to 63.3 V	1.005 V (4.907 mV)
Ringing Voltage Offset	RINGOF	RINGOF[15:0]	0 to 63.3 V	1.005 V (4.907 mV)
Ringing Frequency	RINGFRHI/ RINGFRLO	RINGFRHI[14:3]/ RINGFRLO[14:3]	4 to 100 Hz	
Ringing Amplitude	RINGAMP	RINGAMP[15:0]	0 to 160.173 V	628 mV (4.907 mV)

Table 25. Register and RAM Locations Used for Ringing Generation (Continued)

Parameter	Register/ RAM Mnemonic	Register/RAM Bits	Programmable Range	Resolution (LSB Size)
Ringing Initial Phase Sinusoidal Trapezoid External Ringing	RINGPHAS	RINGPHAS[15:0]	 N/A 0 to 1.024 s 0 to 662.83 mA	 N/A 31.25 µs 2.6 mA (20.3 µA)
Ringing Relay Driver Enable (Si3225 only)	RELAYCON	RDOE	Enabled/Disabled	N/A
Ringing Overhead Voltage	VOVRING	VOVRING[15:0]	0 to 63.3 V	1.005 V (4.907 mV)

Internal Sinusoidal Ringing

A sinusoidal ringing waveform is generated by the on-chip digital tone generator. The tone generator used to generate ringing tones is a two-pole resonator with a programmable frequency and amplitude. Since ringing frequencies are low compared to the audio band signaling frequencies, the sinusoid is generated at a 1 kHz rate. The ringing generator is programmed via the RINGFREQ, RINGAMP, and RINGPHAS registers. The equations are as follows:

$$\text{coeff} = \cos\left(\frac{2\pi f}{1000\text{Hz}}\right)$$

$$\text{RINGAMP} = \frac{1}{4}\sqrt{\frac{1-\text{coeff}}{1+\text{coeff}}} \times (2^{15}) \times \frac{\text{Desired}V_{PK}}{160.173\text{V}}$$

$$\text{RINGPHAS} = 0$$

For example, to generate a 60 V_{rms} (87 V_{PK}), 20 Hz ringing signal, the equations are as follows:

$$\text{RINGFREQ} = \text{coeff}(2^{23})$$

$$\text{coeff} = \cos\left(\frac{2\pi 20}{1000\text{Hz}}\right) = 99211$$

$$\text{RINGFREQ} = 99211 \times (2^{23}) = 8322461 = 0\text{x}7\text{EFD9D}$$

$$\text{RINGAMP} = \frac{1}{4}\sqrt{\frac{00789}{1.99211}} \times (2^{15}) \times \frac{85}{160.173} = 273 = 0\text{x}111$$

In addition to the variable frequency and amplitude, a selectable dc offset (V_{OFF}), which can be added to the waveform is included. The dc offset is defined in the RINGOF RAM location.

As with the tone generators, the ringing generator has two timers which function as described above. They allow on/off cadence settings up to 8 s on/8 s off. In addition to controlling ringing cadence, these timers control the transition into and out of the ringing state.

To initiate ringing, the user must program the RINGFREQ, RINGAMP, and RINGPHAS RAM addresses as well as the RINGTA and RINGTI registers, and select the ringing waveshape and dc offset. After this is done, TAEN and TIEN bits are set as desired. Ringing state is invoked by a write to the linefeed register. At the expiration of RINGTA, the Dual ProSLIC turns off the ringing waveform and goes to the on-hook transmission state. At the expiration of RINGTI, ringing is initiated again. This process continues as long as the two timers are enabled and the linefeed register remains in the ringing state.

Internal Trapezoidal Ringing

In addition to the traditional sinusoidal ringing waveform, the Dual ProSLIC can generate a trapezoidal ringing waveform similar to the one illustrated in Figure 26. The RINGFREQ, RINGAMP, and RINGPHAS RAM addresses are used for programming the ringing wave shape as follows:

RINGPHAS = 4 x Period x 8000

RINGAMP = (Desired V/160.8 V) x (2^{15})

RINGFREQ = (2 x RINGAMP)/(t_{RISE} x 8000)

RINGFREQ is a value that is added or subtracted from the waveform to ramp the signal up or down in a linear fashion. This value is a function of rise time, period, and amplitude, where rise time and period are related through the following equation for the crest factor of a trapezoidal waveform.

$$t_{RISE} = \frac{3}{4}T\left(1 - \frac{1}{CF^2}\right)$$

where

$$T = \text{Period} = \frac{1}{f_{RING}} CF = \text{desired crest factor}$$

So for a 90 V_{PK}, 20 Hz trapezoidal waveform with a crest factor of 1.3, the period is 0.05 s and the rise time requirement is 0.015 s.

RINGPHAS = 4 x 0.05 x 8000 = 1600 (0x0640)

RINGAMP = 90/160.8 x (2^{15}) = 18340 (0x47A5)

RINGFREQ = (2 x RINGAMP)/(0.0153 x 8000) = 300 (0x012C)

The time registers and interrupts described in the sinusoidal ring description also apply to the trapezoidal ring waveform.

Ringing Coefficients

The ringing coefficients are calculated in decimal for sinusoidal and trapezoidal waveforms. The RINGPHAS and RINGAMP hex values are decimal to hex conversions in 16-bit, 2's complement representations for their respective RAM locations.

To obtain sinusoidal RINGFREQ RAM values, the RINGFREQ decimal number is converted to a 24-bit 2's complement value. The lower 12 bits are placed in RINGFRLO bits 14:3. RINGFRLO bits 15 and 2:0 are cleared to 0. The upper 12 bits are set in a similar manner in RINGFRHI, bits 13:3. RINGFRHI bit 14 is the sign bit and RINGFRHI bits 2:0 are cleared to 0.

For example, the register values for RINGFREQ=0x7EFD9D are as follows:

RINGFRHI = 0x3F78
RINGFRLO = 0x6CE8

To obtain trapezoidal RINGFREQ RAM values, the RINGFREQ decimal number is converted to an 8-bit, 2's complement value. This value is loaded into RINGFRHI. RINGFRLO is not used.

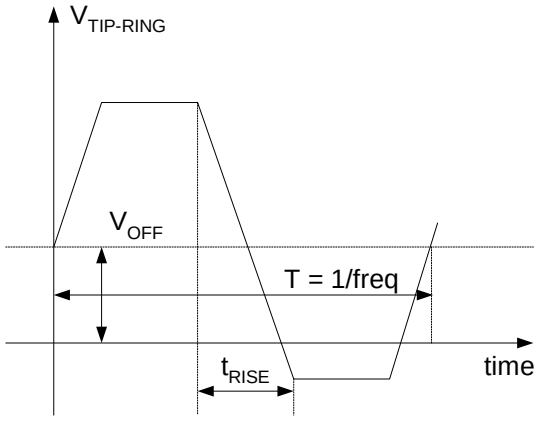


Figure 26. Trapezoidal Ringing Waveform

Ringing DC Offset Voltage

A dc offset voltage can be added to the Si3220's ac ringing waveform by programming the RINGOF RAM location to the appropriate setting. The value of RINGOF is calculated as follows:

$$RINGOF = \frac{V_{OFF}}{64.32} \times 2^{15}$$

External Unbalanced Ringing

The Si3225 supports centralized, battery-backed unbalanced ringing schemes by providing a ringing relay driver as well as inputs from an external ring trip circuit. Using this scheme, line-card designers can use the Dual ProSLIC chipset in existing system architectures with minimal system changes.

Linefeed Overhead Voltage Considerations During Ringing

The ringing mode output impedance allows ringing operation without overhead voltage modification (VOVR = 0). If an offset of the ringing signal from the ring lead is desired, VOVR can be used for this purpose.

Ringing Power Considerations

The total power consumption of the Si3220/Si3200 chipset using internal ringing generation is dependent on the VDD supply voltage, the desired ringing amplitude, the total loop impedance, and the AC load impedance (number of REN). The following equations can be used to approximate the total current required for each channel during ringing mode.

V_{DD} = 3.3 V:

$$I_{DD,AVE} = 22mA + (6mA \times REN)$$

V_{DD} = 5 V:

$$I_{DD,AVE} = 26mA + (6mA \times REN)$$

And

$$I_{BAT,RMS} = \left[\frac{V_{RING,RMS}}{R_{LOAD} + R_{LOOP} + R_{OUT}}\right] \times \frac{2.04}{\pi}$$

Where:

REN = number of REN

R_{LOAD} = 7000/REN for North America

R_{LOOP} = loop impedance

R_{OUT} = ProSLIC output impedance = 320 Ω

Ring Trip Detection

A ring trip event signals that the terminal equipment has transitioned to an off-hook state after ringing has commenced, ensuring that the ringing signal is removed before normal speech begins. The Dual ProSLIC is designed to implement either an ac- or dc-based internal ring trip detection scheme or a combination of both schemes. The system design is flexible to address varying loop lengths of different applications. An ac ring trip detection scheme cannot reliably detect an off-hook condition when sourcing longer loop lengths, as the 20 Hz ac impedance of an off-hook long loop is indistinguishable from a heavily loaded (5 REN) short loop in the on-hook state. Therefore, a dc ring trip detection scheme is required when sourcing longer loop lengths.

The Si3220 can implement either an ac- or dc-based ring trip detection scheme, depending on the application. The Si3225 allows external dc ring trip detection when using a battery-backed external ringing generator by monitoring the ringing feed path through two sensing inputs on each channel. By monitoring this path, the Dual ProSLIC detects a dc current flowing in the loop once the end equipment has gone off-hook. Table 26 provides recommended register and RAM settings for various applications, and Table 27 lists the register and RAM addresses that must be written or monitored to correctly detect a ring trip condition.

Figure 27 illustrates the internal functional blocks that correctly detect and process a ring trip event. The primary input to the system is the loop current sense (ILOOP) value provided by the loop monitoring circuitry and reported in the ILOOP RAM location register. The ILOOP RAM location value is processed by the ISP block when the LFS bits in the Linefeed register indicate the device is in the ringing state. The output of the ISP then feeds into a pair of programmable digital low-pass filters; one for the ac ring trip detection path and one for the dc path. The ac path also includes a full wave rectifier block prior to the LPF block. The outputs of each low pass filter block are then passed on to a programmable ring trip threshold (RTACTH for ac detection and RTDCTH for dc detection). Each threshold block output is then fed to a programmable debounce filter to ensure a valid ring trip event. The output of each debounce filter remains constant unless the input remains in the opposite state for the entire period of time set using the ac and dc ring trip debounce interval registers, RTACDB and RTDCDB, respectively. The outputs of both debounce filter blocks are then ORed together. If either the ac or the dc ring trip circuits indicate a valid ring trip event has occurred, the RTP bit is set. Either the ac or dc ring trip detection circuits are disabled by setting the respective ring trip threshold sufficiently high so that it does not trip under any condition. A ring trip interrupt also generates if the RTRIPE bit is enabled.

Ringtrip Timeout Counter

The Dual ProSLIC incorporates a ringtrip timeout counter (RTCOUNT) that will monitor the status of the ringing control. When exiting ringing, the Dual ProSLIC will allow the ringtrip timeout counter amount of time (RTCOUNT x 1.25 ms/LSB) for the mode to switch to On-hook Transmission or Active. The mode that is being exited to is governed by whether the command to exit ringing is a ringing active timer expiration (on-hook transmission) or ringtrip/manual mode change (Active mode). The ringtrip timeout counter will assure ringing is exited within its time setting (RTCOUNT x 1.25 ms/LSB, typically 200 ms).

Ringtrip Debounce Interval

The ac and dc ring trip debounce intervals can be calculated based on the following equations:

$RTACDB = t_{debounce}\ (1600/RTPER)$

$RTDCDB = t_{debounce}\ (1600/RTPER)$

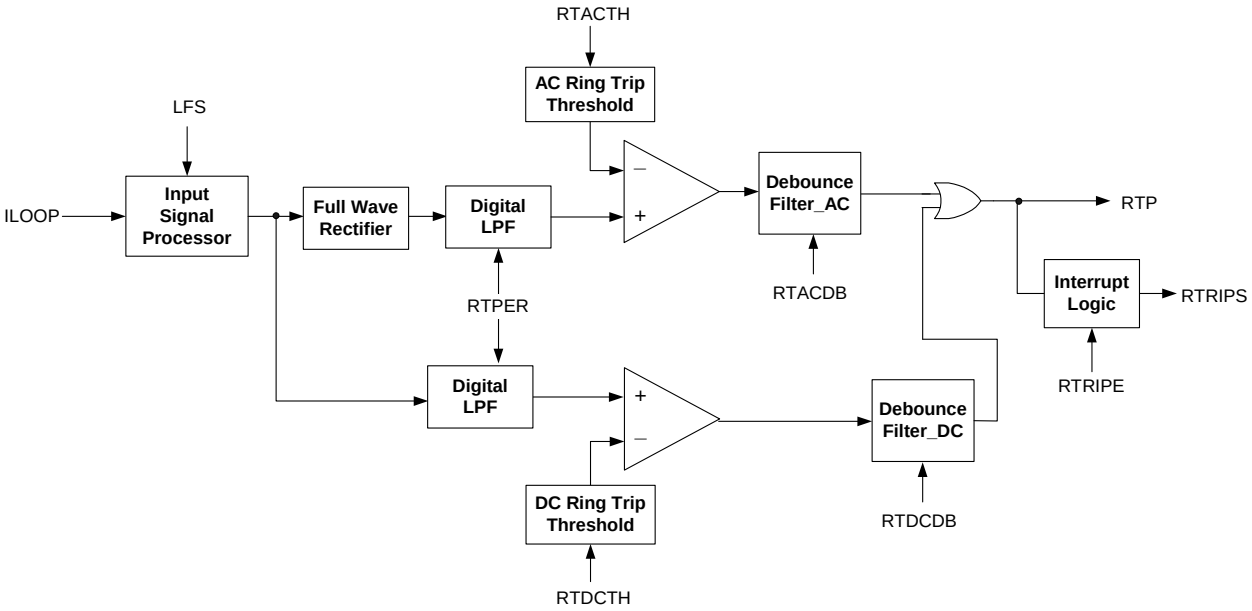


Figure 27. Ring Trip Detect Processing Circuitry

Table 26. Recommended Values for Ring Trip Registers and RAM Addresses[1]

Ringing Method	Ringing Frequency	DC Offset Added?	RTPER	RTACTH	RTDCTH	RTACDB/ RTDCDB
Internal (Si3220)	16–32 Hz	Yes	$800/f_{RING}$	221 x RTPER	$0.577(RTPER \times V_{OFF})$	See Note [2]
		No	$800/f_{RING}$	$1.59 \times V_{RING,PK} \times RTPER$	32767	
	33–60 Hz	Yes	$2(800/f_{RING})$	221 x RTPER	$0.577(RTPER \times V_{OFF})$	
		No	$2(800/f_{RING})$	$1.59 \times V_{RING,PK} \times RTPER$	32767	
External (Si3225)	16–32 Hz	Yes	$800/f_{RING}$	32767	$0.067 \times RTPER \times V_{OFF}$	
	33–60 Hz	Yes	$2(800/f_{RING})$	32767	$0.067 \times RTPER \times V_{OFF}$	

Notes:
1. All calculated values should be rounded to the nearest integer.
2. Refer to Ring Trip Debounce Interval for RTACDB and RTDCDB equations.

Table 27. Register and RAM Locations Used for Ring Trip Detection

Parameter	Register/RAM Mnemonic	Register/RAM Bits	Programmable Range	Resolution
Ring Trip Interrupt Pending	IRQVEC2	RTRIPS	Yes/No	N/A
Ring Trip Interrupt Enable	IRQEN2	RTRIPE	Enabled/Disabled	N/A
AC Ring Trip Threshold	RTACTH	RTACTH[15:0]	See Table 26	
DC Ring Trip Threshold	RTDCTA	RTDCTH[15:0]	See Table 26	
Ring Trip Sample Period	RTPER	RTPER[15:0]	See Table 26	
Linefeed Shadow (monitor only)	LINEFEED	LFS[2:0]	N/A	N/A
Ring Trip Detect Status (monitor only)	LCRRTP	RTP	N/A	N/A
AC Ring Trip Detect Debounce Interval	RTACDB	RTACDB[15:0]	0 to 40.96 s	1.25 ms
DC Ring Trip Detect Debounce Interval	RTDCDB	RTDCDB[15:0]	0 to 40.96 s	1.25 ms
Loop Current Sense (monitor only)	ILOOP	ILOOP[15:0]	0 to 101.09 mA	See Table 19

Loop Closure Mask

The Dual ProSLIC implements a loop closure mask to ensure mode change between Ringing and Active or On-hook Transmission without causing an erroneous loop closure detection. The loop closure mask register, LCRMASK, should be set such that loop closure detection is ignored for LCRMASK 1.25 ms/LSB amount of time. The programmed time is set to mask detection of transitional currents that occur when exiting the ringing mode while driving a reactive load (i.e., 5 REN). A typical setting is 80 ms (LCRMASK = 0x40).

Si3220 Ring Trip Detection

The Si3220 provides the ability to process a ring trip event using an ac-based detection scheme. Using this scheme eliminates the need to add dc offset to the ringing signal, which reduces the total power dissipation during the ringing state and maximizes the available ringing amplitude. This scheme is valid for shorter loop lengths only since it cannot reliably detect a ring trip event if the off-hook line impedance overlaps the on-hook impedance at 20 Hz.

The Si3220 also can add a dc offset component to the ringing signal and detect a ring trip event by monitoring the dc loop current flowing once the terminal equipment transitions to the off-hook state. Although adding dc offset reduces the maximum available ringing amplitude (using the same ringing supply), this method is required to reliably detect a valid ring trip event when sourcing longer loop lengths. The dc offset can be programmed from 0 to 64.32 V in the RINGOF RAM address as

required to produce adequate dc loop current in the off-hook state. Depending on the loop length and the ring trip method, the ac or dc ring trip detection circuits are disabled by setting their respective ring trip thresholds (RTACTH or RTDCTH) sufficiently high so it does not trip under any condition.

Si3225 Ring Trip Detection

The Si3225 implements an external ring trip detection scheme when using a standard battery-backed, external ringing generator. In this application, the centralized ringing generator produces an unbalanced ringing signal that is distributed to individual TIP/RING pairs. A per-channel ringing relay is required to disconnect the Si3225 from the TIP/RING pair and apply the ringing signal. By monitoring the ringing feed path across a ring feed sense resistor (R_{RING} in Figure 31) in series with the ringing source, the Si3225 can detect the dc current path created when the hook switch inside the terminal equipment closes. The internal ring trip detection circuitry is identical to that illustrated in Figure 27. Figure 31 illustrates the typical external ring trip circuitry required for the Si3225. Because of the long loop nature of these applications, a dc ring trip detection scheme is used typically. The user can disable the ac ring trip detection circuitry by setting the RTACTH threshold sufficiently high so it does not trip under any condition.

Relay Driver Considerations

The Dual ProSLIC devices include up to three dedicated relay drivers to drive external ringing and/or test relays. Test relay drivers TRD1a, TRD1b, TRD2a, and TRD2b are provided in all product versions, and ringing relay drivers RRDa and RRDb are included for the Si3225 only. In most applications, the relay can be driven directly from the Dual ProSLIC with no external relay drive circuitry required. Figure 28 illustrates the internal relay driver circuitry using a 3 V or 5 V relay.

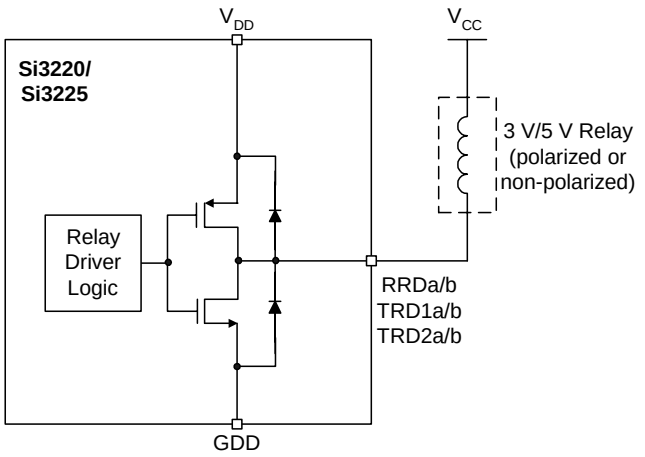


Figure 28. Dual ProSLIC Internal Relay Drive Circuitry

The internal driver logic and drive circuitry is powered by the same V_{DD} supply as the chip's main V_{DD} supply (VDD1–VDD4 pins). When operating external relays from a V_{CC} supply equal to the chip's V_{DD} supply, an internal diode network provides protection against overvoltage conditions from flyback spikes when the relay is opened. Both 3 V or 5 V relays can be used in the configuration shown in Figure 28 and either polarized or non-polarized relays are acceptable if the V_{CC} and V_{DD} supplies are identical. The input impedance (R_{IN}) of the relay driver pins is a constant 11 Ω while sinking less than the maximum rated 85 mA into the pin.

If the operating voltage of the relay (V_{CC}) is higher than the Dual ProSLIC's V_{DD} supply voltage, an external drive circuit is required to eliminate leakage from V_{CC} to V_{DD} through the internal protection diode. In this configuration, a polarized relay will provide optimal overvoltage protection and minimal external components. Figure 29 illustrates the required external drive circuit and Table 28 provides recommended values for R_{DRV} for typical relay characteristics and V_{CC} supplies. The output impedance (R_{OUT}) of the relay driver pins is a constant 63 Ω while sourcing less than the maximum rated 28 mA out of the pin.

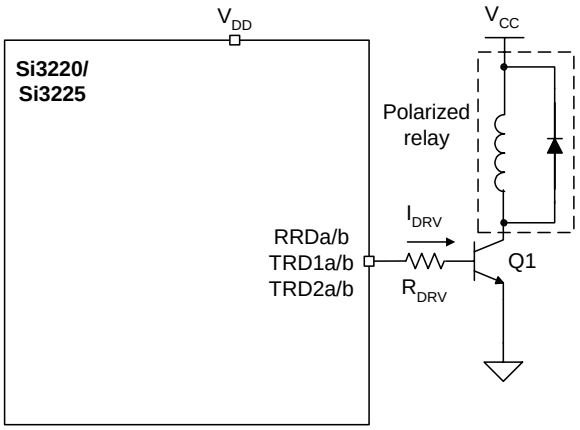


Figure 29. Driving Relays with $V_{CC} > V_{DD}$

The maximum allowable R_{DRV} value can be calculated with the following equation:

$$\text{Max}R_{DRV} = \frac{(V_{DD,MIN} - 0.6\ V)(R_{RELAY})(\beta_{Q1,MIN})}{V_{CC,MAX} - 0.3\ V} - R_{SOURCE}$$

Where $\beta_{Q1,MIN}$ ~ 30 for a 2N2222.

Table 28. Recommended R_{DRV} Values

ProSLIC V_{DD}	Relay V_{CC}	Relay R_{COIL}	Maximum R_{DRV}	Recommended 5% Value
3.3 V ±5%	3.3 V ±5%	64 Ω	Not Required	—
5 V ±5%	5 V ±5%	178 Ω	Not Required	—
3.3 V ±5%	5 V ±5%	178 Ω	2718 Ω	2.7 kΩ
3.3 V ±5%	12 V ±10%	1028 Ω	6037 Ω	5.6 kΩ
3.3 V ±5%	24 V ±10%	2880 Ω	8364 Ω	8.2 kΩ
3.3 V ±5%	48 V ±10%	7680 Ω	11092 Ω	11 kΩ
5 V ±5%	12 V ±10%	1028 Ω	9910 Ω	9.1 kΩ
5 V ±5%	24 V ±10%	2880 Ω	13727 Ω	13 kΩ
5 V ±5%	48 V ±10%	7680 Ω	18202 Ω	18 kΩ

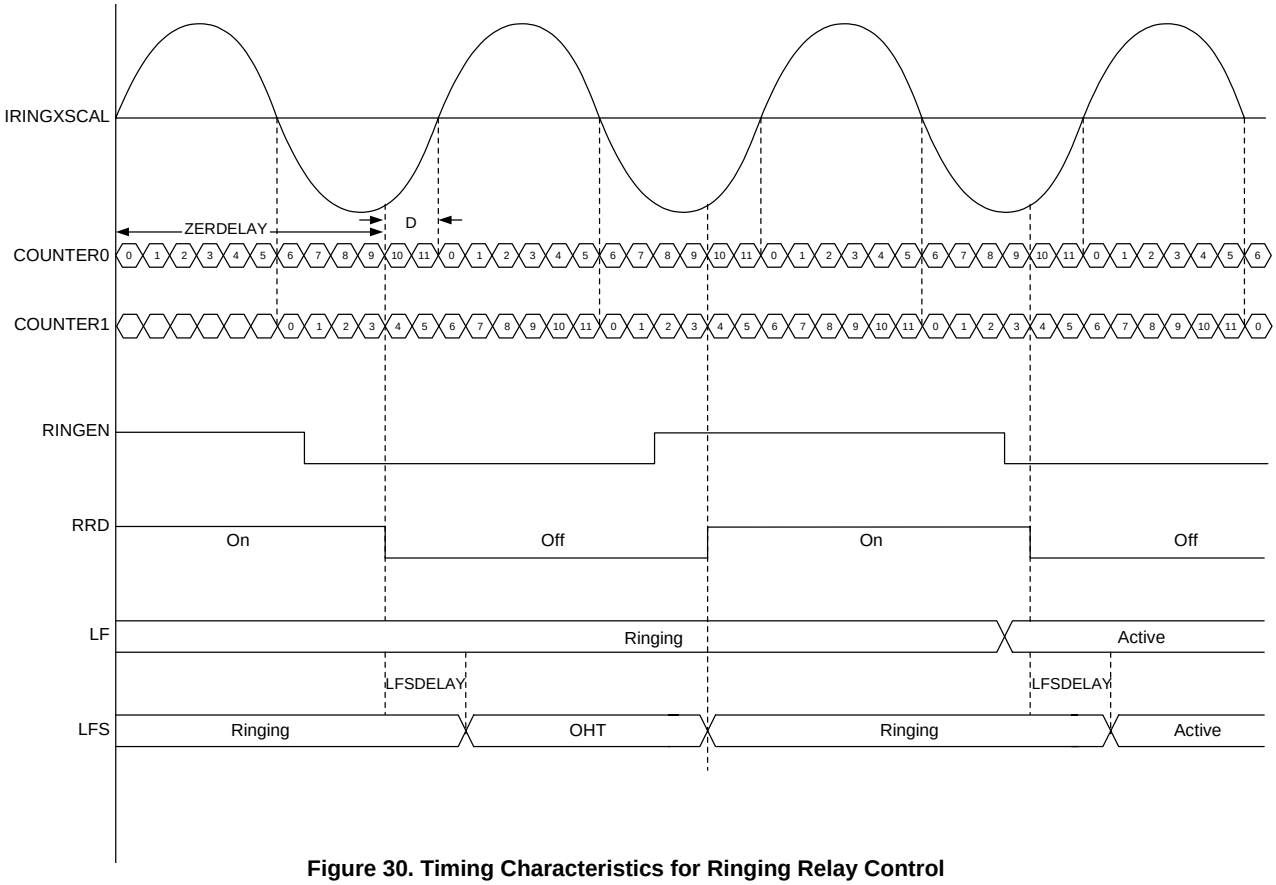


Figure 30. Timing Characteristics for Ringing Relay Control

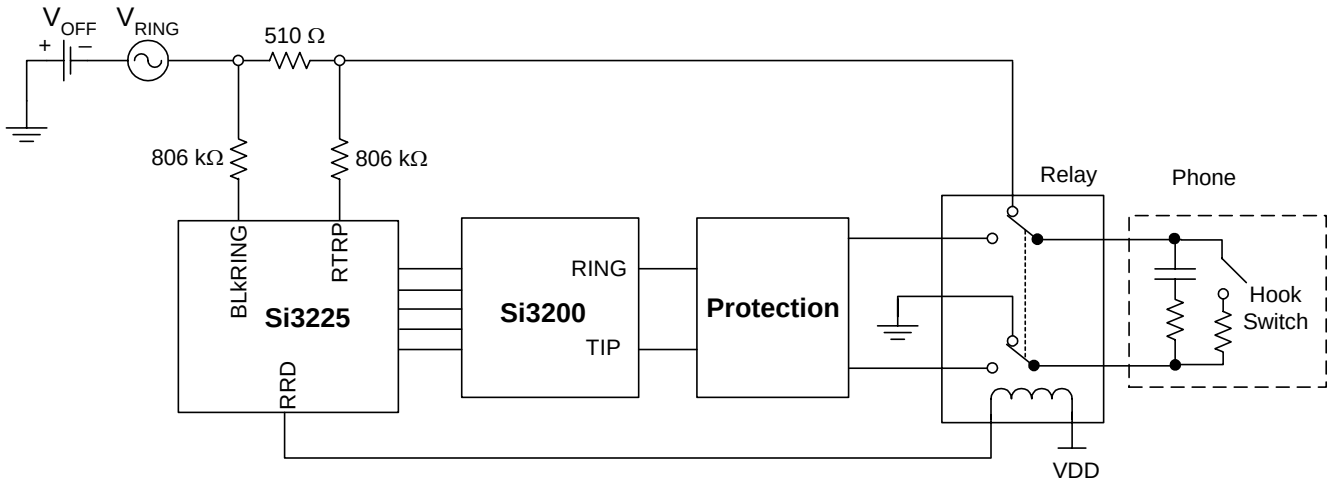


Figure 31. Si3225 External Ring Trip Circuitry

Ringing Relay Activation During Zero Crossings

The Si3225 is for applications that use a centralized ringing generator and a per-channel ringing relay to connect the ringing signal to the TIP/RING pair. The Si3225 has one relay driver output per channel (RRDa and RRDb) that can drive a mechanical or solid-state DPDT relay. To reduce impulse noise that can couple into adjacent lines, the relay should be closed when there is zero voltage across the relay contacts and opened during periods when there is zero current through the contacts.

Closing the Relay at Zero Voltage

Internal voltage monitoring circuitry closes the relay at zero voltage with respect to the line voltage. By observing the phase of the ringing signal and constantly monitoring the open-circuit T-R voltage, V_{OC}, the Si3225 can detect the next time when there is zero voltage across the relay contacts.

Opening the Relay at Zero Current

Opening the ringing relay at zero current also is accomplished using the internal monitoring circuitry and prevents arcing from excess current flow when the relay contacts are opened. The current flowing through the ringing relay is continuously monitored in the IRNGNG RAM address, and two internal counters (COUNTER0 and COUNTER1) detect time elapsed since the last two zero current crossings based on the ringing period and predict when the next zero crossing occurs. The ringing relay current and internal counters are both updated at an 8 kHz rate. To account for the mechanical delay of the relay, a programmable advance firing timer allows the user to initiate relay opening up to 10 ms prior to the zero current crossing event. Figure 30 illustrates the timing sequence for a typical ringing relay control application.

During a typical ringing sequence, the Si3225 monitors both the ringing relay current (IRNGNG) and the RINGEN bit of the RINGCON register. The RINGEN bit toggles because of pre-programmed ringing cadence or a change in operating state. COUNTER0 and COUNTER1 are re-started at each alternating zero current crossing event, and the delay period ZERDELAY equal to the ringing frequency period less the desired advance firing time (D) is entered by the user. If either counter reaches the same value as ZERDELAY, the relay control signal is enabled when the RINGEN bit transition has already occurred. During typical ringing bursts, the LFS bits of the Linefeed register toggle between the RINGING and OHT states based on the pre-programmed ringing cadence. The transition from OHT to RINGING is synchronized with the RRD state transitions so the ringing burst starts immediately. The transition from RINGING to OHT is gated by a user-programmed delay period LFSDELAY that ensures the ringing burst has ceased before going to the OHT state or to the ACTIVE state in response to a Linefeed state change.

Polarity Reversal

The Dual ProSLIC devices support polarity reversal for message waiting functionality and various signaling modes. The ramp rate can be programmed for a smooth transition or an abrupt transition to accommodate different application requirements. A wink function is provided for special equipment that responds to a smooth ramp to V_{OC} = 0 V. Table 29 illustrates the register bits required to program the polarity reversal modes.

Setting the Linefeed register to the opposite polarity immediately reverses (hard reversal) the line polarity. For example, to transition from Forward Active mode to Reverse Active mode changes LF[2:0] from 001 to 101. Polarity reversal is accommodated in the OHT and ground start modes. The POLREV bit is a read-only bit that reflects if the device is in Polarity Reversal mode.

For smooth polarity reversal, set the PREN bit to 1 and the RAMP bit to 0 or 1 depending on the desired ramp rate (see Table 29). Polarity reversal is then accomplished by toggling the linefeed register from forward to reverse modes as desired.

A wink function slowly ramps down the TIP-RING voltage (V_{OC}) to 1 followed by a return to the original VOC value (set in the VOC RAM location). This scheme lights a message-waiting lamp in certain handsets. No change to the linefeed register is necessary to enable this function. Instead, the user sets the VOCZERO bit to 1 so that the TIP-RING voltage collapses to 0 V at the rate programmed by the RAMP bit. Setting the VOCZERO bit back to 0 returns the TIP-RING voltage to its normal setting. With a software timer, the user can automate the cadence of the wink function. Figure 32 illustrates the wink function.

Table 29. Register and RAM Locations used for Polarity Reversal

Parameter	Programmable Range	Register/RAM Bits	Register/RAM Mnemonic
Linefeed	See table 15	LF[2:0]	LINEFEED
Polarity Reversal Status	Read only	POLREV	POLREV
Wink Function (Smooth transition to Voc=0V)	1 = Ramp to 0 V 0 = Return to previous V_{OC}	VOCZERO	POLREV
Smooth Polarity Reversal Enable	0 = Disabled 1 = Enabled	PREN	POLREV
Smooth Polarity Reversal Ramp Rate	0 = 1 V/1.25 ms 1 = 2 V/1.25 ms	RAMP	POLREV

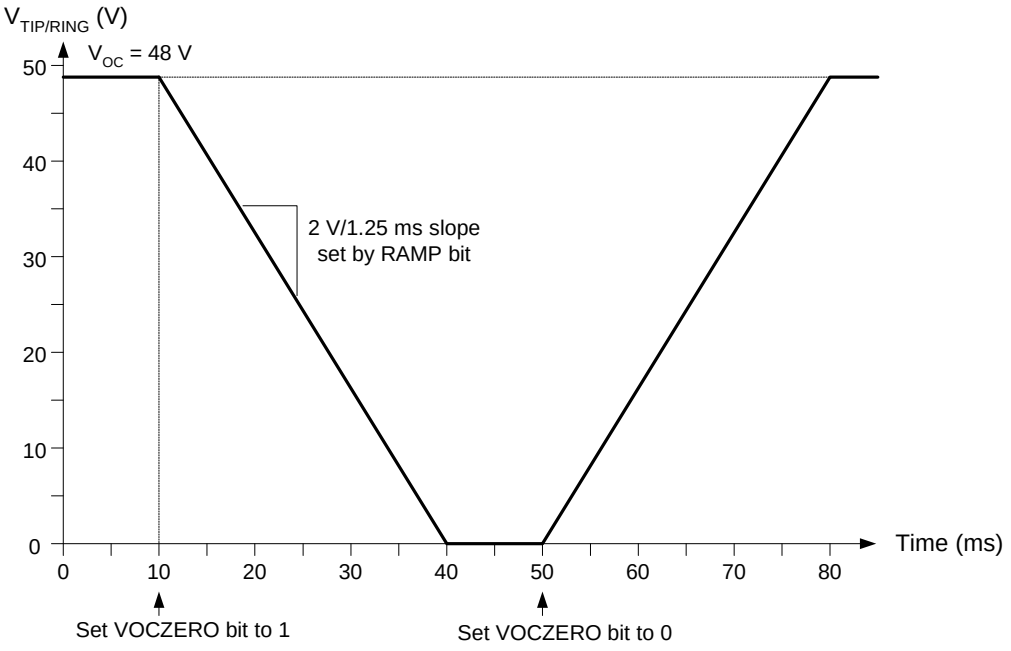


Figure 32. Wink Function with Programmable Ramp Rate

Two-Wire Impedance Synthesis

Two-wire impedance synthesis is performed on-chip to optimally match the output impedance of the Dual ProSLIC to the impedance of the subscriber loop to minimize the receive path signal reflected back onto the transmit path. The Dual ProSLIC chipset provides on-chip digitally programmable, two-wire impedance synthesis to meet return loss requirements against virtually any global two-wire impedance requirement. Real and complex two-wire impedances are realized by a programmable digital filter block. (See Z block in Figure 11 on page 22.)

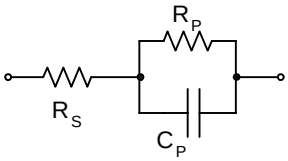


Figure 33. Two-Wire Impedance Synthesis Configuration

Table 30. Two-Wire Impedance Synthesis Limitations

Desired Configuration	Programmable Limits
R_S only	100–1000 Ω
$R_S + C_P$	$R_S \times C_P > 0.5$ ms
$R_S + R_P \| C_P$	$R_S/(R_S + R_P) > 0.1$

The two-wire impedance is programmed by loading the desired real or complex impedance value into the Si322X Coefficient Generator software in the format $R_S + R_P||C_P$, as shown in Figure 33. The software calculates the appropriate hex coefficients and loads them into the appropriate control registers (registers 33–52). The two-wire impedance can be set to any real or complex value within the boundaries set in Table 30. The actual impedance presented to the subscriber loop varies with series impedance from protection devices placed between the Dual ProSLIC chipset outputs and the TIP/RING pair according to the following equation:

$$Z_T = 2R_{PROT} + (R_S + R_P \| C_P)$$

Where: Z_T is the termination impedance presented to the TIP/RING pair

R_{PROT} is the series resistance caused by protection devices

R_S is the series portion of the synthesized impedance

$R_P||C_P$ is the parallel portion of the synthesized impedance

The user must enter the value of R_{PROT} into the software so the equalizer block can compensate for additional series impedance. (See Figure 11 on page 22.) Figure 34 illustrates the simplified two-wire impedance circuit including external protection resistors, where Z_L is the actual line impedance for the specific geographical region. The Dual ProSLIC devices can accomodate up to 50 Ω of series protection impedance per leg. The Dual ProSLIC devices load a 600 Ω default setting into the RS register if the user does not define the impedance setting, which assumes there is no additional series protection resistance.

The ac impedance generation scheme is comprised of analog and DSP-based coefficients. To turn off the analog coefficients (RS, ZP, and ZZ bits in the ZRS and ZZ registers), the user can simply set the ZSDIS bit of the ZZ register to 0. To turn off the DSP coefficients (ZA1H1 through ZB3LO registers), each register must be loaded with 0x00.

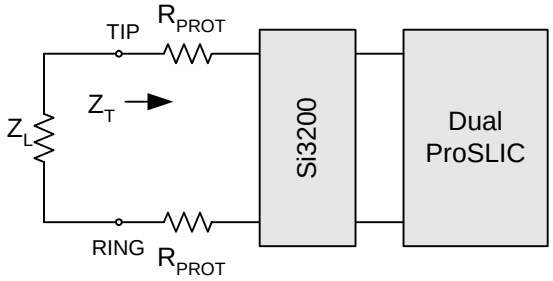


Figure 34. Two-Wire Impedance Simplified Circuit

Transhybrid Balance Filter

The Dual ProSLIC devices provide a transhybrid balance function via a digitally programmable balance filter block. (See “H” block in Figure 11 on page 22.) The Dual ProSLIC devices implement a 8-tap FIR filter and a second order IIR filter, both running at a 16 kHz sample rate. These two filters combine to form a digital replica of the reflected signal (echo) from the transmit path inputs. The user can filter settings on a per-line basis by loading the desired impedance cancellation coefficients into the appropriate registers. The Si322X Coefficient Generator software interface is provided for calculating the appropriate coefficients for the FIR and IIR filter blocks.

The transhybrid balance filters can be disabled to implement loopback diagnostic modes. To disable the transhybrid balance filter (zero cancellation), set the HYBDIS bit in the DIGCON register to 1. With the hybrid balance cancellation scheme disabled, the user can accurately measure the full transmit path signal to measure the two-wire return loss.

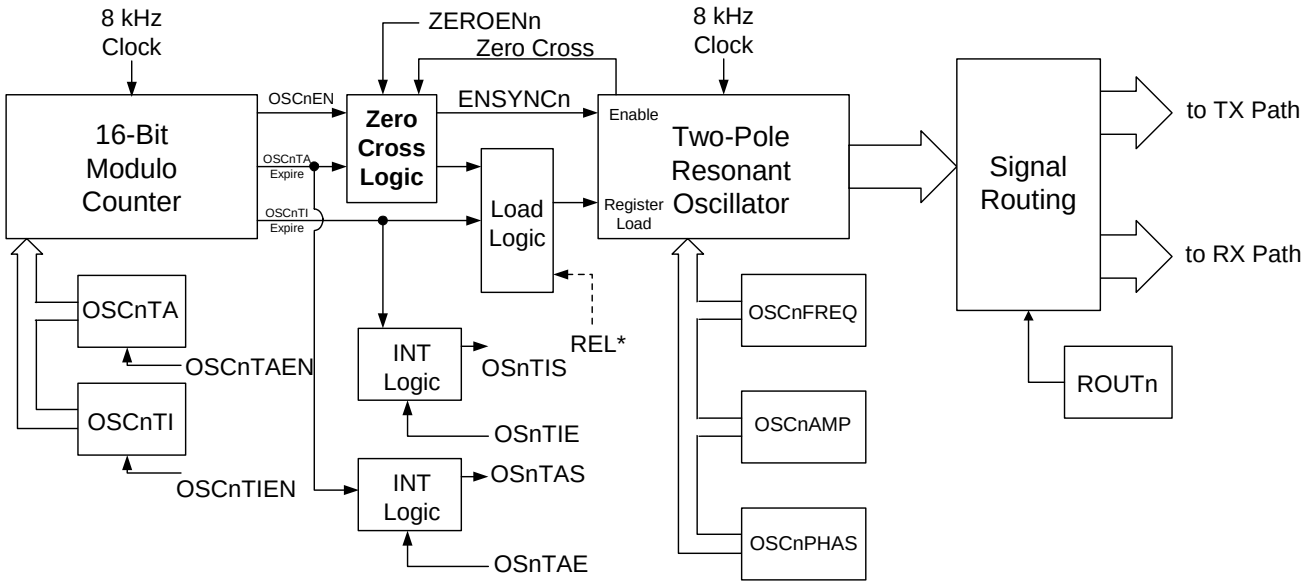
Note: The user *must* enter values into each register location to ensure correct operation when the hybrid balance block is enabled.

Tone Generators

Dual ProSLIC devices have two digital tone generators that allow a wide variety of single or dual tone frequency and amplitude combinations that spare the user the effort of generating the required POTS signaling tones on the PCM highway. DTMF, FSK (caller ID), call progress, and other tones can all be generated on-chip. The tones are sent to the receive or transmit paths. (See Figure 11 on page 22.)

Tone Generator Architecture

A simplified diagram of the tone generator architecture is shown in Figure 35. The oscillator, active/inactive timers, interrupt block, and signal routing block are connected for flexibility in creating audio signals. Control and status register bits are placed in the figure to indicate their association with the tone generator architecture. The register set for tone generation is summarized in Table 31 on page 55.



*Tone Generator 1 Only
n = "1" or "2" for Tone Generator 1 and 2, respectively

Figure 35. Tone Generator Diagram

Oscillator Frequency and Amplitude

Each of the two tone generators contains a two-pole resonant oscillator circuit with a programmable frequency and amplitude, which are programmed via RAM addresses OSC1FREQ, OSC1AMP, OSC1PHAS, OSC2FREQ, OSC2AMP, and OSC2PHAS. The sample rate for the two oscillators is 8000 Hz. The equations are as follows:

$$coeff_n = \cos(2\pi f_n/8000\ Hz),$$

where f_n is the frequency to be generated;

$$OSCnFREQ = coeff_n \times (2^{14});$$

$$OSCnAMP = \frac{1}{4}\sqrt{\frac{1-coeff}{1+coeff}} \times (2^{15}-1) \times \frac{DesiredVrms}{1.11Vrms}$$

where desired Vrms is the amplitude to be generated;

$$OSCnPHAS = 0,$$

n = 1 or 2 for oscillator 1 or oscillator 2, respectively.

For example, to generate a DTMF digit of 8, the two required tones are 852 Hz and 1336 Hz. Assuming we want to generate half-scale values (ignoring twist), the following values are calculated:

$$coeff_1 = \cos\left(\frac{2\pi 852}{8000}\right) = 0.78434$$

$$OSC1FREQ = 0.78434(2^{14}) = 12851 = 0x3233$$

$$OSC1AMP = \frac{1}{4}\sqrt{\frac{0.21556}{1.78434}} \times (2^{15}-1) \times 0.5 = 1424$$

$$= 0x590$$

$$OSC1PHAS = 0$$

$$coeff_2 = \cos(2\pi\ 1336 / 8000) = 0.49819$$

$$OSC2FREQ = 0.49819\ (2^{14}) = 8162 = 0x1FE2$$

$$OSC2AMP = \frac{1}{4}\sqrt{\frac{0.50181}{1.49819}} \times (2^{15}-1) \times 0.5 = 2370$$

$$= 0x942$$

$$OSC2PHAS = 0$$

The computed values above are written to the corresponding registers to initialize the oscillators. Once the oscillators are initialized, the oscillator control registers can be accessed to enable the oscillators and direct their outputs.

Tone Generator Cadence Programming

Each of the two tone generators contains two timers, one for setting the active period and one for setting the inactive period. The oscillator signal is generated during the active period and suspended during the inactive period. Both the active and inactive periods can be programmed from 0 to 8 seconds in 125 µs steps. The active period time interval is set using OSC1TA for tone generator 1 and OSC2TA for tone generator 2.

To enable automatic cadence for tone generator 1, define the OSC1TA and OSC1TI registers and then set the OSC1TAEN and OSC1TIEN bits. This enables each of the timers to control the state of the Oscillator Enable bit, OSC1EN. The 16-bit counter counts until the active timer expires, when the 16-bit counter resets to zero and begins counting until the inactive timer expires. The cadence continues until the user clears the OSC1TA and OSC1TIEN control bits. Setting the ZEROEN1 bit implements the zero crossing detect feature. This ensures that each oscillator pulse ends without a dc component. The timing diagram in Figure 36 is an example of an output cadence that uses the zero crossing feature.

One-shot oscillation is possible with OSC1EN and OSC1TAEN. Direct control over the cadence is achieved by setting the OSC1EN bit directly if OSC1TAEN and OSC1TIEN are disabled.

The operation of tone generator 2 is identical to that of tone generator 1 using its respective control registers.

Note: Tone Generator 2 should not be enabled simultaneously with the ringing oscillator because of resource sharing within the hardware.

Table 31. Register and RAM Locations Used for Tone Generation

Tone Generator 1			
Parameter	**Register/RAM Mnemonics**	**Register/RAM Bits**	**Description/Range (LSB Size)**
Oscillator 1 Frequency Coefficient	OSC1FREQ	OSC1FREQ[15:3]	Sets oscillator frequency
Oscillator 1 Amplitude Coefficient	OSC1AMP	OSC1AMP[15:0]	Sets oscillator amplitude
Oscillator 1 Initial Phase Coefficient	OSC1PHAS	OSC1PHAS[15:0]	Sets initial phase (default = 0)
Oscillator 1 Active Timer	O1TALO/O1TAHI	OSC1TA[15:0]	0 to 8.19 s (125 μs)
Oscillator 1 Inactive Timer	O1TILO/O1TIHI	OSC1TI[15:0]	0 to 8.19 s (125 μs)
Oscillator 1 Control	OMODE, OCON	FSKSSEN, OSC1FSK, ZEROEN1, ROUT1, ENSYNC1, OSC1TAEN, OSC1TIEN, OSC1EN	Enables all Oscillator 1 parameters
Oscillator 1 Interrupts	IRQVEC1, IRQEN1	OS1TAS, OS1TIS, OS1TAE, OS1TIE	Interrupt enable/status
Tone Generator 2			
Parameter	**Location**	**Register/RAM Address**	**Description/Range**
Oscillator 2 Frequency Coefficient	OSC2FREQ	OSC2FREQ[15:3]	Sets oscillator frequency
Oscillator 2 Amplitude Coefficient	OSC2AMP	OSC2AMP[15:0]	Sets oscillator amplitude
Oscillator 2 Initial Phase Coefficient	OSC2PHAS	OSC2PHAS[15:0]	Sets initial phase (default = 0)
Oscillator 2 Active Timer	O2TALO/O2TAHI	OSC2TA[15:0]	0 to 8.19 s (125 μs)
Oscillator 2 Inactive Timer	O2TILO/O2TIHI	OSC2TI[15:0]	0 to 8.19 s (125 μs)
Oscillator 2 Control	OMODE, OCON	ZEROEN2, ROUT2, ENSYNC2, OSC2TAEN, OSC2TIEN, OSC2EN	Enables all Oscillator 2 parameters
Oscillator 2 Interrupts	IRQVEC1, IRQEN1	OS2TAS, OS2TIS, OS2TAE, OS2TIE	Interrupt enable/status

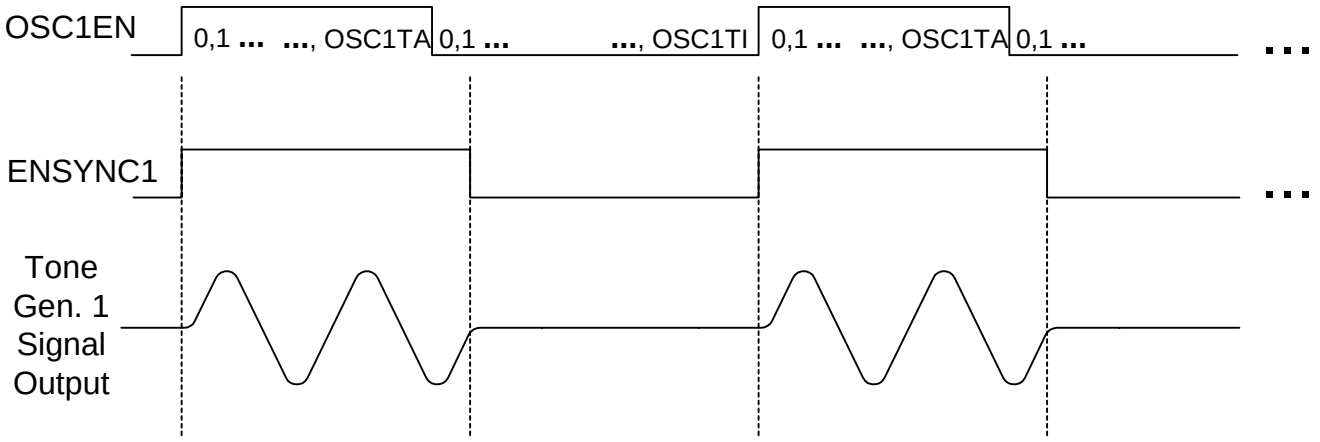


Figure 36. Tone Generator Timing Diagram

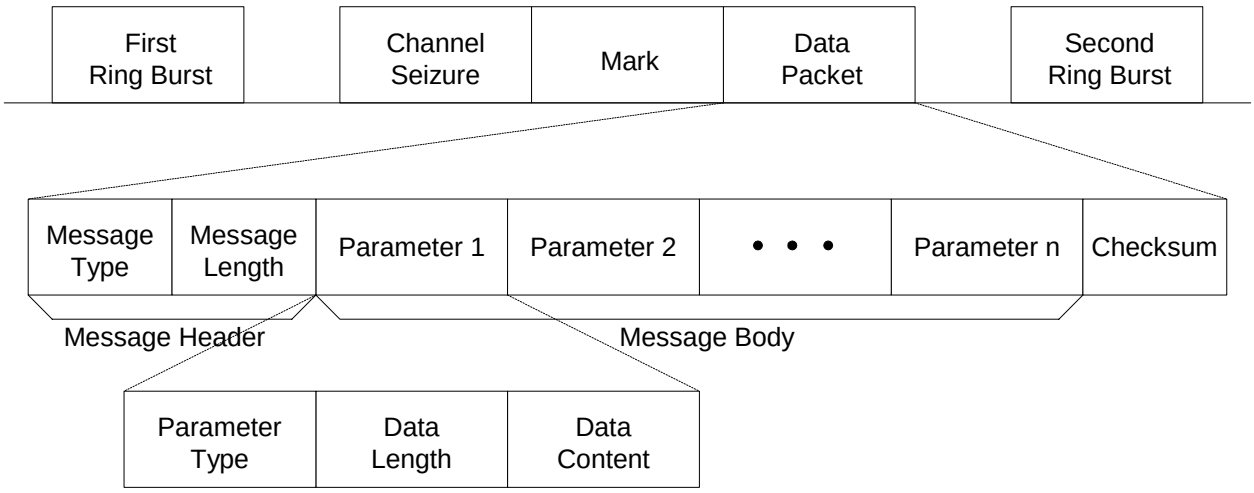


Figure 37. On-Hook Caller ID Transmission Sequence

Tone Generator Interrupts

Both the active and inactive timers can generate an interrupt to signal “on/off” transitions to the software. The timer interrupts for tone generator 1 can be individually enabled by setting the OS1TAE and OS1TIE bits. Timer interrupts for tone generator 2 are OS2TAE and OS2TIE. A pending interrupt for each of the timers is determined by reading the OS1TAS, OS1TIS, OS2TAS, and OS2TIS bits in the IRQVEC1 register.

Caller ID Generation

The Dual ProSLIC devices generate caller ID signals in compliance with various Bellcore and ITU specifications as described in Table 32 by providing continuous phase binary frequency shift key (FSK) modulation. Oscillator 1 is required because it preserves phase continuity during frequency shifts whereas Oscillator 2 does not. Figure 37 illustrates a typical caller ID transmission sequence in accordance with Bellcore requirements.

Table 32. FSK Modulation Requirements

Parameter	ITU-T V.23	Bellcore GR-30-CORE
Mark Frequency (logic 1)	1300 Hz	1200 Hz
Space Frequency (logic 0)	2100 Hz	2200 Hz
Transmission Rate	1200 baud	

Table 33. Register and RAM Locations used for Caller ID Generation

Parameter	Register/RAM Mnemonic	Register/RAM Bits	Description/Range
FSK Start & Stop Bit Enable	OMODE	O1FSK8	Enable/disable
Oscillator 1 Active Timer	O1TALO/O1TAHI	OSC1TA[15:0]	0 to 8.19 s/125 μs
FSK Data Byte	FSKDAT	FSKDAT[7:0]	Caller ID data
FSK Frequency for Space	FSKFREQ0	FSKFREQ0[15:3]	Audio range
FSK Frequency for Mark	FSKFREQ1	FSKFREQ1[15:3]	Audio range
FSK Amplitude for Space	FSKAMP0	FSKAMP0[15:3]	
FSK Amplitude for Mark	FSKAMP1	FSKAMP1[15:3]	
FSK 0-1 Transition Freq, High	FSK01HI	FSK01HI[15:3]	
FSK 0-1 Transition Freq, Low	FSK01LO	FSK01LO[15:3]	
FSK 1-0 Transition Freq, High	FSK10HI	FSK10HI[15:3]	
FSK 1-0 Transition Freq, Low	FSK10LO	FSK10LO[15:3]	

The register and RAM locations for caller ID generation are listed in Table 33. Caller ID data is entered into the 8-bit FSKDAT register. The data byte is double buffered so that the Dual ProSLIC can generate an interrupt indicating the next data byte can be written when processing begins on the current data byte. The caller ID data can be transmitted in one of two modes controlled by the O1FSK8 register bit. When O1FSK8 = 0 (default case), the 8-bit caller ID data is transmitted with a start bit and stop bit to create a 10-bit data sequence. If O1FSK8 = 1, the caller ID data is transmitted as a raw 8-bit sequence with no start or stop bits. The value programmed into the OSC1TA register determines the bit rate, and the interrupt rate is equal to the bit rate divided by the data sequence length (8 or 10 bits).

Pulse Metering Generation

The Si3220 offers an additional tone generator to generate tones above the audio frequency band. This oscillator generates billing tones which are typically 12 kHz or 16 kHz. The generator follows the same algorithm as described in "Tone Generator Architecture" on page 53 with the exception that the sample rate for computation is 64 kHz instead of 8 kHz. The equation is as follows:

$$\text{Coeff} = \cos(2\pi f / 64000\ \text{Hz})$$

$$\text{PMFREQ} = \text{coeff} \times (2^{14} - 1)$$

$$PMAMPL = \frac{1}{4}\sqrt{\frac{1-coeff}{1+coeff}} \times (2^{15}-1) \times \frac{DesiredV_{PK}}{FullScaleV_{PK}}$$

where Full Scale V_{PK} = 0.5 V.

The pulse metering oscillator has a volume envelope (linear ramp) on the on/off transitions of the oscillator. The ramp is controlled by the value in the PMRAMP RAM address, and the sinusoidal generator output is multiplied by this volume before it is sent to the Pulse Metering DAC. The volume value is incremented by the value in PMRAMP at an 8 kHz rate. The volume will ramp from 0 to 7FFF in increments of PMRAMP to allow the value of PMRAMP to set the slope of the ramp. The clip detector stops the ramp once the signal seen at the transmit path exceeds the amplitude threshold set by PMAMPTH, which provides an automatic gain control (AGC) function to prevent the audio signal from clipping. When the pulse metering signal is turned off, the volume ramps down to 0 by decrementing according to the value of PMRAMP. Figure 38 illustrates the functional blocks involved in pulse metering generation, and Table 34 presents the register and RAM locations required that must be set to generate pulse metering signals.

Table 34. Register and RAM Locations Used for Pulse Metering Generation

Parameter	Register/RAM Mnemonic	Register/RAM Bits	Description/Range (LSB Size)
Pulse Metering Frequency Coefficient	PMFREQ	PMFREQ[15:3]	Sets oscillator frequency
Pulse Metering Amplitude Coefficient	PMAMPL	PMAMPL[15:0]	Sets oscillator amplitude
Pulse Metering Attack/Decay Ramp Rate	PMRAMP	PMRAMP[15:0]	0 to PMAMPL (full amplitude)
Pulse Metering Active Timer	PMTALO/PMTAHI	PULSETA[15:0]	0 to 8.19 s (125 µs)
Pulse Metering Inactive Timer	PMTILO/PMTIHI	PULSETI[15:0]	0 to 8.19 s (125 µs)
Pulse Metering, Control Interrupt	IRQVEC1, IRQEN1	PULSTAE, PULSTIE, PULSTAS, PULSTIS	Interrupt Status and control registers
Pulse Metering AGC Amplitude Threshold	PMAMPTH	PMAMPTH[15:0]	0 to 500 mV
PM Waveform Present	PMCON	ENSYNC	Indicates signal present
PM Active Timer Enable	PMCON	TAEN	Enable/disable
PM Inactive Timer Enable	PMCON	TIEN	Enable/disable
Pulse Metering Enable	PMCON	PULSE1	Enable/disable

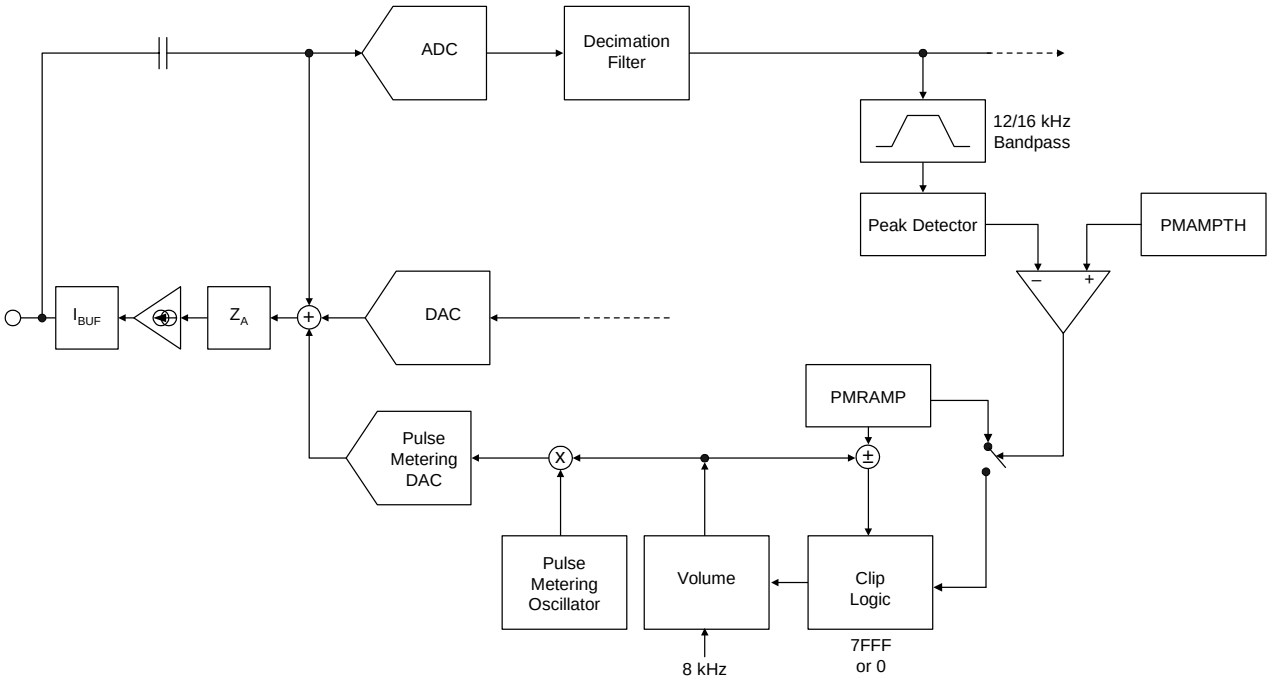


Figure 38. Pulse Metering Generation Block Diagram

DTMF Detection

On-chip DTMF detection, also known as Touch Tone, is available in the Si3220 and Si3225.

It is an in-band signaling system that replaces the pulse-dial signaling standard. In DTMF, two tones generate a DTMF digit. One tone is chosen from the four possible row tones and one tone is chosen from the four possible column tones. The sum of these tones constitute one of 16 possible DTMF digits. The row and column tones and corresponding digits are shown in Table 35.

DTMF detection is performed using a modified Goertzel algorithm to compute the DFT for each of the eight DTMF frequencies and their second harmonics. At the end of the DFT computation, the squared magnitudes of the DFT results for the 8 DTMF fundamental tones are computed. The row results are sorted to determine the strongest row frequency, and the column frequencies are sorted as well. At the completion of this process, checks are made to determine if the strongest row and column tones constitute a DTMF digit.

The detection process occurs twice within the 45 ms minimum tone time. A digit must be detected on two consecutive tests after a pause to be recognized as a new digit. If all tests pass, an interrupt is generated and the DTMF digit value is loaded into the DTMF register according to the following table. If tones occur at the maximum rate of 100 ms per digit, the interrupt must be serviced within 85 ms so that the current digit is not overwritten by a new one. There is no buffering of the digit information.

Table 35. DTMF Row/Column Tones

697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D
	1209 Hz	1336 Hz	1477 Hz	1633 Hz

Table 36 outlines the hex code corresponding to the detected DTMF digits.

Table 36. DTMF Hex Codes

Digit	Hex code
1	0x1
2	0x2
3	0x3
4	0x4
5	0x5
6	0x6
7	0x7
8	0x8
9	0x9
0	0xA
*	0xB
#	0xC
A	0xD
B	0xE
C	0xF
D	0x0

Modem Tone Detection

The Dual ProSLIC devices are capable of detecting a 2100 Hz modem tone as described in ITU-T Recommendation V.8. The detection scheme can be implemented in both transmit and receive paths, and is enabled by programming the appropriate register bit. The detection scheme should be disabled for power conservation after the modem tone window has passed. Once a valid modem tone is detected, a register bit will be set accordingly and the user can check the results by reading the register value. A programmable debounce interval is provided to eliminate false detection and can be programmed in increments of 67 ms by writing to the appropriate register.

Audio Path Processing

Unlike traditional SLICs, the Dual ProSLIC devices integrate the codec function into the same IC. The on-chip 16-bit codec offers programmable gain/attenuation blocks and multiple loopback modes for self testing. The signal path block diagram is shown in Figure 11 on page 22.

Transmit Path

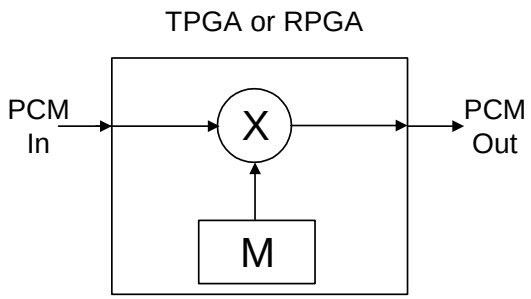
In the transmit path, the analog signal fed by the external ac coupling capacitors is passed through an anti-aliasing filter before being processed by the A/D converter. An analog mute function is provided directly prior to the A/D converter input. The output of the A/D converter is an 8 kHz, 16-bit wide, linear PCM data stream. The standard requirements for transmit path attenuation for signals above 3.4 kHz are part of the combined decimation filter characteristic of the A/D converter. One more digital filter is available in the transmit path, THPF. THPF implements the high-pass attenuation requirements for signals below 65 Hz. An equalizer block then equalizes the transmit signal path to compensate for series protection resistance (R_{PROT}) outside of the ac-sensing inputs. The linear PCM data stream output from the equalizer block is amplified by the transmit-path programmable gain amplifier, TPGA, which can be programmed from –∞ to 6 dB. The DTMF decoder receives the linear PCM data stream and performs the digit extraction if enabled by the user. The final step in the transmit path signal processing is the A-law or μ-law compression which can reduce the data stream word width to 8 bits. Depending on the PCM Mode Select register selection, every 8-bit compressed serial data word occupies one time slot on the PCM highway, or every 16-bit uncompressed serial data word occupies two time slots on the PCM highway.

Receive Path

In the receive path, the optionally compressed 8-bit data is first expanded to 16-bit words. The PCMF register bit can bypass the expansion process, so that two 8-bit words are assembled into one 16-bit word. RPGA is the receive path programmable gain amplifier which can be programmed from –∞ dB to 6 dB. An 8 kHz, 16-bit signal is then provided to a D/A converter. An analog mute function is provided directly after the D/A converter. When not muted, the resulting analog signal is applied at the input of the transconductance amplifier, Gm, which drives the off-chip current buffer, I_{BUF}.

TPGA/RPGA Gain/Attenuation Blocks

The TPGA and RPGA blocks are essentially linear multipliers with the structure illustrated in Figure 39. Both blocks can be independently programmed from –∞ to +6 dB (0 to 2 linear scale). The TXGAIN and RXGAIN RAM locations are used to program each block. A setting of 0000h will mute all audio signals; a setting of 4000h will pass the audio signal with no gain or attenuation (0 dB), and a setting of 7FFFh will provide the maximum 6 dB of gain to the incoming audio signal. The DTXMUTE and DRXMUTE bits in the DIGCON register are also available in order to allow muting of the transmit and receive paths without requiring modifications to the TXGAIN or RXGAIN settings.



where M = {0, 1/16384, 2/16384,...32767/16384}

Figure 39. TPGA and RPGA structure

Audio Characteristics

The dominant source of distortion and noise in both the transmit and receive paths is the quantization noise introduced by the μ-law or the A-law compression process. Figure 5 on page 18 specifies the minimum Signal-to-Noise-and-Distortion Ratio for either path for a sine wave input of 200 Hz to 3400 Hz.

Both the μ-law and the A-law speech encoding allow the audio codec to transfer and process audio signals larger than 0 dBm0 without clipping. The maximum PCM code is generated for a μ-law encoded sine wave of 3.17 dBm0 or an A-law encoded sine wave of 3.14 dBm0. The device overload clipping limits are driven by the PCM encoding process. Figure 6 on page 19 shows the acceptable limits for the analog-to-analog fundamental power transfer-function, which bounds the behavior of the device.

The transmit path gain distortion versus frequency is shown in Figure 7 on page 19. The same figure also presents the minimum required attenuation for out-of-band analog signals applied on the line. The presence of a high-pass filter transfer-function ensures at least 30 dB of attenuation for signals below 65 Hz. The low-pass filter transfer function attenuates signals above 3.4 kHz. It is implemented as part of the A-to-D converter.

The receive path transfer function requirement, shown in Figure 8 on page 20, is very similar to the transmit path transfer function. The PCM data rate is 8 kHz so no frequencies greater than 4 kHz are digitally encoded in the data stream. At frequencies greater than 4 kHz, the plot in Figure 8 is interpreted as the maximum allowable magnitude of spurious signals that are generated when a PCM data stream representing a sine wave signal in the range of 300 Hz to 3.4 kHz at a level of 0 dBm0 is applied at the digital input.

The group delay distortion in either path is limited to no more than the levels indicated in Figure 9. The reference in Figure 9 is the smallest group delay for a sine wave in the range of 500 Hz to 2500 Hz at 0 dBm0.

The block diagram for the voice-band signal processing paths are shown in Figure 11 on page 22. Both the receive and the transmit paths employ the optimal combination of analog and digital signal processing for maximum performance while maintaining sufficient flexibility for users to optimize their particular application of the device. The two-wire (TIP/RING) voice-band interface to the device is implemented with a small number of external components. The receive path interface consists of a unity-gain current buffer, I_{BUF}, while the transmit path interface is an ac coupling capacitor. Signal paths, although implemented differentially, are shown as single-ended for simplicity.

System Clock Generation

The Dual ProSLIC devices generate the internal clock frequencies from the PCLK input. PCLK must be synchronous to the 8 kHz FSYNC clock and run at one of the following rates: 256 kHz, 512 kHz, 786 kHz, 1.024 MHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, 4.096 MHz or 8.192 MHz. The ratio of the PCLK rate to the FSYNC rate is determined by a counter clocked by PCLK. The three-bit ratio information is transferred into an internal register, PLL_MULT, after a device reset. The PLL_MULT controls the internal PLL which multiplies PCLK to generate the rate required to run the internal filters and other circuitry.

The PLL clock synthesizer settles quickly after powerup or update of the PLL_MULT register. However, the settling time depends on the PCLK frequency and it is approximately predicted by the following equation:

$T_{settle} = 64/F_{PCLK}$

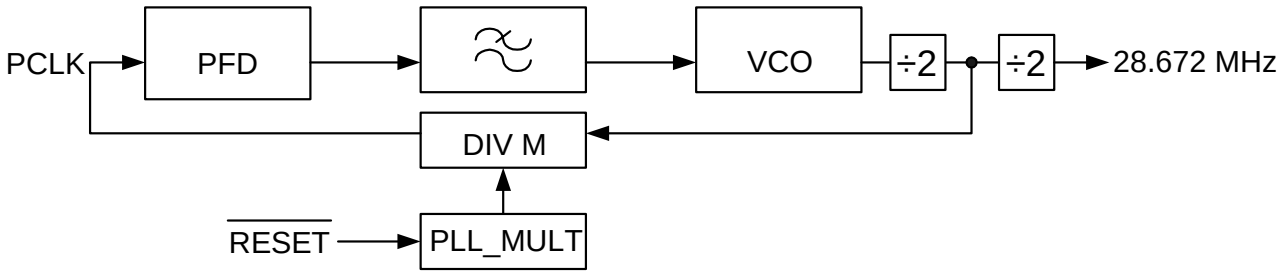


Figure 40. PLL Frequency Synthesizer

Interrupt Logic

The Dual ProSLIC devices are capable of generating interrupts for the following events:

- Loop current/ring ground detected.
- Ring trip detected.
- Ground Key detected.
- Power alarm.
- DTMF digit detected.
- Active timer 1 expired.
- Inactive timer 1 expired.
- Active timer 2 expired.
- Inactive timer 2 expired.
- Ringing active timer expired.
- Ringing inactive timer expired.
- Pulse metering active timer expired.
- Pulse metering inactive timer expired.
- RAM address access complete.
- Receive path modem tone detected.
- Transmit path modem tone detected.

The interface to the interrupt logic consists of six registers. Three interrupt status registers (IRQ0–IRQ3) contain 1 bit for each of the above interrupt functions. These bits are set when an interrupt is pending for the associated resource. Three interrupt mask registers (IRQEN1–IRQEN3) also contain 1 bit for each interrupt function. For interrupt mask registers, the bits are active high. Refer to the appropriate functional description text for operational details of the interrupt functions.

When a resource reaches an interrupt condition, it signals an interrupt to the interrupt control block. The interrupt control block sets the associated bit in the interrupt status register if the mask bit for that interrupt is set. The INT pin is a NOR of the bits of the interrupt status registers. Therefore, if a bit in the interrupt status registers is asserted, IRQ asserts low. Upon receiving the interrupt, the interrupt handler should read interrupt status registers to determine which resource requests service. All interrupt bits in the interrupt status registers IRQ0–IRQ3 are cleared following a register read operation. If the interrupt status registers are non-0, the INT pin remains asserted.

SPI Control Interface

The control interface to the Dual ProSLIC devices is a 4-wire interface modeled after micro-controller and serial peripheral devices. The interface consists of a clock (SCLK), chip select (CS), serial data input (SDI), and serial data output (SDO). In addition, the Dual ProSLIC devices include a serial data through output (SDI_THRU) to support a daisy-chain operation of up to eight devices (up to sixteen channels). The device operates with both 8-bit and 16-bit SPI controllers. Each SPI operation consists of a control byte, an address byte (of which only the seven LSBs are used internally), and either one or two data bytes depending on the width of the controller and whether the access is to an 8-bit register or 16-bit RAM address. Bytes are always transmitted MSB first.

There are variations of usage on this four-wire interface as follows:

- **Continuous clocking**. During continuous clocking, the data transfers are controlled by the assertion of the CS pin. CS must be asserted before the falling edge of SCLK on which the first bit of data is expected during a read cycle, and must remain low for the duration of the 8-bit transfer (command/ address or data), going high after the last rising of SCLK after the transfer.
- **Clock during transfer only**. In this mode, only the clock is cycling during the actual byte transfers. Each byte transfer will consist of eight clock cycles in a return to “1” format.
- **SDI/SDO wired operation**. Independent of the clocking options described, SDI and SDO can be treated as two separate lines or wired together if the master is capable of tri-stating its output during the data byte transfer of a read operation.
- **Soft reset**. The SPI state machine resets whenever CS asserts during an operation on an SCLK cycle that is not a multiple of eight. This is a mechanism for the controller to force the state machine to a known state when the controller and the device are out of synchronization.

The control byte has the following structure and is presented on the SDI pin MSB first.

7	6	5	4	3	2	1	0
BRDCST	R/W	REG/RAM	Reserved	CID[0]	CID[1]	CID[2]	CID[3]

The bits are defined as follows:

Table 37. SPI Control Interface

7	BRDCST	Indicates a broadcast operation that is intended for all devices in the daisy chain. This is only valid for write operations, since it would cause contention on the SDO pin during a read.
6	R/W	**Read/Write Bit.** 0 = Write operation. 1 = Read operation.
5	REG/RAM	**Register/RAM Access Bit.** 0 = RAM access. 1 = Register access.
4	Reserved	
3:0	CID[3:0]	Indicates the channel that is targeted by the operation. The 4-bit channel value is provided LSB first. The devices reside on the daisy chain such that device 0 is nearest to the controller and device 15 is furthest down the SDI/SDU_THRU chain. (See Figure 41.) As the CID information propagates down the daisy chain, each channel decrements the CID by 1. The SDI nodes between devices reflects a decrement of 2 per device since each device contains two channels. The device receiving a value of 0 in the CID field responds to the SPI transaction. (See Figure 42.) If a broadcast to all devices connected to the chain is requested, the CID does not decrement. In this case, the same 8-bit or 16-bit data is presented to all channels regardless of the CID values.

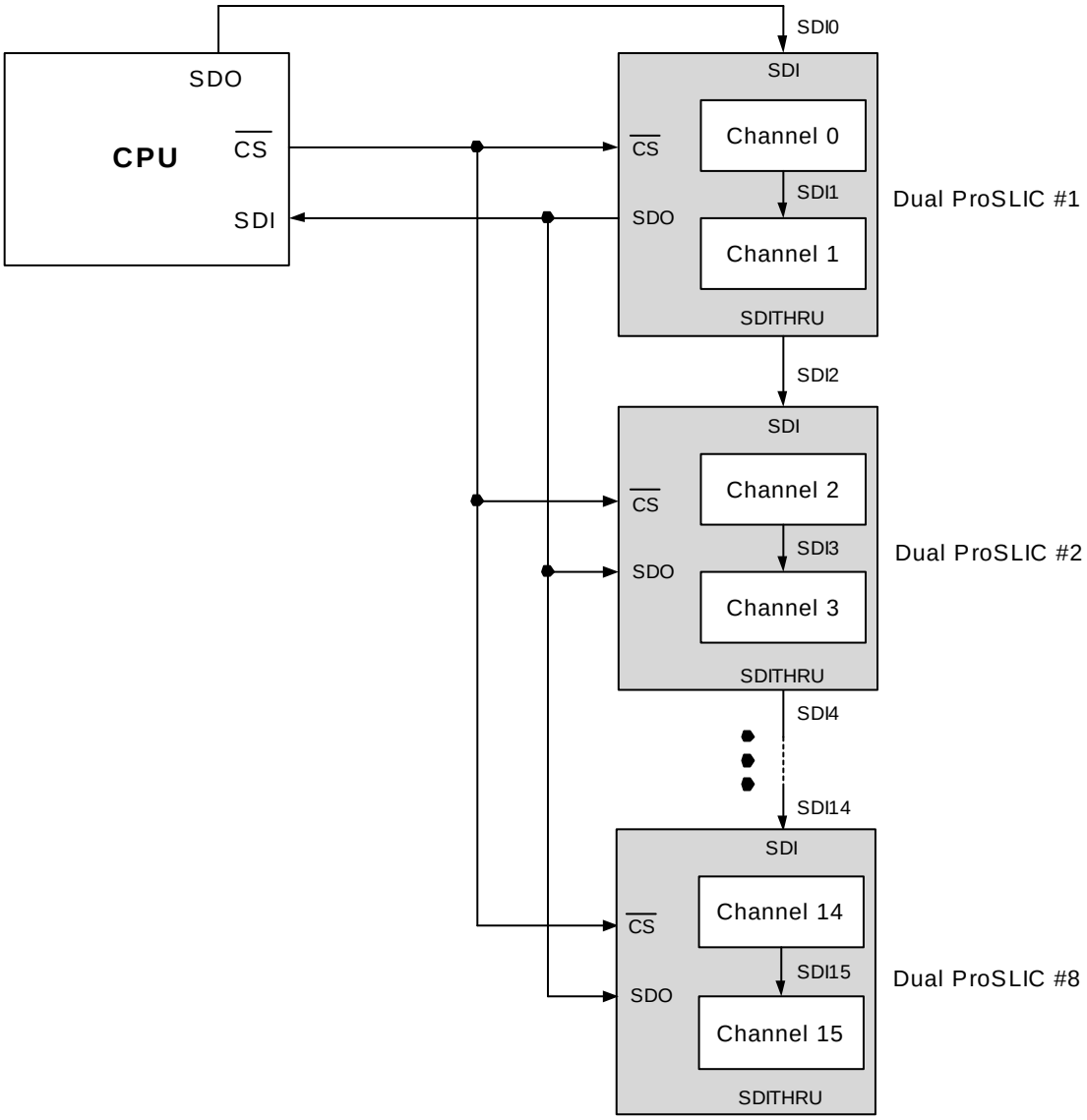


Figure 41. SPI Daisy-Chain Mode

In Figure 42 the CID field is 0. As this field is decremented (in LSB to MSB order) the value decrements for each SDI down the line. The BRDCST, R/W, and REG/RAM bits remain unchanged as the control word passes through the entire chain. The odd SDIs are internal to the device and represent the SDI to SDI_THRU connection between channels of the same device. A unique CID is presented to each channel, and the channel receiving a CID value of zero is the target of the operation (channel 0 in this case). The last line of Figure 42 illustrates that in Broadcast mode, all bits pass through the chain without permutation.

SPI Control Word

	BRDCST	R/W	REG/RAM	Reserved	CID[0]	CID[1]	CID[2]	CID[3]
SDI0	0	A	B	C	0	0	0	0
SDI1 (Internal)	0	A	B	C	1	1	1	1
SDI2	0	A	B	C	0	1	1	1
SDI3 (Internal)	0	A	B	C	1	0	1	1
				●				
				●				
				●				
SDI 14	0	A	B	C	0	1	0	0
SDI15 (Internal)	0	A	B	C	1	0	0	0
SDI0-15	1	A	B	C	D	E	F	G

Figure 42. Sample SPI Control Word to Address Channel 0

Figures 43 and 44 illustrate WRITE and READ operations to register addresses via an 8-bit SPI controller. These operations are performed as a 3-byte transfer. $\overline{CS}$ is asserted between each byte which is required for $\overline{CS}$ to be asserted before the first falling edge of SCLK after the DATA byte to indicate to the state machine that one byte only should be transferred. The state of SDI is a “don’t care” during the DATA byte of a read operation.

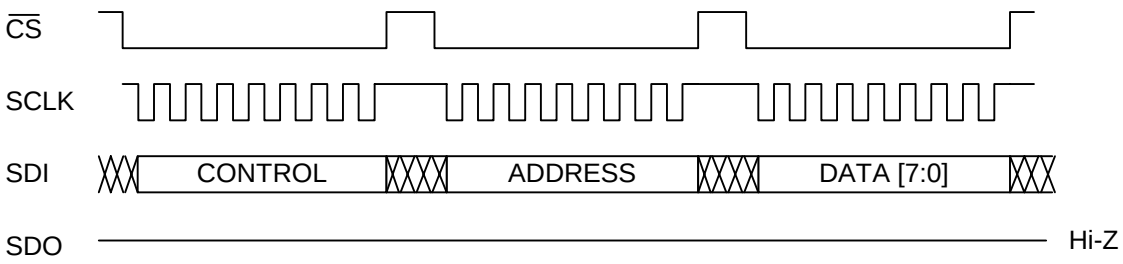


Figure 43. Register Write Operation via an 8-Bit SPI Port

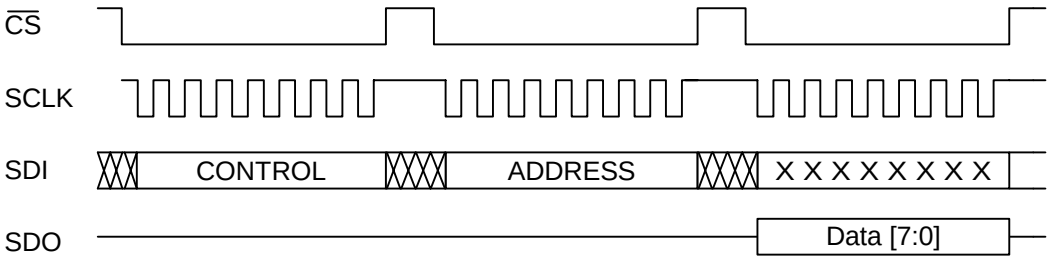


Figure 44. Register Read Operation via an 8-Bit SPI Port

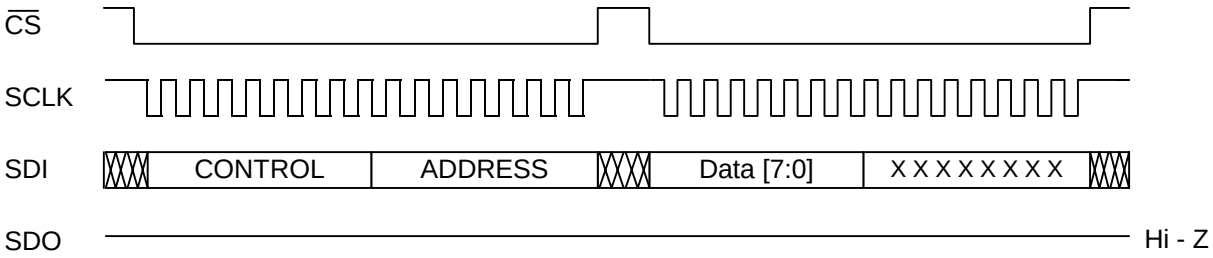


Figure 45. Register Write Operation via a 16-Bit SPI Port

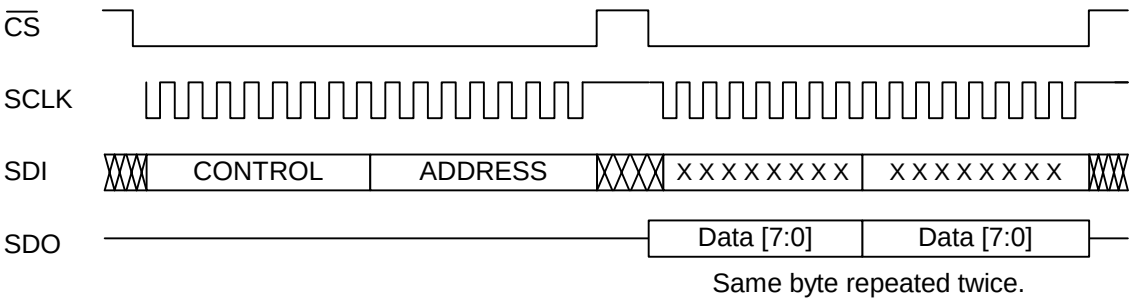


Figure 46. Register Read Operation via a 16-Bit SPI Port

Figures 45 and 46 illustrate WRITE and READ operations to register addresses via a 16-bit SPI controller. These operations require a 4-byte transfer arranged as two 16-bit words. The absence of $\overline{CS}$ going high after the eighth bit of data indicates to the SPI state machine that eight more SCLK pulses follow to complete the operation. For a WRITE operation, the last eight bits are ignored. For a read operation, the 8-bit data value repeats so that the data is captured during the last half of a data transfer if required by the controller.

During register accesses, the CONTROL, ADDRESS, and DATA are captured in the SPI module. At the completion of the ADDRESS byte of a READ access, the contents of the addressed register move into the data register of the SPI data register. At the completion of the DATA byte of a WRITE access, the data is transferred from the SPI to the addressed register.

Figures 47–50 illustrate the various cycles for accessing RAM addresses. RAM addresses are 16-bit entities; therefore, the accesses always require four bytes.

During RAM address accesses, the CONTROL, ADDRESS, and DATA are captured in the SPI module. At the completion of the ADDRESS byte of a READ access, the contents of the channel-based data buffer move into the data register in the SPI for shifting out during the DATA portion of the SPI transfer. This is the data loaded into the data buffer in response to the previous RAM address read request. Therefore, there is a one-deep pipeline nature to RAM address READ operations. At the completion of the DATA portion of the READ cycle, the ADDRESS is transferred to the channel-based address buffer register and a RAM address is logged for that channel. The RAMSTAT bit in each channel is polled to monitor the status of RAM address accesses that are serviced twice per sample period at dedicated windows in the DSP algorithm.

A RAM access interrupt in each channel indicates that the pending RAM access request is serviced. For a RAM access, the ADDRESS and DATA is transferred from the SPI registers to the address and data buffers in the appropriate channel. The RAM WRITE request will be then logged. As for READ operations, the status of the pending request is monitored by either polling the RAMSTAT bit for the channel or enabling the RAM access interrupt for the channel. By keeping the address, data buffers, and RAMSTAT register on a per channel basis, RAM address accesses can be scheduled for both channels without interface.

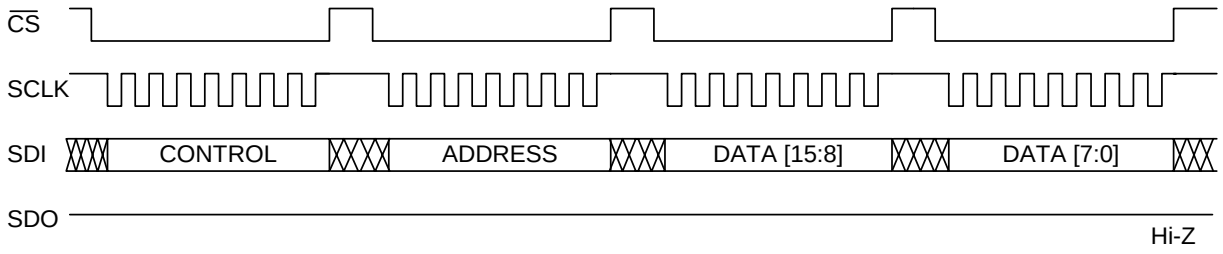


Figure 47. RAM Write Operation via an 8-Bit SPI Port

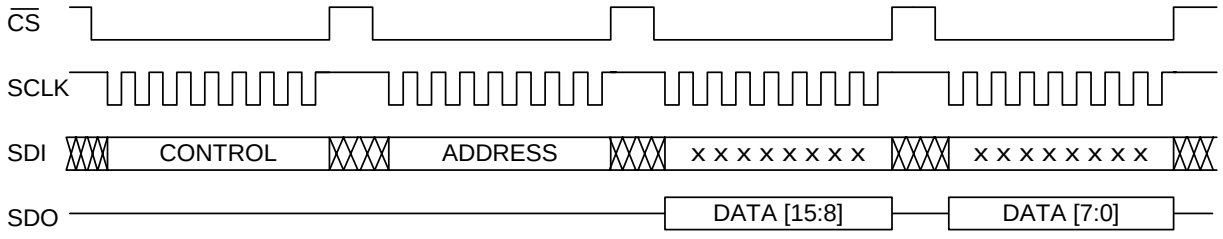


Figure 48. RAM Read Operation via an 8-Bit SPI Port

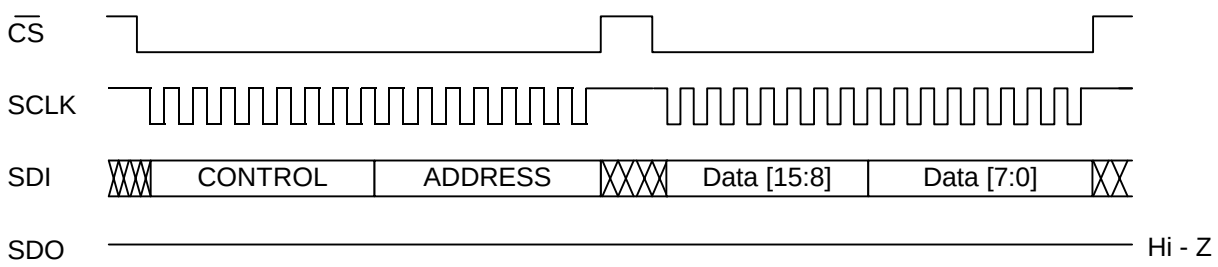


Figure 49. RAM Write Operation via a 16-Bit SPI Port

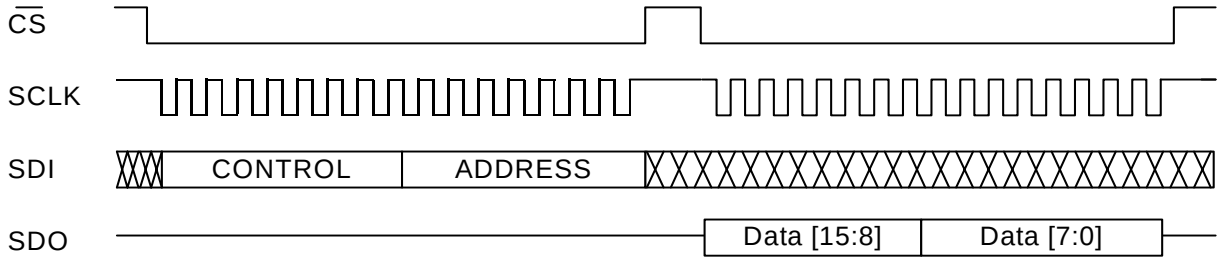


Figure 50. RAM Read Operation via a 16-Bit SPI Port

PCM Interface

The Dual ProSLIC devices contain a flexible programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled by the PCLK and FSYNC inputs, PCM Mode Select, PCM Transmit Start Count (PCMTXHI/PCMTXLO), and PCM Receive Start Count (PCMRXHI/PCMRXLO) registers. The interface can be configured to support from 4 to 128 8-bit timeslots in each frame. This corresponds to PCLK frequencies of 256 kHz to 8.192 MHz in power of 2 increments. (768 kHz, 1.536 MHz and 1.544 MHz also are available.) Timeslots for data transmission and reception are independently configured with the PCMTXHI, PCMTXLO, PCMRXHI, and PCMRXLO. Setting the correct starting point of the data configures the part to support long FSYNC and short FSYNC variants, IDL2 8-bit, 10-bit, B1 and B2 channel time slots. DTX data is high-impedance except for the duration of the 8-bit PCM transmit. DTX returns to high-impedance on the negative edge of PCLK during the LSB or on the positive edge of PCLK following the LSB. This is based on the setting of the PCMTRI bit of the PCM Mode Select register. Tristating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots without the risk of driver contention. In addition to 8-bit data modes, there is a 16-bit mode provided for testing. This mode can be activated via the PCMF bits of the PCM Mode Select register. Setting the PCMTXHI/PCMTXLO or PCMRXHI/PCMRXLO register greater than the number of PCLK cycles in a sample period stops data transmission because PCMTXHI/PCMTXLO or PCMRXHI/PCMRXLO do not equal the PCLK count. Figures 51–53 illustrate the usage of the PCM highway interface to adapt to common PCM standards.

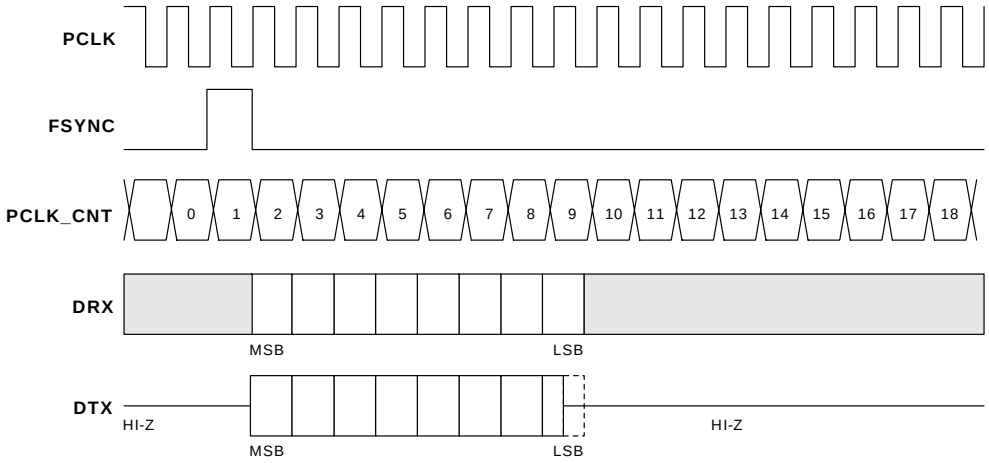


Figure 51. Example, Timeslot 1, Short FSYNC (TXS/RXS = 1)

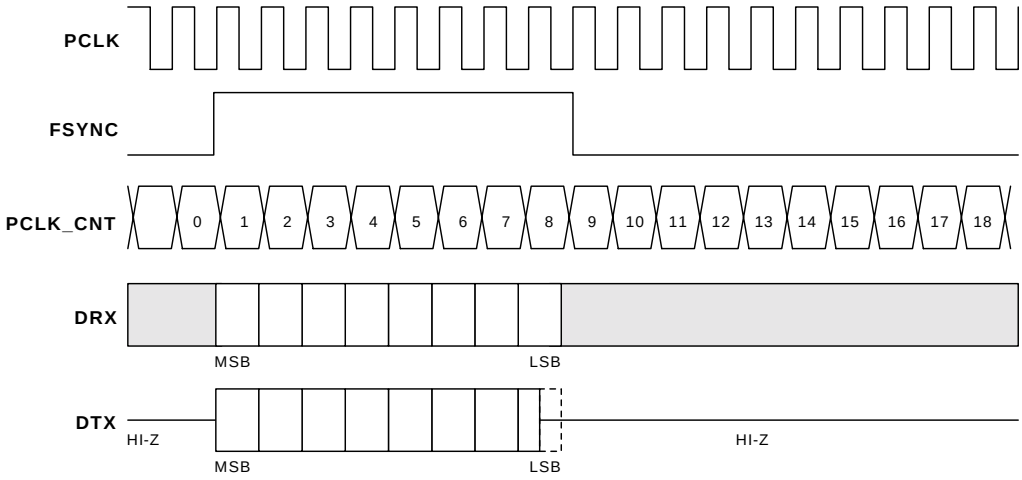


Figure 52. Example, Timeslot 1, Long FSYNC (TXS/RXS = 0)

PCM Companding

The Dual ProSLIC devices support both µ-255 Law (µ-Law) and A-Law companding formats in addition to Linear Data mode. The data format is selected via the PCMF bits of the PCM Mode Select register. µ-Law mode is more commonly used in North America and Japan, and A-Law is primarily used in Europe and other countries. These 8-bit companding schemes follow a segmented curve formatted as a sign bit (MSB) followed by three chord bits and four step bits. A-Law typically uses a scheme of inverting all even bits while µ-Law does not. Dual ProSLIC devices also support A-Law with inversion of even bits, inversion of all bits, or no bit inversion by programming the ALAW bits of the PCM Mode Select register to the appropriate setting. Tables 38 and 39 define the µ-Law and A-Law encoding formats.

The Dual ProSLIC devices also support a 16-bit linear data format with no companding. This Linear mode is typically used in systems that convert to another companding format such as adaptive delta PCM (ADPCM) or systems that perform all companding in an external DSP. The data format is 2's complement with MSB first (sign bit). Transmitting and receiving data via Linear mode requires two continuous time slots. An 8-bit Linear mode enables 8-bit transmission without companding.

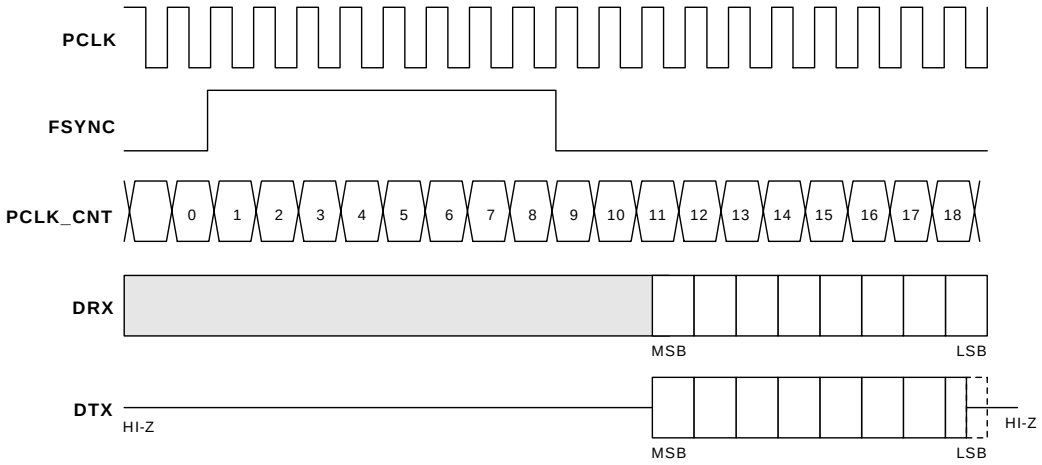


Figure 53. Example, IDL2 Long FSYNC, B2, 10-Bit Mode (TXS/RXS = 10)

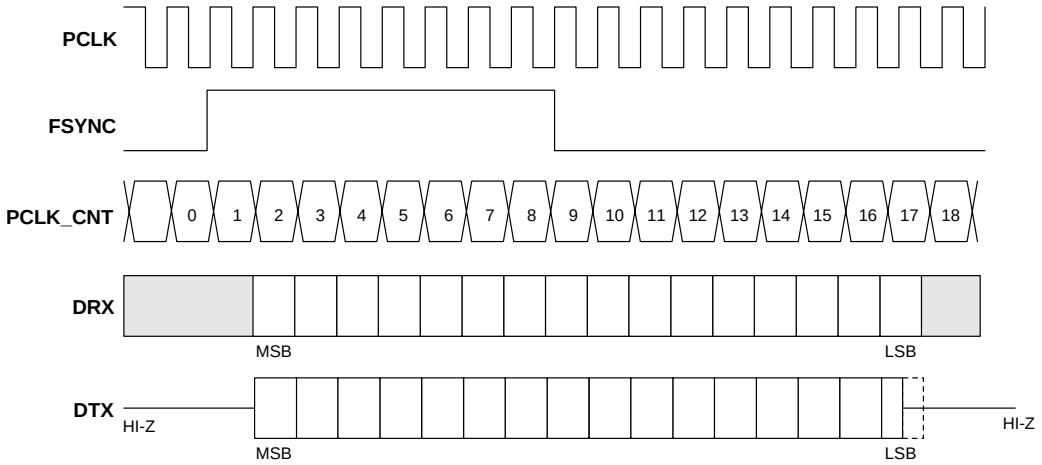


Figure 54. 16-Bit Linear Mode Example, Timeslots 1 and 2, Long FSYNC

Table 38. μ-Law Encode-Decode Characteristics*

Segment Number	#Intervals X Interval Size	Value at Segment Endpoints	Digital Code	Decode Level
8	16 X 256	8159 . . . 4319 4063	10000000b 10001111b	8031 4191
7	16 X 128	. . . 2143 2015	 10011111b	 2079
6	16 X 64	. . . 1055 991	 10101111b	 1023
5	16 X 32	. . . 511 479	 10111111b	 495
4	16 X 16	. . . 239 223	 11001111b	 231
3	16 X 8	. . . 103 95	 11011111b	 99
2	16 X 4	. . . 35 31	 11101111b	 33
1	15 X 2 1 X 1	. . . 3 1 0	 11111110b 11111111b	 2 0
***Note:** Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.				

Table 39. A-Law Encode-Decode Characteristics[1,2]

Segment Number	#intervals X interval size	Value at segment endpoints	Digital Code	Decode Level
7	16 X 128	4096 3968 . . 2176 2048	 10101010b 10100101b	 4032 2112
6	16 X 64	. . . 1088 1024	 10110101b	 1056
5	16 X 32	. . . 544 512	 10000101b	 528
4	16 X 16	. . . 272 256	 10010101b	 264
3	16 X 8	. . . 136 128	 11100101b	 132
2	16 X 4	. . . 68 64	 11110101b	 66
1	32 X 2	. . . 2 0	 11010101b	 1

Notes:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative values.
2. Digital code includes inversion of even numbered bits. Other available formats include inversion of odd bits, inversion of all bits, or no bit inversion. See "PCM Companding" on page 70 for more details.

General Circuit Interface

The Dual ProSLIC devices also contain an alternate communication interface to the SPI and PCM control and data interface. The general circuit interface (GCI) is used for the transmission and reception of both control and data information onto a GCI bus. The PCM and GCI interfaces are both four-wire interfaces and share the same pins. The SPI control interface is not used as a communication interface in the GCI mode, but rather as hard-wired channel selector pins. The selection between PCM and GCI modes is performed out of reset using the SDITHRU pin. Tables 40 and 41 illustrate how to select the communication mode and how the pins are used in each mode.

Table 40. PCM or GCI Mode Selection

SDITHRU	SCLK	Mode Selected
0	0	GCI Mode—1x PCLK (2.048 MHz)
0	1	GCI Mode—2x PCLK (4.096 MHz)
1	x	PCM Mode

Note: Values shown are the states of the pins at the rising edge of $\overline{\text{RESET}}$.

Table 41. Pin Functionality in PCM or GCI Mode

Pin Name	PCM Mode	GCI Mode
$\overline{\text{CS}}$	SPI Chip Select	Channel Selector, bit 0
SCLK	SPI Clock Input	PCLK Rate Selector
SDI	SPI Serial Data Input	Channel Selector, bit 2
SDO	SPI Serial Data Output	Channel Selector, bit 1
SDITHRU	SPI Data Through-put pin for Daisy Chaining Operation (Connects to the SDI pin of the subse-quent device in the daisy chain)	PCM/GCI Mode Selector
FSYNC	PCM Frame Sync Input	GCI Frame Sync Input
PCLK	PCM Input Clock	GCI Input Clock
DTX	PCM Data Transmit	GCI Data Transmit
DRX	PCM Data Receive	GCI Data Receive

Note: This table denotes pin functionality after the rising edge of $\overline{\text{RESET}}$ and mode selection.

If GCI mode is selected, the following pins must be tied to the correct state to select one of eight sub-frame timeslots in the GCI frame (described below). These pins must remain in this state while the Dual ProSLIC is operating. Selecting a particular subframe causes that individual Dual ProSLIC device to transmit and receive on the appropriate sub-frame in the GCI frame, which is initiated by an FSYNC pulse. No further register settings are needed to select which sub-frame a device uses, and the sub-frame for a particular device cannot be changed while in operation.

Table 42. GCI Mode Sub-Frame Selection

	SDI	SDO	$\overline{\text{CS}}$
GCI Subframe 0 Selected (Voice channels 1–2)	1	1	1
GCI Subframe 1 Selected (Voice channels 3–4)	1	1	0
GCI Subframe 2 Selected (Voice channels 5–6)	1	0	1
GCI Subframe 3 Selected (Voice channels 7–8)	1	0	0
GCI Subframe 4 Selected (Voice channels 9–10)	0	1	1
GCI Subframe 5 Selected (Voice channels 11–12)	0	1	0
GCI Subframe 6 Selected (Voice channels 13–14)	0	0	1
GCI Subframe 7 Selected (Voice channels 15–16)	0	0	0

In GCI mode, the PCLK input requires either a 2.048 MHz or a 4.096 MHz clock signal, and the FSYNC input requires an 8 kHz frame sync signal. The overall unit of data used to communicate on the GCI highway is a frame 125 μs in length. Each frame is initiated by a pulse on the FSYNC pin, whose rising edge signifies the beginning of the next frame. In 2x PCLK mode, the user sees twice as many PCLK cycles during each 125 μs frame versus 1x PCLK mode. Each frame consists of eight fixed timeslot sub-frames, which are assigned by the Sub-Frame Select pins as described above (SDI, SDO, and $\overline{\text{CS}}$). Within each sub-frame are four channels (bytes) of data, including two voice data channels B1 and B2, one Monitor channel M used for initialization and setup of the device, and one Signaling and Control channel (SC) used for communicating status of the device and for initiating commands. Within the SC channel are six Command/

Indicate (C/I) bits and two handshaking bits, MR and MX. The C/I bits indicate status and command communication, while the handshaking bits Monitor Receive (MR) and Monitor Transmit (MX), exchange data in the Monitor channel. Figure 55 illustrates the contents of a GCI highway frame.

16-Bit GCI Mode

In addition to the standard 8-bit GCI mode, the Dual ProSLIC devices also offer a 16-bit GCI mode for passing 16-bit voice data to the upstream host processor. This mode can be used for testing purposes or for passing non-companded voice data to an upstream DSP for further processing.

In 16-bit GCI mode, both of the 8-bit voice data channels (B1 and B2, Figure 56) of each sub-frame are required to pass the 16-bit voice data to the host. Each 125 μs frame can therefore accommodate up to eight voice channels (the Dual ProSLIC can accommodate up to sixteen voice channels in 8-bit GCI mode). Table 43 describes the GCI mode sub-frame selection for 16-bit GCI mode.

Table 43. Sub-Frame Selection 16-Bit GCI Mode

	SDI	SDO
GCI Subframe 0 Selected (Voice channels 0–1)	1	1
GCI Subframe 1 Selected (Voice channels 2–3)	1	0
GCI Subframe 2 Selected (Voice channels 4–5)	0	1
GCI Subframe 3 Selected (Voice channels 6–7)	0	0

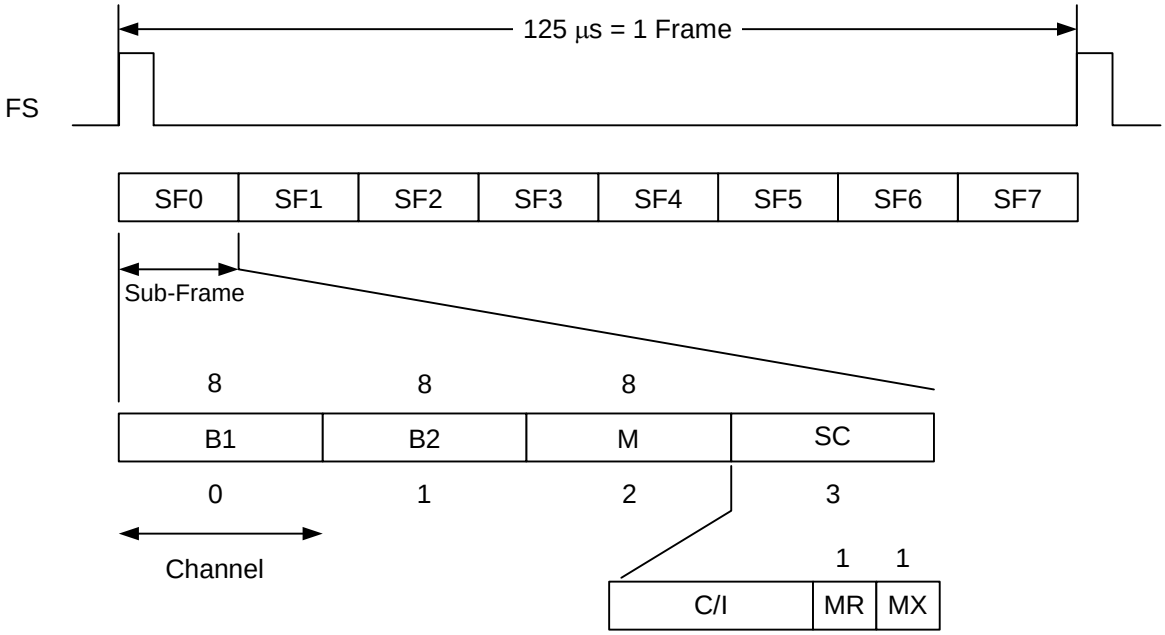


Figure 55. Time-Multiplexed GCI Highway Frame Structure

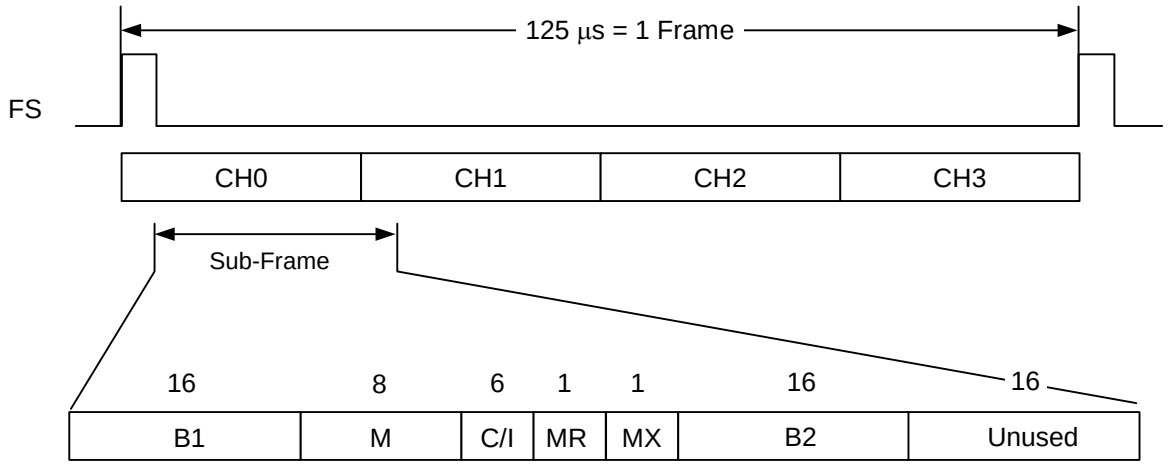


Figure 56. GCI Highway Frame Structure for 16-Bit GCI Mode

Monitor Channel

The Monitor channel is used for initialization and setup of the Dual ProSLIC devices. It is also for general communication with the Dual ProSLIC by allowing read and write access to the Dual ProSLIC devices registers. Use of the monitor channel requires manipulation of the MR and MX handshaking bits, located in bits 1 and 0 of the SC channel described. For purposes of this specification, “downstream” is identified as the data sent by a host to the Dual ProSLIC. “Upstream” is identified as the data sent by the Dual ProSLIC devices to a host.

The following diagram illustrates the Monitor channel communication protocol. For successful communication with the Dual ProSLIC, the transmitter should anticipate the falling edge of the receiver’s acknowledgement. This also maximizes communication speed. Because of the handshaking protocol required for successful communication, the data transfer rate using the Monitor channel is less than 8 kbps.

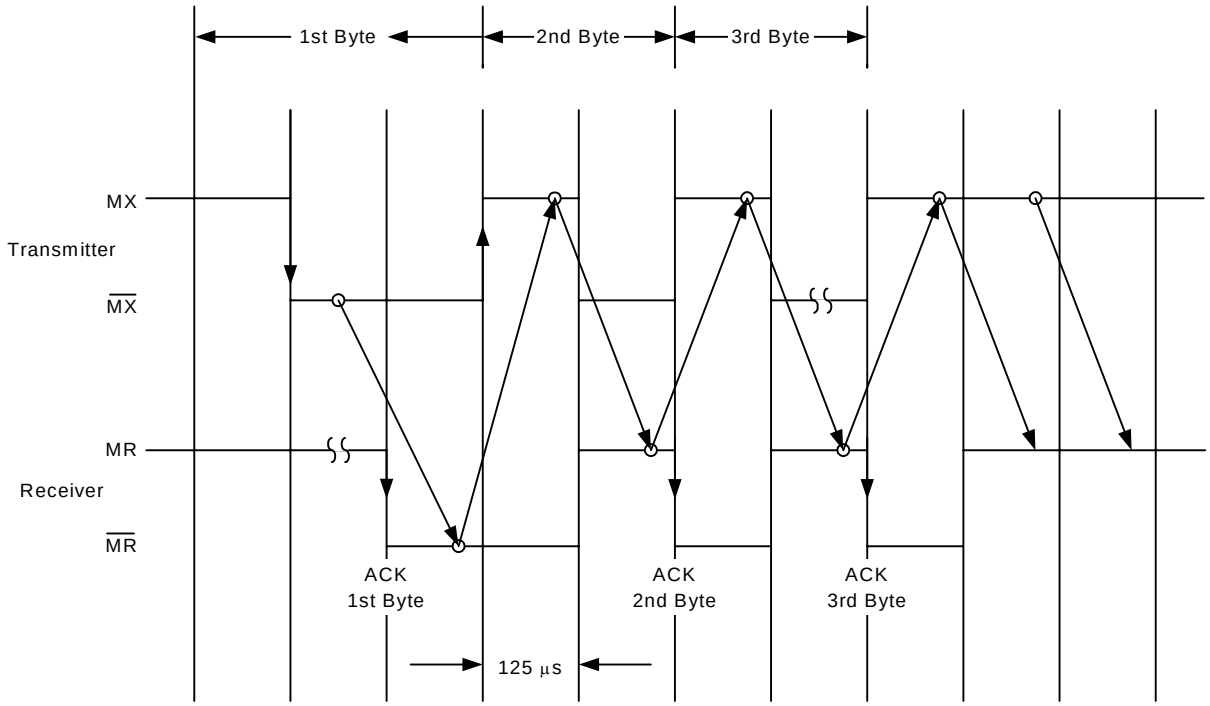


Figure 57. Monitor Handshake Timing

The Idle state is achieved by the MX and MR bits being held inactive for two or more frames. When a transmission is initiated by a host device, an active state is seen on the downstream MX bit. This signals the Dual ProSLIC that a transmission has begun on the Monitor channel and it should begin accepting data from it. The Dual ProSLIC, after reading the data on the Monitor channel, acknowledges the initial transmission by placing the upstream MR bit in an active state. The data is received and the upstream MR becomes active in the frame immediately following the downstream MX becoming active. The upstream MR then remains active until either the next byte is received or an end of message is detected (signaled by the downstream MX being held inactive for two or more consecutive frames). Upon receiving acknowledgement from the Dual ProSLIC that the initial data was received (signaled by the upstream MR bit transitioning from an inactive to an active state), the host device places the downstream MX bit in the inactive state for one frame and then either transmit another byte by placing the downstream MX bit in an active state again, or signal an end of message by leaving the downstream MX bit inactive for a second frame.

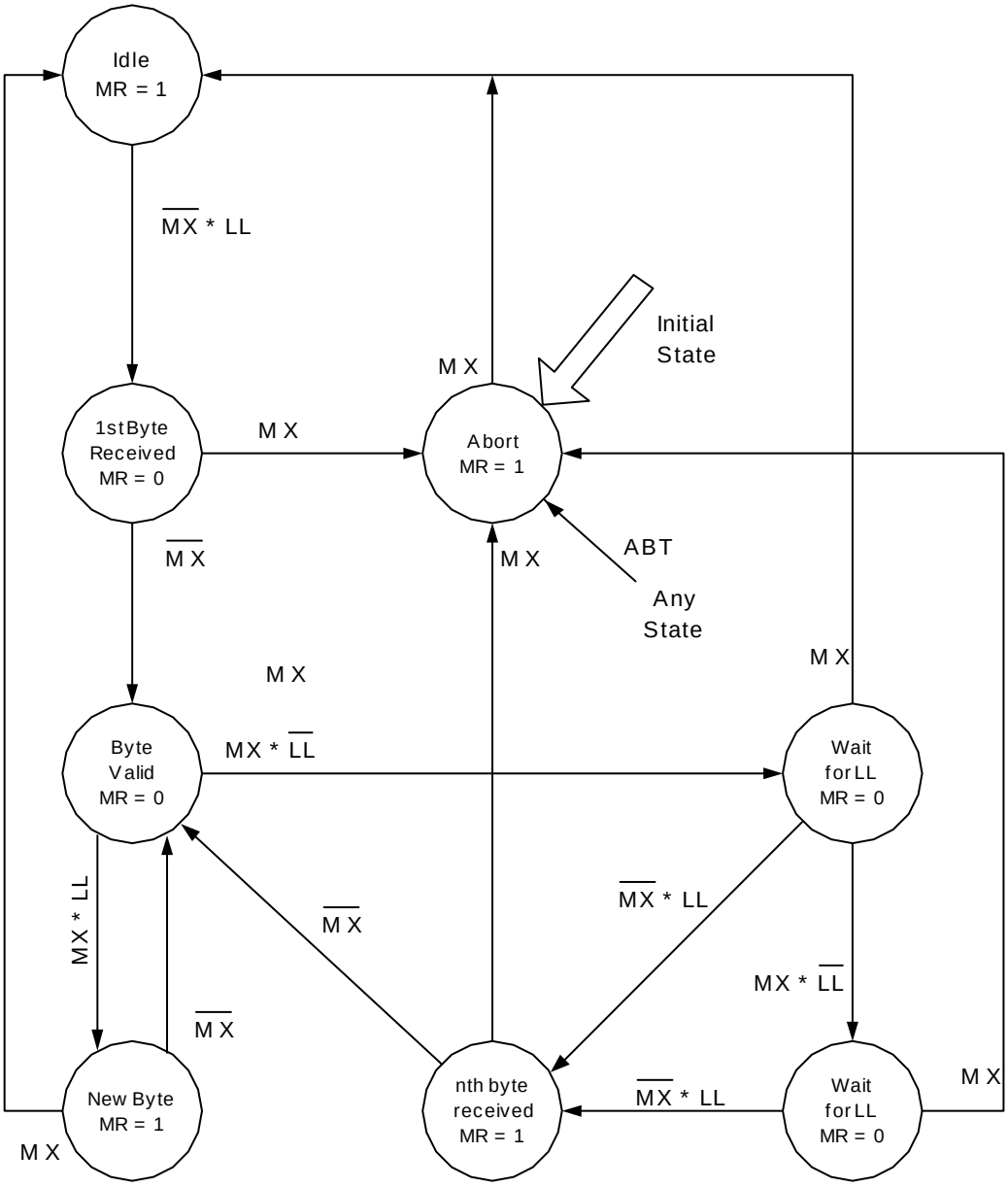
When the host is performing a write command, the host only manipulates the downstream MX bit, and the Dual ProSLIC only manipulates the upstream MR bit. If a read command is performed, the host initially manipulates the downstream MX bit to communicate the command, but then manipulates the downstream MR bit in response to the Dual ProSLIC responding with the requested data. Similarly, the Dual ProSLIC initially manipulates its upstream MR bit to receive the read command, and will then manipulate its upstream MX bit to respond with the requested data. If the host is transmitting data, the Dual ProSLIC always transmits a $FF value on its Monitor data byte. While the Dual ProSLIC is transmitting data, the host should always transmit a $FF value on its Monitor byte. If the Dual ProSLIC is transmitting data and detects a value other than a $FF on the downstream Monitor byte, the Dual ProSLIC signals an Abort.

For read and write commands, an initial address must be specified. The Dual ProSLIC responds to a read or a write command at this address, and then subsequently increment this address after every register access. In this manner, multiple consecutive registers can be read or written in one transmission sequence. By correctly manipulating the MX and MR bits, a transmission sequence can continue from the beginning specified address until an invalid memory location is reached. To end a transmission sequence, the host processor must signal an End-of-Message (EOM) by placing the downstream MX and MR bits inactive for two consecutive frames. The transmission can also be stopped by the Dual ProSLIC by signaling an Abort. This is signaled by placing the upstream MR bit inactive for at least two consecutive cycles in response to the downstream MX bit going active. An abort is signaled by the Dual ProSLIC for the following reasons:

- A read or write to an invalid memory address is attempted.
- An invalid command sequence is received.
- A data byte was not received for at least two consecutive frames.
- A collision occurs on the Monitor data bytes while the Dual ProSLIC is transmitting data.
- Downstream monitor byte not $FF while upstream monitor byte is transmitting.
- MR/MX protocol violation

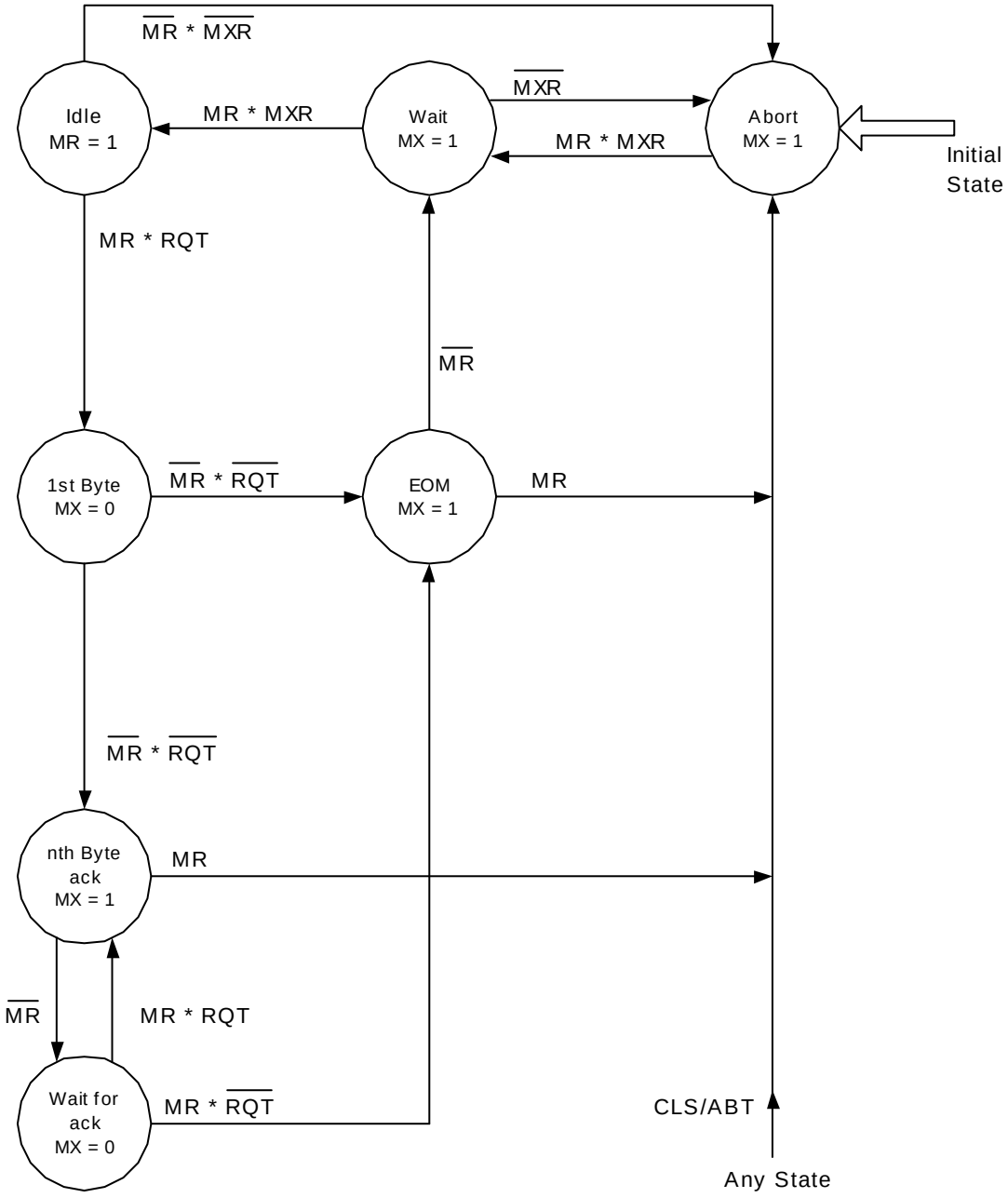
Whenever the Dual ProSLIC aborts due to an invalid command sequence, the state of the Dual ProSLIC does not change. If a read or write to an invalid memory address is attempted, all previous reads or writes in that transmission sequence are valid up to the read or write to the invalid memory address. If an end-of-message is detected before a valid command sequence is communicated, the Dual ProSLIC returns to the idle state and remains unchanged.

The data presented to the Dual ProSLIC in the downstream Monitor bits must be present for two consecutive frames to be considered valid data. The Dual ProSLIC is designed to ensure it has received the same data in two consecutive frames. If it does not, it does not acknowledge receipt of the data byte and waits until it does receive two consecutive identical data bytes before acknowledging to the transmitter it has received the data. If the transmitter attempts to signal transmission of a subsequent data byte by placing the downstream MX bit in an inactive state while the Dual ProSLIC is still waiting to receive a valid data byte transmission of two consecutive identical data bytes, the Dual ProSLIC signals an abort and ends the transmission. Figure 58 shows a state diagram for the Receiver Monitor channel for the Dual ProSLIC. Figure 59 shows a state diagram for the Transmitter Monitor channel for the Dual ProSLIC.



MR: MR bit calculated and transmitted on data upstream (DTX) line.
MX: MX bit received data downstream (DRX) line.
LL: Last look of monitor byte received on DRX line.
ABT: Abort indication to internal source.

Figure 58. Dual ProSLIC Monitor Receiver State Diagram



MR: MR bit received on DRX line.
MX: MX bit calculated and expected on DTX line.
MXR: MX bit sampled on DTX line.
CLS: Collision within the monitor data byte on DTX line.
RQT: Request for transmission from internal source.
ABT: Abort request/indication.

Figure 59. Dual ProSLIC Monitor Transmitter State Diagram

Figures 60 and 61 are example timing diagrams of a register read and a register write to the Dual ProSLIC using the GCI. As noted in Figure 59, the transmitter should always anticipate the acknowledgement of the receiver for correct communication with the Dual ProSLIC. **Devices that do not accept this "best case" timing scenario will not be able to communicate with the Dual ProSLIC.**

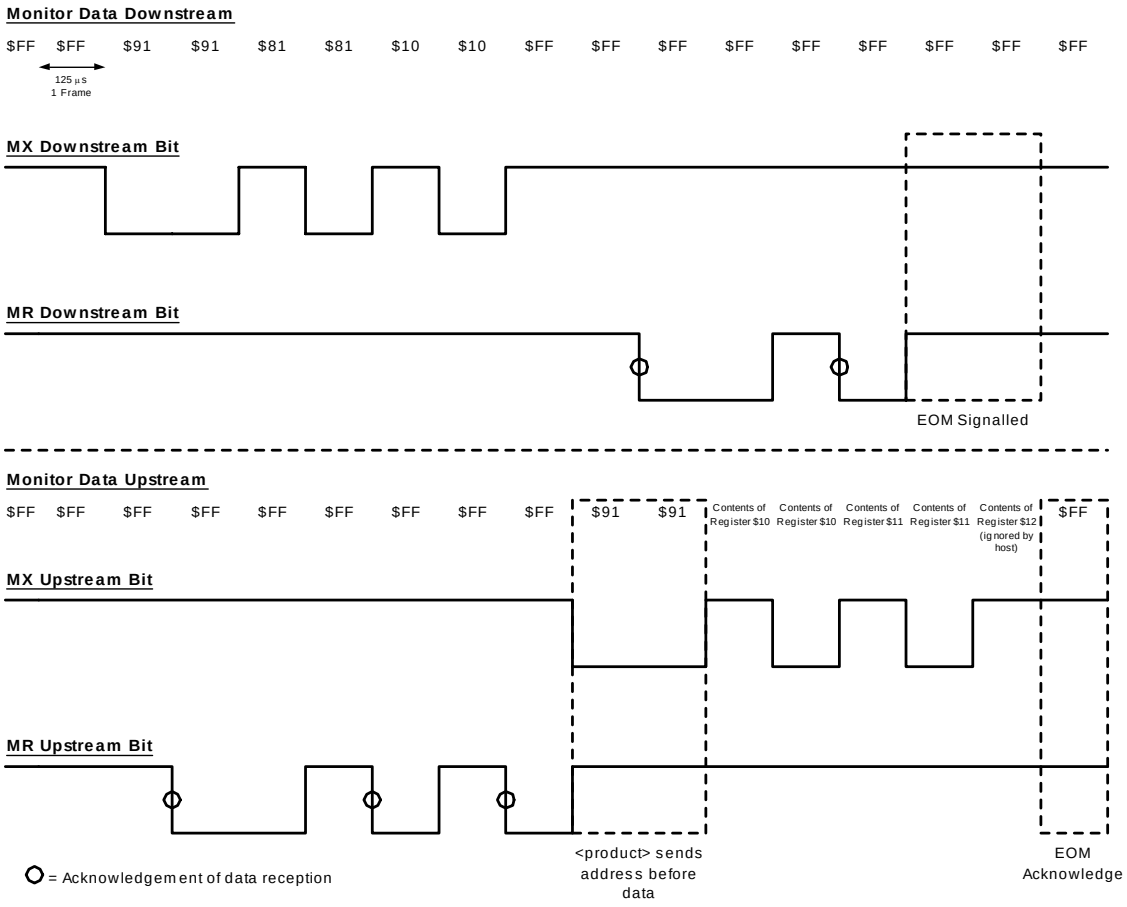


Figure 60. Example Read of Registers $10 and $11 in Channel 0 of the Dual ProSLIC

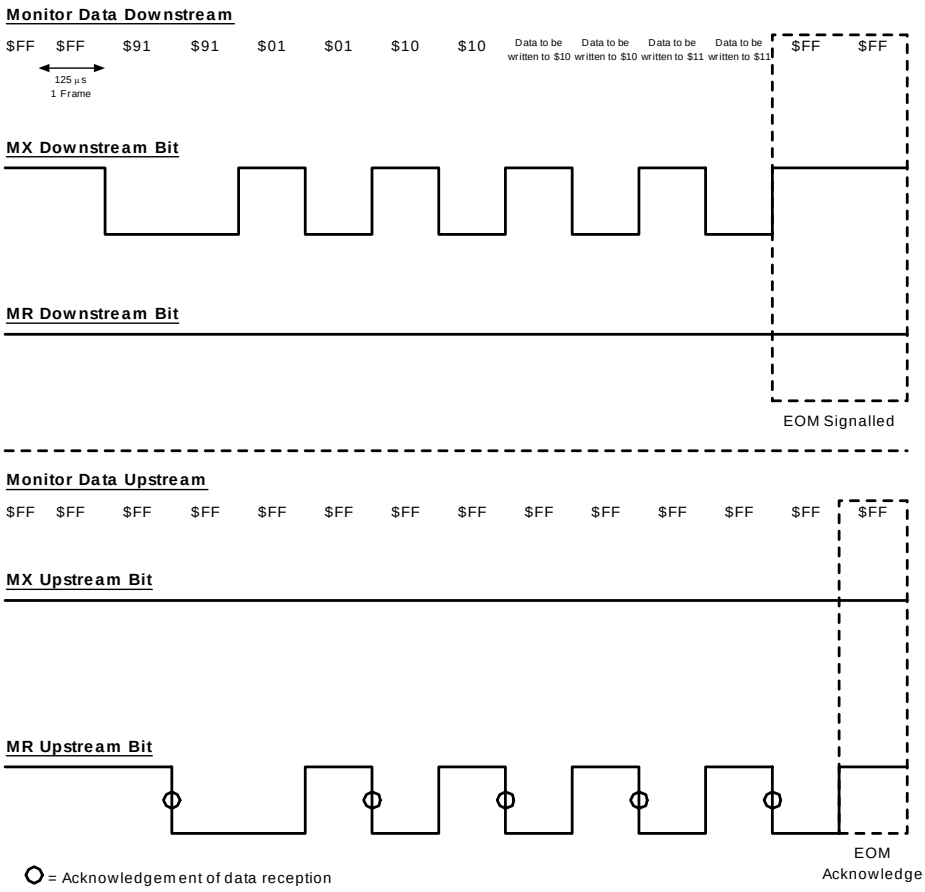


Figure 61. Example Write to Registers $10 and $11 in Channel 0 of the Dual ProSLIC

Programming the Dual ProSLIC Using the Monitor Channel

The Dual ProSLIC devices use the monitor channel to Transfer Status or Operating mode information to and from the host processor. Communication with the Dual ProSLIC should be in the following format:

Byte 1: Device Address Byte

Byte 2: Command Byte

Byte 3: Register Address Byte

Bytes 4-n: Data Bytes

Bytes n+1, N+2: EOM

Device Address Byte

The Device Address Byte identifies which device receives the particular message. This address must be the first byte sent to the Dual ProSLIC at the beginning of each transmission sequence. The Device Address Byte has the following structure:

MSB							LSB
7	6	5	4	3	2	1	0
1	0	0	A	B	0	0	C

A = 1: Channel A receives the command

A = 0: Channel A does not receive the command

B = 1: Channel B receives the command

B = 0: Channel B does not receive the command

C = 1: Normal command follows

C = 0: Channel identification command

When C = 1, bits A and B are channel enable bits. When these bits are set to 1, the corresponding channels receives the command in the next command byte. The channels with corresponding bits set to 0 ignore the subsequent command byte.

Channel Identification (CID) Command

The lowest programmable bit of the Device Address Byte, C, enables a special Channel Identification Command to identify themselves by software. The structure of this command is as follows:

A = 1: Channel A is the destination

A = 0: Channel B is the destination

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Address Byte	1	0	0	A	0	0	0	0
Command Byte	0	0	0	0	0	0	0	0

Immediately after the last bit of the CID command is received, the Dual ProSLIC responds with a fixed two-byte identification code as follows:

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Address Byte	1	0	0	A	0	0	0	0
Command Byte	1	0	1	1	1	1	1	0

A = 1: Channel A is the source

A = 0: Channel B is the source

Upon sending the two-byte CID command, the Dual ProSLIC sends an EOM signal (MR = MX = 1) for two consecutive frames. When C = 0, B must be 0 or the Dual ProSLIC signals an abort due to an invalid command. In this mode, only bit C is programmable.

Command Byte

The Command Byte has the following structure:

MSB		LSB
RW	CMD[6:0]	

RW = 1: A Read operation is performed from the Dual ProSLIC

RW = 0: A Write operation is performed to the Dual ProSLIC

CMD[6:0] = 0000001: Read or Write from the Dual ProSLIC

CMD[6:0] = 0000010-1111111: Reserved

Register Address Byte

The Register Address Byte has the following structure:

MSB	LSB
ADDRESS[7:0]	

This byte contains the actual 8-bit address of the register to be read or written.

SC Channel

The downstream and upstream SC channels are continuously carrying I/O information to and from the Dual ProSLIC during every frame. The upstream processor has immediate access to the receive (downstream) and transmit (upstream) data present on the Dual ProSLIC's digital I/O port when used in GCI mode. The SC channel consists of six C/I bits and two handshaking bits as described in the tables below. The functionality of the handshaking bits is defined in the Monitor Channel section. This section defines the functionality of the six C/I bits whether they are being transmitted to the GCI bus via the DTX pin (upstream) or received from the GCI bus via the DRX pin (downstream). The structure of the SC channel is shown in Figure 62.

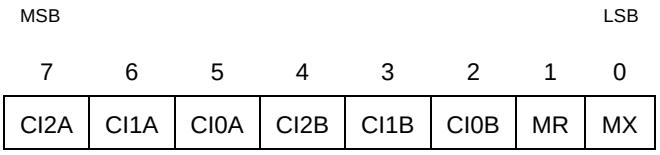


Figure 62. SC Channel Structure

Downstream (Receive) SC Channel Byte

The first six bits in the downstream SC channel control both channels of the Dual ProSLIC where the C/I bits are defined as follows:

CI2A, CI1A, CI0A	Used to select operating mode for channel A
CI2B, CI1B, CI0B	Used to select operating mode for channel B
MR, MX	Monitor channel handshake bits

Table 44. Programming Operating Modes Using Downstream SC Channel C/I Bits

Channel Specific C/I bits			Dual ProSLIC Operating Mode
CI2x	CI1x	CI0x	
0	0	0	Open (high impedence, no line monitoring)
0	0	1	Forward Active
0	1	0	Forward On-Hook Transmission
0	1	1	Ground Start (Tip Open)
1	0	0	Ringing
1	0	1	Reverse Active
1	1	0	Reverse On-Hook Transmission
1	1	1	Ground Start (Ring Open)

Note: x = A or B, corresponding to channel A or channel B.

Figure 63 illustrates the transmission protocol for the C/I bits within the downstream SC channel. New data received by either channel must be present and match for two consecutive frames to be considered valid. When a new command is communicated via the downstream C/I bits, this data must be sent for at least two consecutive frames to be recognized by the Dual ProSLIC.

The current state of the C/I bits is stored in a primary register P. If the received C/I bits are identical to the current state, no action is taken. If the received C/I bits differ from those in register P, the new set of C/I bits is loaded into secondary register S and a latch is set. When the next set of C/I bits is received during the frame that immediately follows, the following rules apply:

- If the received C/I bits are identical to the contents of register S, the stored C/I bits are loaded into register P and a valid C/I bit transition is recognized. The latch is reset and the Dual ProSLIC responds accordingly to the command represented by the new C/I bits.
- If the received C/I bits differ from both the contents of register S and the contents of register P, the newly received C/I bits are loaded into register S and the latch remains set. This cycle continues as long as any new set of C/I bits differs from the contents of registers S and P.
- If the newly received C/I bits are identical to the contents of register P, the contents of register P remain unchanged and the latch is reset.

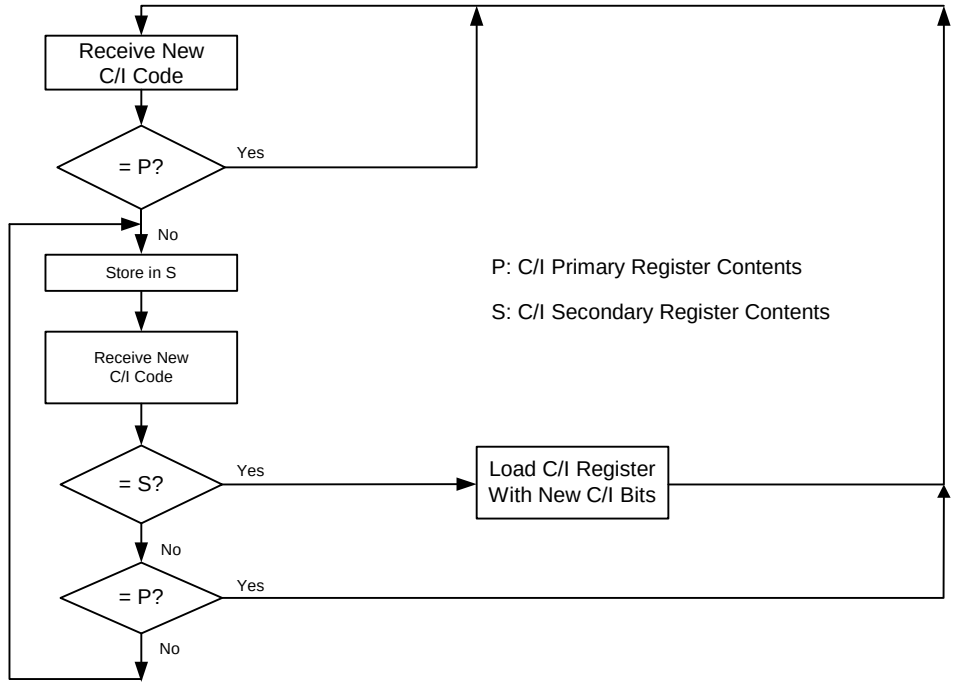


Figure 63. Protocol for Receiving C/I Bits in the Dual ProSLIC

When the Dual ProSLIC is set to GCI mode at initialization, the default setting ignores the downstream SC channel byte and allows linefeed state commands to be directed through the monitor channel. This default configuration is enabled by initializing the GCILINE bit of the PCMMODE register to 0, which prevents the Dual ProSLIC from transitioning between linefeed operating states due to invalid data that may exist within the downstream SC channel byte. To transfer direct linefeed control to the downstream SC channel, the user must set the GCILINE bit to 1. Once the GCILINE bit has been set, the Dual ProSLIC follows the commands that are contained in the downstream SC channel byte as described in Figure 62.

The Dual ProSLIC architecture also enables automatic transitions between linefeed operating states to reduce the amount of interaction required between the host processor and the Dual ProSLIC. When a GCI bus is implemented, the user must ensure that these automatic linefeed state transitions are consistent with the linefeed commands contained within the downstream SC channel byte.

In normal operation these automatic linefeed state transitions are accompanied by the setting of a threshold detection flag and an interrupt bit, if enabled. To allow the Dual ProSLIC to automatically detect the appropriate thresholds and control the linefeed transitions, the downstream SC channel byte should be updated accordingly once the interrupt bit is read from the upstream SC channel byte. To disable the automatic transitions, the user must set the GCILINE bit. Enabling this Manual mode requires the host processor to read the upstream SC channel information and provide the appropriate downstream SC channel byte command to program the correct linefeed state.

Table 45 presents the automatic linefeed state transitions and their associated registers that cause the transition.

The transition to the OPEN state stemming from power alarm detection is intended to protect the Dual ProSLIC circuit in the event that too much power is dissipated in the Si3200 LFIC. This alarm is typically due to a fault in the application circuit or on the subscriber loop, but can be caused by intermittent power spikes depending on the threshold to which the alarm is set. The user can re-initialize the linefeed operating state that was in effect just prior to the power alarm by toggling the downstream SC channel byte to the OPEN state for two consecutive cycles and then resetting the downstream SC channel byte to the intended linefeed state for two consecutive

cycles. If the Dual ProSLIC continues to automatically transition to the OPEN state, the power alarm threshold might be set incorrectly. If this problem persists after the power alarm settings are verified, a system fault is probable and the user should take measures to diagnose the problem.

Table 45. Automatic Linefeed State Transitions

Initiating Action	Automatic Linefeed State Transition	Detection/Control Bits	Interrupt Enable/Status Bits
Loop closure detected	On-hook active → off-hook active, Off-hook active → on-hook active	LCR (Register 9)	LOOPE, LOOPS (Register 16/19)
Ring trip detected	Ringing → off-hook active	RTP (Register 9)	RTRIPE, RTRIPS (Register 16/19)
Ringing burst cadence	Ringing → on-hook transmission On-hook transmission → ringing	T1EN, T2EN (Register 23)	RINGT1E, RINGT2E, RINGT1S, RINGT2S (Register 15/18)
Power alarm detected	Any state → open	PQ1DL (RAM 50)	PQ1E, PQ1S (Registers 17/20)

Upstream (Transmit) SC Channel Byte

The upstream SC channel byte looks similar to the downstream SC channel byte, except that the information quickly transfers the most time-critical information from the Dual ProSLIC to the GCI bus. Each upstream SC channel byte transfer from the Dual ProSLIC lasts for at least two consecutive frames to represent a valid transfer. The upstream C/I bits are defined as follows:

CI2A, CI1A, CI0A	Monitors status data for channel A
CI2B, CI1B, CI0B	Monitors status data for channel B
MR, MX	Monitor channel handshake bits (see Monitor Channel section)

Table 46. Monitored Data via Upstream SC Channel C/I Bits

C/I Bit	Information Provided	Context
CI2A	Interrupt information on channel A	CI2A = 0: No interrupt on channel A CI2A = 1: Interrupt present on channel A
CI1A	Hook status information on channel A	CI1A = 0: Channel A is on-hook CI1A = 1: Channel A is off-hook
CI0A	Ground key information on channel A	CI0A = 0: No longitudinal current detected CI0A = 1: Longitudinal current detected in ch A
CI2B	Interrupt information on channel B	CI2A = 0: No interrupt on channel B CI2A = 1: Interrupt present on channel B
CI1B	Hook status information on channel B	CI1A = 0: Channel B is on-hook CI1A = 1: Channel B is off-hook
CI0B	Ground key information on channel B	CI0A = 0: No longitudinal current detected CI0A = 1: Longitudinal current detected in ch B

The interrupt information for channels A and B is a single bit that indicates that one or more interrupts might exist on the respective channel. Each of the individual interrupt flags (see registers 18–20) can be individually masked by writing the appropriate bit in registers 21–23 to ignore specific interrupts. When using the GCI mode, the user should verify that each of the desired interrupt bits are set so the upstream SC channel byte includes the required interrupt functions.

System Testing

The Dual ProSLIC devices include a complete suite of test tools to test the functionality of the line card and detect fault conditions present on the TIP/RING pair. Using one of the loopback test modes with the signal generation and measurement tools eliminates the need for per-line test relays and centralized test equipment.

Loopback Modes

Three loopback test options are available for the Dual ProSLIC devices:

- The codec loopback path encompasses almost entirely the electronics of both the transmit and receive paths. The analog signal at the output of the receive path is fed back to the input of the transmit path through a feedback path on the analog side of the audio codec. Both the impedance synthesis and transhybrid balance functions are disabled in this mode. (See DLM3 path in Figure 11 on page 22.) The signal path starts with 8-bit PCM data input to the receive path and ends with 8-bit PCM data at the output of the transmit path. The user can bypass the companding process and interface directly to the 16-bit data.
- A second digital loopback takes the receive path digital stream and routes it back to the transmit path via the transhybrid feedback path. (See DLM2 path through block H in Figure 11.) This mode characterizes the transhybrid filter response. The transhybrid block also can be disabled (set to unity gain) in this mode for diagnosing the digital gain blocks and filter stages in both transmit and receive paths. The signal path starts with 8-bit PCM data input to the receive path and ends with 8-bit PCM data at the output of the transmit path. The user can bypass the companding process and interface directly to the 16-bit data.
- A third digital loopback takes the digital stream at the output of the µ-Law/A-Law expander and feeds it back to the input of the µ-Law/A-Law compressor. (See DLM1 path in Figure 11.) This path verifies that the host is connected correctly with the Dual ProSLIC through the PCM interface and that the PCLK and FSYNC signals are correctly set. This mode also can test the µ-Law/A-Law companding process. The signal path starts with 8-bit PCM data input to the receive path and ends with 8-bit PCM data at the output of the transmit path. The user can also connect directly to the 16-bit data to eliminate the µ-Law/A-Law companding process when testing the PCM interface.

Line Test and Diagnostics

The Dual ProSLIC devices provide a variety of signal generation and measurement tools that facilitate fault detection and parametric diagnostics on the TIP/RING pair and line card functionality verification. The Dual ProSLIC generates test signals, measures the appropriate voltage/current/signal levels, and processes the results to provide a meaningful result to the user. Interaction is required from the host microprocessor to load the test parameters into the appropriate registers, initiate the test(s), and read the results from the registers. In some cases, the host processor might also be required to perform some simple mathematics to achieve the results. Software modules are available to simplify integration of the diagnostics functions into the system. The need for test relays and a separate test head is eliminated in most applications. To address legacy applications, all versions of the Dual proSLIC include test-in and test-out relay drivers to switch in a centralized test head.

The Dual ProSLIC's line test and diagnostics capabilities are categorized into three sections: signal generation tools, measurement tools, and diagnostics capabilities. Using these signal generation and measurement tools, a variety of other diagnostics functions can also be performed to meet the unique requirements of specific applications. Table 47 summarizes the ranges and capabilities of the signal generation and measurement tools.

Table 47. Summary of Signal Generation and Measurement Tools

Function	Range	Accuracy/Resolution	Comments
Signal Generation Tools			
DC Current Generation	18 to 45 mA	0.875 mA	
DC Voltage Generation	0 to 63.3 V	1.005 V	
Audio Tone Generation	200 to 3400 Hz		
Ringing Signal Generation	4 to 15 Hz 16 to 100 Hz	±5% ±1%	
Measurement Tools			
8-Bit DC/Low Frequency Monitor A/D Converter	High Range: 0 to 160.173 V 0 to 101.09 mA	628 mV 396.4 µA	800 Hz update rate ac_{rms}, ac_{PK}, and dc post-processing blocks
	Low Range: 0 to 64.07 V 0 to 50.54 mA	251 mV 198.2 µA	
Programmable Timer	0 to 8.19 s	125 µs	
AC Low Pass Filter	3 to 400 Hz		
16-Bit Audio A/D Converter	0 to 2.5 V	38 µV	
Transmit Path Notch Filter	300 to 3400 Hz		Single or dual notch, ≥90 dB attenuation
Transmit Path Bandpass Filter	300 to 3400 Hz		

Signal Generation Tools

- **TIP/RING DC signal generation.** The Dual ProSLIC line feed D/A converter can program a constant current linefeed from 18–45 mA in 0.87 mA steps with a ±10% total accuracy. In addition, the open-circuit TIP/RING voltage can be programmed from 0 to 63 V in 1 V steps. The linefeed circuitry also can generate a controlled polarity reversal.
- **Tone generation.** The Dual ProSLIC devices can generate single or dual tones over the entire audio band, and can direct them into either the transmit or the receive path depending on the diagnostic requirements. Ringing signals from 4–100 Hz also can be generated.
- **Diagnostics mode ringing generation.** The Dual ProSLIC devices can generate an internal low-level ringing signal to test for the presence of REN without causing the terminal equipment to ring audibly. This ringing signal can be either balance or unbalanced depending on the state of the RINGUNB bit of the RINGCON register. This feature is also available with the Si3225 provided that a sufficient battery voltage is present.

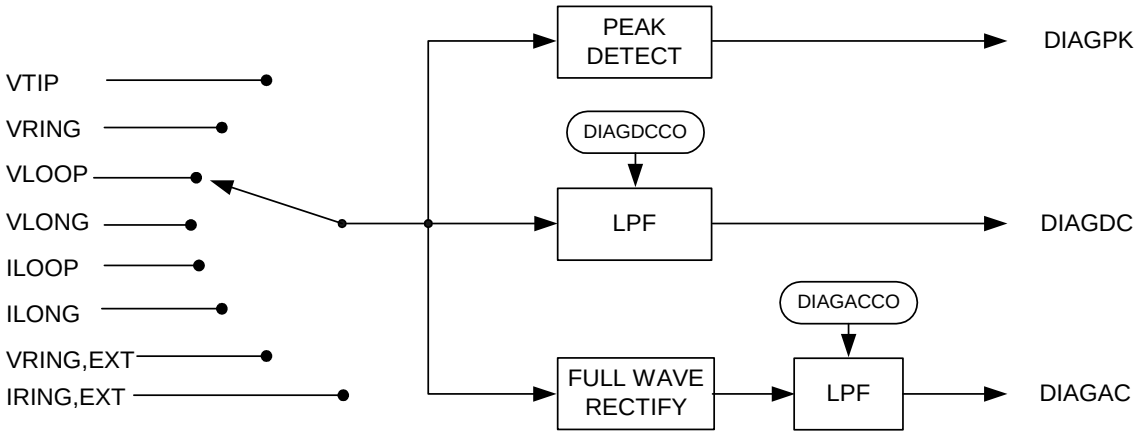


Figure 64. SLIC Diagnostic Filter Structure

Measurement Tools

- **8-Bit monitor A/D converter.** This 8-bit A/D converter monitors all dc and low frequency voltage and current data from TIP to ground and RING to ground. Two additional values, TIP – RING and TIP + RING, are calculated and stored in on-chip registers to analyze metallic and longitudinal effects. The A/D operates at an 800 Hz update rate to allow measurement bandwidth from dc to 400 Hz. A dual-range capability allows high-voltage/high-current measurement in the high range but also can measure lower voltages and currents with a tighter resolution.
- **Programmable bandpass filter.** A bandpass filter discriminates certain frequency ranges such as ringing frequencies and 50 Hz/60 Hz induction from nearby or crossed power leads.
- **SLIC diagnostics filter.** Several post-processing filter blocks monitor peak dc and ac characteristics of the Monitor A/D converter outputs and values derived from these outputs. Setting the SDIAG bit in the DIAG register enables the filters. There are separate filters for each channel, and their control is independent. These filters require DSP processing which is available only when voice band processing is not being performed. If an off-hook or a ring trip condition is detected while the SDIAG bit is set, the bit is cleared and the diagnostic information is not processed.
  The following parameters can be selected as inputs to the diagnostic block by setting the SDIAG bits in the DIAG register to values 0–7 corresponding to the order below:
  - V_{TIP} = voltage on the TIP lead
  - $V_{RI\ NG}$ = voltage on the RING lead
  - $V_{LOOP} = V_{TIP}-V_{RING}$ = metallic (loop) voltage
  - $V_{LONG} = (V_{TIP}+V_{RING})/2$ = longitudinal voltage
  - $I_{LOOP} = I_{TIP}-I_{RING}$ = metallic (loop) current
  - $I_{LOOP} = I_{TIP}-I_{RING}$ = metallic (loop) current
  - $I_{LONG} = (I_{TIP}+I_{RING})/2$ = longitudinal current
  - $V_{RING,\ EXT}$ = ringing voltage when using an external ringing source (Si3225 only)
  - $I_{RING,EXT}$ = ringing current when using an external ringing source (Si3225 only)

The SLIC diagnostic capability consists of a peak detect block and two filter blocks, one for dc and one for ac. The topology is illustrated in Figure 64.

The peak detect filter block reports the magnitude of the largest positive or negative value without sign. The dc filter block consists of a single pole IIR low pass filter with a coefficient held in the DIAGDCCO RAM location. The filter output is read from the DIAGDC RAM location. The ac filter block consists of a full wave rectifier, followed by a single pole IIR low pass filter with a coefficient held in the DIAGACCO RAM location. The peak value is read from the DIAGPK RAM location. The peak value is cleared and the filters are flushed on the 0-1 transition of the SDIAG bit and when the input source changes. The user can write 0 to the DIAGPK RAM location to get peak information for a specific time interval.

- **16-bit audio A/D converter.** The A/D converter portion of the audio codec is made available for processing test data received back through the transmit audio path. The audio path offers a 2.5 V peak voltage measurement capability and a coarse attenuation stage for scenarios where the incoming signal amplitude must be attenuated by as much as 3 dB to bring it into the allowable input range without clipping.

- **Programmable timer.** The Dual ProSLIC devices incorporate several digital oscillator circuits to program the on- and off-times of the ringing and pulse metering signals. The tone generation oscillator can be used to program a time period for averaging specific measured test parameters.
- **Transmit audio path diagnostics filter.** Transmit path audio diagnostics are facilitated by implementing a sixth-order IIR filter followed by peak detection and power estimation blocks. This filter can be programmed to eliminate or amplify specific signals for the purpose of measuring the peak amplitude and power content of individual components in the audio spectrum. Figure 11 on page 22 illustrates the location of the diagnostics filter block.
  The sixth order IIR filter operates at an 8 kHz sample rate and is implemented as three second-order filter stages in cascade. Each second-order filter offers five fully programmable coefficients (a1, a2, b0, b1, and b2) with 25-bit precision by providing several user-accessible registers. Each filter stage is implemented with the following format:

$$H(z) = \frac{(b0 + b1z^{-1} + b2z^{-2})}{(1 - a1z^{-1} - a2z^{-2})}$$

  If any of the second-order filter stages are not required, they can be programmed to H(z)=1 by setting a1=0, a2=0, b0=1, b1=0, and b2=0. This flexible filter block can be programmed any of the following characteristics:
  - **Single notch.** Used for measuring noise/distortion in the presence of a single tone. 90 dB attenuation is provided at the notched frequency. Implemented by placing two 0s on the unit circle at the notch frequency and two poles inside the unit circle at the notch frequency.
  - **Dual notch.** Used for measuring noise/distortion in the presence of dual tones.
  - **Single notch/single peak.** Used for measuring particular harmonic in the presence of a single tone.
  - **Dual notch/single peak.** Used to measure particular intermodulation product in the presence of dual tones.

Because each second-order filter stage is fully programmable, there are many other possible filter implementations.

The IIR filter output is measured for power and peak post-processing. The peak measurement window duration is programmable by entering a value into the TESTWLN RAM address. The peak value (TESTPKO) is updated at the end of each window period. Power measurement is performed by using a single pole IIR filter to average the output of the sixth-order IIR filter. The power averaging filter time constant is absolute value programmable, and the average power result is read from the TESTAVO RAM location.

Diagnostics Capabilities

- **Foreign voltages test.** The Dual ProSLIC devices can detect the presence of foreign voltages according to GR-909 requirements of ac voltages > 10 V and dc voltages > 6 V from T-G or R-G. This test is performed when it has been determined that a hazardous voltage is not present on the line.
- **Resistive faults (leakage current) test.** Resistive fault conditions are measured from T-G, R-G, or T-R for dc resistance per GR-909 specifications. If the dc resistance is < 150 kΩ, it is considered a resistive fault. To perform this test, program the Dual ProSLIC chipset to generate a constant open-circuit voltage and measure the resulting current. The resistance is then calculated.
- **Receiver off-hook test.** Uses a similar procedure as described in the Resistive Faults test above, but is measured across T-R only. In addition, two measurements must be performed at different open-circuit voltages to verify the resistive linearity. If the calculated resistance has more than 15% nonlinearity between the two calculated points and the voltage/current origin, it is determined to be a resistive fault.
- **Ringers (REN) test.** Verifies the presence of REN at the end of the TIP/RING pair per TA-909 specifications. It can be implemented by generating a 20 Hz ringing signal between 7 V_{rms} and 17 V_{rms} and measuring the 20 Hz ac current using the 8-bit monitor ADC. The resistance (REN) can then be calculated using the software module. The acceptable REN range is > 0.175 REN (< 40 kΩ) or < 5 REN (> 1400 Ω). A returned value of < 1400 Ω is determined to be a resistive fault from T-R, and a returned value > 40 kΩ is determined to be a loop with no handset attached.
- **ac line impedance measurement.** Determines the ac loop impedence across T-R. It can be implemented by sending out multiple discrete tones, one at a time, and measuring the returned amplitude with the hybrid balance filter disabled. By calculating the voltage difference between the initial amplitude and the received amplitude and dividing the result by the audio current, the line impedance can then be calculated.

- **Line capacitance measurement.** Implemented like the *ac line impedance measurement* test above, but the frequency band of interest is between 1 kHz and 3.4 kHz. Knowing the synthesized 2-wire impedance of the Dual ProSLIC, the roll-off effect can be used to calculate the ac line capacitance.
- **Ringing voltage verification.** Verifies that the desired ringing signal is correctly applied to the TIP/RING pair and can be measured in the 8-bit monitor ADC, which senses low frequency signals directly across T-R.
- **Idle channel noise measurement.** Given any transmission mode with no tone generated and the hybrid balance filter turned off, the voice band energy can be measured through the normal audio path and read through the appropriate register.
- **Echo path gain measurement.**
- **Harmonic distortion measurement.** Detects the power content of a particular harmonic. It can be implemented by programming two of the IIR diagnostics filter stages to provide a notch at the fundamental frequency and a peak at the harmonic of interest. Performing this procedure on all relevant harmonics individually and summing the results provide the total harmonic distortion.
- **Intermodulation distortion measurement (two-tone method).** Measures the intermodulation distortion product in the presence of two tones. It can be implemented by programming the three IIR diagnostics filter stages to provide two notches at the two tone frequencies and a peak at the frequency of interest.

8-Bit Control Register Summary

Any register not listed here is reserved and must not be written. Shaded registers are read only. All registers are assigned a default value during initialization and following a system reset. Only registers 0, 2, 3, and 14 are available until a PLL lock is established or during a clock failure. Refer to AN58 “Dual ProSLIC Programmer Guide” for detailed register descriptions and recommended settings.

(Ordered alphabetically by mnemonic except in cases of high, medium and low bytes which are ordered high to low.)

Reg Addr[3]	Mnemonic	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	R/W	Def. Hex
Audio													
21	AUDGAIN	Audio Gain Control		ATXMUTE				ARXMUTE			Init	R/W	0x00
Calibration													
11	CALR1	Calibration Register 1	CAL		CALOFFR	CALOFFT	CALOFFRN	CALOFFTN	CALDIFG	CALCMG	Init	R/W	0x3F
12	CALR2	Calibration Register 2			CALLKGR	CALLKGT	CALMADC	CALDACO	CALADCO	CALCMBAL	Init	R/W	0x3F
Diagnostic Tools													
13	DIAG	Diagnostics Tool Enable	IQ2HR	IQ1HR	TSTRING	TXFILT	SDIAG	SDIAGIN[2:0]			Diag	R/W	
Digital Control and Loopback													
22	DIGCON	Digital Control and Loopback Enable	CODECLB	PCMLB	HYBLB	HYBDIS	THPFDIS	RHPFDIS	DTXMUTE	DRXMUTE	Diag	R/W	0x00
FSK Data Byte													
68	FSKDAT	FSK Data Byte	FSKBYTE[7:0]								Oper	R/W	0x00
Chip ID													
0	ID	Chip ID		PARTNUM[2:0][4]			REV[3:0][4]				Init	R	0x—
Loop Current Limit													
10	ILIM	Loop Current Limit				ILIM[4:0]					Init	R/W	0x05
Interrupts													
14	IRQ0	Interrupt Status 0	CLKIRQ[4,6]	IRQ3B[4,6]	IRQ2B[4,6]	IRQ1B[4,6]		IRQ3A[4,6]	IRQ2A[4,6]	IRQ1A[4,6]	Oper	R	0x00
15	IRQ1	Interrupt Status 1	PULSTAS	PULSTIS	RINGTAS	RINGTIS	OS2TAS	OS2TIS	OS1TAS	OS1TIS	Oper	R/W	0x00
16	IRQ2	Interrupt Status 2	RXMDMS	TXMDMS	RAMIRS	DTMFS	VOCTRKS	LONGS	LOOPS	RTRIPS	Oper	R/W	0x00
17	IRQ3	Interrupt Status 3	CMBALS		PQ6S	PQ5S	PQ4S	PQ3S	PQ2S	PQ1S	Oper	R/W	0x00
18	IRQEN1	Interrupt Enable 1	PULSTAE	PULSTIE	RINGTAE	RINGTIE	OS2TAE	OS2TIE	OS1TAE	OS1TIE	Init	R/W	0x00
19	IRQEN2	Interrupt Enable 2	RXMDME	TXMDME	RAMIRE	DTMFE	VOCTRKE	LONGE	LOOPE	RTRIPE	Init	R/W	0x00
20	IRQEN3	Interrupt Enable 3	CMBALE		PQ6E	PQ5E	PQ4E	PQ3E	PQ2E	PQ1E	Init	R/W	0x00
Linefeed Control													
9	LCRRTP	Loop Closure/Ring Trip/ Ground Key Detection			CMH[4]	SPEED[4]	VOCTST[4]	LONGHI[4]	RTP[4]	LCR[4]	Oper	R	0x40
6	LINEFEED	Linefeed		LFS[2:0][4]				LF[2:0]			Oper	R/W	0x00

Notes:

1. Any register not listed is reserved and must not be written. Default hex value is loaded to register following any RESET. Only registers ID, MSTREN, MSTRSTAT, and IRQ0 are valid while the PLL is not locked (MSTRSTAT[PLOCK]).
2. Reserved bit values are indeterminate.
3. Register address is in decimal.
4. Read only.
5. Protected bits.
6. Per channel bit(s).
7. Si3220 only.

Reg Addr[3]	Mnemonic	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	R/W	Def. Hex
SPI													
2	MSTREN	Master Initialization Enable	PLLFLT	FSFLT	PCFLT						Init	R/W	0x00
3	MSTRSTAT	Master Initialization Status	PLLFAULT	FSFAULT	PCFAULT	SRCLR[4]	PLOCK[4]	FSDET[4]	FSVAL[4]	PCVAL[4]	Init	R/W	0x00
Oscillators													
61	O1TAHI	Oscillator 1 Active Timer—High Byte	OSC1TA[15:8]								Init	R/W	0x00
60	O1TALO	Oscillator 1 Active Timer—Low Byte	OSC1TA[7:0]								Init	R/W	0x00
63	O1TIHI	Oscillator 1 Inactive Timer—High Byte	OSC1TI[15:8]								Init	R/W	0x00
62	O1TILO	Oscillator 1 Inactive Timer—Low Byte	OSC1TI[7:0]								Init	R/W	0x00
65	O2TAHI	Oscillator 2 Active Timer—High Byte	OSC2TA[15:8]								Init	R/W	0x00
64	O2TALO	Oscillator 2 Active Timer—Low Byte	OSC2TA[7:0]								Init	R/W	0x00
67	O2TIHI	Oscillator 2 Inactive Timer—High Byte	OSC2TI[15:8]								Init	R/W	0x00
66	O2TILO	Oscillator 2 Inactive Timer—Low Byte	OSC2TI[7:0]								Init	R/W	0x00
59	OCON	Oscillator Control	ENSYNC2[4]	OSC2TAEN	OSC2TIEN	OSC2EN	ENSYNC1[4]	OSC1TAEN	OSC1TIEN	OSC1EN	Oper	R/W	0x00
58	OMODE	Oscillator Mode Select	FSKSSEN	ZEROEN2	ROUT2[1:0]		OSC1FSK	ZEROEN1	ROUT1[1:0]		Init	R/W	0x00
PCM Control													
53	PCMMODE	PCM Mode Select	GCILINE[6]	PCLK2X[6]	PCMTRI[6]	PCMEN	ALAW[1:0][6]		PCMF[1:0][6]		Init	R/W	0x05
57	PCMRXHI	PCM RX Clock Slot—High Byte							PCMRX[9:8]		Init	R/W	0x00
56	PCMRXL0	PCM RX Clock Slot—Low Byte	PCMRX[7:0]								Init	R/W	0x00
55	PCMTXHI	PCM TX Clock Slot—High Byte							PCMTX[9:8]		Init	R/W	0x00
54	PCMTXLO	PCM TX Clock Slot—Low Byte	PCMTX[7:0]								Init	R/W	0x00
Pulse Metering													
28	PMCON	Pulse Metering Control	ENSYNC[4,7]			TAEN1[7]	TIEN1[7]	PULSE1[7]			Oper	R/W	0x00
30	PMTAHI	Pulse Metering Oscillator Active Timer—High Byte	PULSETA[15:8][7]								Init	R/W	0x00
29	PMTALO	Pulse Metering Oscillator Active Timer—Low Byte	PULSETA[7:0][7]								Init	R/W	0x00
32	PMTIHI	Pulse Metering Oscillator Inactive Timer—High Byte	PULSETI[15:8][7]								Init	R/W	0x00

Notes:

1. Any register not listed is reserved and must not be written. Default hex value is loaded to register following any RESET. Only registers ID, MSTREN, MSTRSTAT, and IRQ0 are valid while the PLL is not locked (MSTRSTAT[PLOCK]).
2. Reserved bit values are indeterminate.
3. Register address is in decimal.
4. Read only.
5. Protected bits.
6. Per channel bit(s).
7. Si3220 only.

Reg Addr[3]	Mnemonic	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	R/W	Def. Hex
31	PMTILO	Pulse Metering Oscillator Inactive Timer—Low Byte	PULSETI[7:0][7]								Init	R/W	0x00
Polarity Reversal													
7	POLREV	Polarity Reversal Settings					POLREV[4]	VOCZERO	PREN	RAMP	Init	R/W	
RAM Access													
103	RAMADDR	RAM Address	RAMADDR[7:0]								Oper	R/W	0x00
102	RAMDATHI	RAM Data—High Byte	RAMDAT[15:8]								Oper	R/W	0x00
101	RAMDATLO	RAM Data—Low Byte	RAMDAT[7:0]								Oper	R/W	0x00
4	RAMSTAT	RAM Address Status								RAMSTAT[4]	Init	R	0x00
Soft Reset													
1	RESET	Soft Reset							RESETB	RESETA	Init	R/W	0x00
Ringing													
23	RINGCON	Ringing Configuration	ENSYNC[4]	RDACEN[4]	RINGUNB	TAEN	TIEN	RINGEN[4]	UNBPOLR	TRAP	Init	R/W	0x00
25	RINGTAHI	Ringing Oscillator Active Timer—High Byte	RINGTA[15:8]								Init	R/W	0x00
24	RINGTALO	Ringing Oscillator Active Timer—Low Byte	RINGTA[7:0]								Init	R/W	0x00
27	RINGTIHI	Ringing Oscillator Inactive Timer—High Byte	RINGTI[15:8]								Init	R/W	0x00
26	RINGTILO	Ringing Oscillator Inactive Timer—Low Byte	RINGTI[7:0]								Init	R/W	0x00
Relay Configuration													
5	RLYCON	Relay Driver and Battery Switching Configuration			BSEL[5]	RRAIL	RDOE	RRD/GPO	TRD2	TRD1	Diag	R/W	0x00
SLIC Bias Control													
8	SBIAS	SLIC Bias Control					OBIAS[1:0][5]		ABIAS[1:0][5]		Init	R/W	0xE0
Si3200 Thermometer													
72	THERM	Si3200 Thermometer	STAT[4]								Oper	R/W	0x45
Tone Detection													
70	TONDET	Modem Tone Detection	FAILCNT[3:0]				PASSCNT[3:0]				Oper	R/W	0x00
69	TONDTMF	DTMF Detection			VALID[4]	VALTONE[4]	DTMFDIGIT[3:0][4]				Oper	R	0x00
71	TONDEN	Tone Detection Enable						DTMF	RXMDM	TXMDM	Init	R/W	0x00
Impedance Synthesis Coefficients													
49	ZA1HI	Impedance Synthesis Coeff A1— High Byte				COEFFA1[20:16][6]					Init	R/W	0x00
48	ZA1MID	Impedance Synthesis Coeff A1—Middle Byte	COEFFA1[15:8][6]								Init	R/W	0x00

Notes:
1. Any register not listed is reserved and must not be written. Default hex value is loaded to register following any RESET. Only registers ID, MSTREN, MSTRSTAT, and IRQ0 are valid while the PLL is not locked (MSTRSTAT[PLOCK]).
2. Reserved bit values are indeterminate.
3. Register address is in decimal.
4. Read only.
5. Protected bits.
6. Per channel bit(s).
7. Si3220 only.

Reg Addr[3]	Mnemonic	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	R/W	Def. Hex
47	ZA1LO	Impedance Synthesis Coeff A1—Low Byte	COEFFA1[7:0]								Init	R/W	0x00
52	ZA2HI	Impedance Synthesis Coeff A2—High Byte				COEFFA2[20:16][6]					Init	R/W	0x00
51	ZA2MID	Impedance Synthesis Coeff A2—Middle Byte	COEFFA2[15:8][6]								Init	R/W	0x00
50	ZA2LO	Impedance Synthesis Coeff A2—Low Byte	COEFFA2[7:0][6]								Init	R/W	0x00
37	ZB0HI	Impedance Synthesis Coeff B0—High Byte	COEFFB0[23:16][6]								Init	R/W	0x00
36	ZB0MID	Impedance Synthesis Coeff B0—Middle Byte	COEFFB0[15:8][6]								Init	R/W	0x00
35	ZB0LO	Impedance Synthesis Coeff B0—Low Byte	COEFFB0[7:0][6]								Init	R/W	0x00
40	ZB1HI	Impedance Synthesis Coeff B1—High Byte	COEFFB1[23:16][6]								Init	R/W	0x00
39	ZB1MID	Impedance Synthesis Coeff B1—Middle Byte	COEFFB1[15:8][6]								Init	R/W	0x00
38	ZB1LO	Impedance Synthesis Coeff B1— Low Byte	COEFFB1[7:0][6]								Init	R/W	0x00
43	ZB2HI	Impedance Synthesis Coeff B2—High Byte	COEFFB2[23:16][6]								Init	R/W	0x00
42	ZB2MID	Impedance Synthesis Coeff B2—Middle Byte	COEFFB2[15:8][6]								Init	R/W	0x00
41	ZB2LO	Impedance Synthesis Coeff B2— Low Byte	COEFFB2[7:0][6]								Init	R/W	0x00
46	ZB3HI	Impedance Synthesis Coeff B3—High Byte	COEFFB3[23:16][6]								Init	R/W	0x00
45	ZB3MID	Impedance Synthesis Coeff B3—Middle Byte	COEFFB3[15:8][6]								Init	R/W	0x00
44	ZB3LO	Impedance Synthesis Coeff B3—Low Byte	COEFFB3[7:0][6]								Init	R/W	0x00
33	ZRS	Impedance Synthesis Analog Real Coeff					RS[3:0][6]				Init	R/W	0x00
34	ZZ	Impedance Synthesis Analog Complex Coeff	ZSDIS[6]	ZSOHT[6]	ZP[1:0][6]				ZZ[1:0][6]		Init	R/W	0x00

Notes:

1. Any register not listed is reserved and must not be written. Default hex value is loaded to register following any RESET. Only registers ID, MSTREN, MSTRSTAT, and IRQ0 are valid while the PLL is not locked (MSTRSTAT[PLOCK]).
2. Reserved bit values are indeterminate.
3. Register address is in decimal.
4. Read only.
5. Protected bits.
6. Per channel bit(s).
7. Si3220 only.

16-Bit RAM Address Summary

All internal 16-bit RAM addresses can be assigned unique values for each SLIC channel and are accessed in a similar manner as the 8-bit control registers except the data is twice as long. In addition, one more READ cycle is required during READ operations to accommodate the one-deep pipeline architecture. See "SPI Control Interface" on page 62 for more details. All internal RAM addresses are assigned a default value of 0 during initialization and following a system reset. Unless otherwise noted, all RAM addresses use a 2's complement, MSB first date format. Refer to AN58 "Dual ProSLIC Programmer Guide" for detailed RAM location descriptions and recommended settings.

Note: Any RAM address not listed is reserved and must not be written. (ordered alphabetically by mnemonic)

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Example Hex	Example Dec	Unit
Battery Selection and VOC Tracking																						
31	BATHTH	High Battery Switch Threshold		BATHTH[14:7][2]															Init	0E54	18	V
34	BATLPF	Battery Tracking Filter Coeff	BATLPF[15:3]																Init	0A08	10	Hz
32	BATLTH	Low Battery Switch Threshold		BATLTH[14:7][2]															Init	0D88	17	V
33	BSWLPF	RING Voltage Filter Coeff	BSWLPF[15:3]																Init	0A08	10	Hz
Speedup																						
36	CMHITH	Speedup Threshold—High Byte	CMHITH[15:0]																Init	0001	1	V
35	CMLOTH	Speedup Threshold—Low Byte	CMLOTH[15:0]																Init	07F5	10	V
SLIC Diagnostics Filter																						
53	DIAGAC	SLIC Diags AC Detector Threshold	DIAGAC[15:0]																Diag			V
54	DIAGACCO	SLIC Diags AC Filter Coeff	DIAGACCO[15:3]																Diag	7FF8	127.3	Hz
51	DIAGDC	SLIC Diags DC Output	DIAGDC[15:0]																Diag			V
52	DIAGDCCO	SLIC Diags DC Filter Coeff	DIAGDCCO[15:3]																Diag	0A08	10	Hz
55	DIAGPK	SLIC Diags Peak Detector	DIAGPK[15:0]																Diag			V
DTMF Detection																						
118	DTCOL2HTH	DTMF Column Second Harmonic Threshold	DTCOL2HTH[15:3]																Init	1013		
116	DTCOLRTH	DTMF Column Ratio Threshold	DTCOLRTH[15:3]																Init	0CC5		
112	DTCOLTH	DTMF Column Peak Threshold	DTCOLTH[15:3]																Init	1999		
113	DTFTWTH	DTMF Forward Twist Threshold	DTFTWTH[15:3]																Init	1013		
120	DTHOTTH	DTMF Hot Limit Threshold	DTHOTTH[15:0]																Init	0A1C		
119	DTMINPTH	DTMF Minimum Power Threshold	DTMINPTH[15:0]																Init	00E5		

Notes:

1. Any register not listed is reserved and must not be written.
2. Only positive input values are valid for these RAM addresses.
3. Si3225 only.
4. Si3220 only.
5. For the Si3220, the RINGFRHI RAM address location is used to store the high byte of the internal ringing signal frequency. For the Si3225, this address location stores the desired time delay between when the relay opens and when the LFS register transitions out of the ringing state.
6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Example Hex	Example Dec	Unit
108	DTROW0TH	DTMF Row 0 Peak Threshold	DTROW0TH[15:3]																Init	2AE1		
109	DTROW1TH	DTMF Row 1 Peak Threshold	DTROW1TH[15:3]																Init	28FB		
117	DTROW2HTH	DTMF Row Second Harmonic Threshold	DTROW2HTH[15:3]																Init	308C		
110	DTROW2TH	DTMF Row 2 Peak Threshold	DTROW2TH[15:3]																Init	25C2		
111	DTROW3TH	DTMF Row 3 Peak Threshold	DTROW3TH[15:3]																Init	249B		
115	DTROWRTH	DTMF Row Ratio Threshold	DTROWRTH[15:3]																Init	0CC5		
114	DTRTWTH	DTMF Reverse Twist Threshold	DTRTWTH[15:3]																Init	1013		
Echo Cancellation																						
89	ECCO0	Echo Cancellation Coeff 0	ECCO0[15:3]																Init	01B0	1728	
82	ECCO1	Echo Cancellation Coeff 1	ECCO1[15:3]																Init	FF20	–896	
83	ECCO2	Echo Cancellation Coeff 2	ECCO2[15:3]																Init	1548	21792	
84	ECCO3	Echo Cancellation Coeff 3	ECCO3[15:3]																Init	1E38	30944	
85	ECCO4	Echo Cancellation Coeff 4	ECCO4[15:3]																Init	1238	18656	
86	ECCO5	Echo Cancellation Coeff 5	ECCO5[15:3]																Init	01B8	1760	
87	ECCO6	Echo Cancellation Coeff 6	ECCO6[15:3]																Init	FD08	–3040	
88	ECCO7	Echo Cancellation Coeff 7	ECCO7[15:3]																Init	FFA0	–384	
92	ECIIRA1	Echo Cancel IIR Filter Coeff A1	ECIIRA1[15:3]																Init	0370	3520	
93	ECIIRA2	Echo Cancel IIR Filt Coeff A2	ECIIRA2[15:3]																Init	CB58	–53920	
90	ECIIRB0	Echo Cancel IIR Filt Coeff B0	ECIIRB0[15:3]																Init	0068	416	
91	ECIIRB1	Echo Cancel IIR Filt Coeff B1	ECIIRB1[15:3]																Init	FEA0	–1408	
FSK Generation																						
102	FSKAMP0	FSK Amplitude for Space	FSKAMP0[15:3]																Init	0100	.22	V_{rms}
103	FSKAMP1	FSK Amplitude for Mark	FSKAMP1[15:3]																Init	01E0	.22	V_{rms}
100	FSKFREQ0	FSK Frequency for Space	FSKFREQ0[15:3]																Init	3CE0	1200	Hz
101	FSKFREQ1	FSK Frequency for Mark	FSKFREQ1[15:3]																Init	35B0	2200	Hz
104	FSK01HI	FSK 0-1 Transition Freq—High	FSK01HI[15:3]																Init	3BE0		
105	FSK01LO	FSK 0-1 Transition Frequency—Low	FSK01LO[15:3]																Init	1330		
106	FSK10HI	FSK 1-0 Transition Frequency—High	FSK10HI[15:3]																Init	1118		
107	FSK10LO	FSK 1-0 Transition Frequency—Low	FSK10LO[15:3]																Init	1D88		

Notes:

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3. Si3225 only.
4. Si3220 only.
5. For the Si3220, the RINGFRHI RAM address location is used to store the high byte of the internal ringing signal frequency. For the Si3225, this address location stores the desired time delay between when the relay opens and when the LFS register transitions out of the ringing state.
6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Example Hex	Example Dec	Unit
Loop Currents																						
9	ILONG	Longitudinal Current Sense Value	ILONG[15:0][2]																DIag			mA
8	ILOOP	Loop Current Sense Value	ILOOP[15:0][2]																Diag			mA
18	IRING	Q5 Current Measurement	IRING[15:0]																Diag			mA
16	IRINGN	Q3 Current Measurement	IRINGN[15:0]																Diag			mA
15	IRINGP	Q2 Current Measurement	IRINGP[15:0]																Diag			mA
21	IRNGNG	External Ringing Generator Current Measurement	IRNGNG[15:0][3]																Diag			mA
19	ITIP	Q6 Current Measurement	ITIP[15:0]																Diag			mA
17	ITIPN	Q4 Current Measurement	ITIPN[15:0]																Diag			mA
14	ITIPP	Q1 Current Measurement	ITIPP[15:0]																Diag			mA
Loop Closure Detection																						
24	LCRDBI	Loop Closure Detection Debounce Interval	LCRDBI[15:0][2]																Init	000C	15	ms
25	LCRLPF	Loop Closure Filter Coefficient	LCRLPF[15:3]																Init	0A10	10	Hz
26	LCRMASK	Loop Closure Mask Interval Coeff	LCRMASK[15:0][2]																Init	0040	80	ms
166	LCRMSKPR	LCR Mask During Polarity Reversal	LCRMSKPR[15:0]																Init	0040	80	ms
22	LCROFFHK	Off-Hook Detect Threshold	LCROFFHK[15:0][2]																Init	0C0C	10	mA
23	LCRONHK	On-Hook Detect Threshold	LCRONHK[15:0][2]																Init	0DEO	11	mA
Longitudinal Current Detection																						
29	LONGDBI	Ground Key Detection Debounce Interval	LONGDBI[15:0][2]																Init			ms
27	LONGHITH	Ground Key Detection Threshold	LONGHITH[15:0][2]																Init	08D4	7	mA
28	LONGLOTH	Ground Key Removal Detection Threshold	LONGLOTH[15:0][2]																Init	0A17	8	mA
30	LONGLPF	Ground Key Filter Coefficient	LONGLPF[15:3]																Init	0A08	10	Hz
Oscillator Coefficients																						
95	OSC1AMP	Oscillator 1 Amplitude	OSC1AMP[15:0]																Init	004F	0.0775	V_{rms}
94	OSC1FREQ	Oscillator 1 Frequency	OSC1FREQ[15:3]																Init	3D98	350	Hz
96	OSC1PHAS	Oscillator 1 Initial Phase	OSC1PHAS[15:0]																Init	0000		
98	OSC2AMP	Oscillator 2 Amplitude	OSC2AMP[15:0]																Init	0063	0.0775	V_{rms}
97	OSC2FREQ	Oscillator 2 Frequency	OSC2FREQ[15:3]																Init	3C38	440	Hz
99	OSC2PHAS	Oscillator 2 Initial Phase	OSC2PHAS[15:0]																Init	0000		
Power Calculations																						

Notes:

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6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Example Hex	Example Dec	Unit
40	PLPFQ12	Q1/Q2 Thermal Low Pass Filter Coeff	PLFPQ12[15:3]																Init	0008	.3	s
41	PLFPQ34	Q3/Q4 Thermal Low Pass Filter Coeff	PLFPQ34[15:3]																Init	0008	.3	s
42	PLFPQ56	Q5/Q6 Thermal Low Pass Filter Coeff	PLFPQ56[15:3]																Init	0008	.3	s
Pulse Metering																						
68	PMAMPL	Pulse Metering Amplitude	PMAMPL[15:0][4]																Init	4000	65536	V
70	PMAMPTH	Pulse Metering AGC Amplitude Threshold	PMAMPTH[15:0][4]																Init	00C8	798	V
67	PMFREQ	Pulse Metering Frequency	PMFREQ[15:3][4]																Init	0000	0	Hz
69	PMRAMP	Pulse Metering Ramp Rate	PMRAMP[15:0][4]																Init	008A	550	s
Power Calculations																						
44	PQ1DH	Q1 Calculated Power	PQ1DH[15:0]																Diag			W
45	PQ2DH	Q2 Calculated Power	PQ2DH[15:0]																Diag			W
46	PQ3DH	Q3 Calculated Power	PQ3DH[15:0]																Diag			W
47	PQ4DH	Q4 Calculated Power	PQ4DH[15:0]																Diag			W
48	PQ5DH	Q5 Calculated Power	PQ5DH[15:0]																Diag			W
49	PQ6DH	Q6 Calculated Power	PQ6DH[15:0]																Diag			W
50	PSUM	Total Calculated Power	PSUM[15:0]																Diag			W
37	PTH12	Q1/Q2 Power Threshold	PTH12[15:0][2]																Init	0007	.22	W
38	PTH34	Q3/Q4 Power Threshold	PTH34[15:0][2]																Init	003C	17	W
39	PTH56	Q5/Q6 Power Threshold	PTH56[15:0][2]																Init	002A	1.28	W
43	RB56	Q5/Q6 Base Resistor	RB56[15:0]																Init			Ω
Ringing																						
59	RINGAMP	Ringing Amplitude/Zero Crossing Delay	RINGAMP[15:0][6]/ZERDELAY[15:0]																Init	00D5	47	Vrms
57	RINGFRHI	Ringing Frequency—High Byte/Linefeed Status Delay		RINGFRHI[14:3][5]/LFSDELAY[14:3]															Init	3F78	20	Hz
58	RINGFRLO	Ringing Frequency—Low Byte		RINGFRLO[14:3][4]															Init	6CE8	20	Hz
56	RINGOF	Ringing Waveform DC Offset	RINGOF[15:0][4]																Init	0000	0	V
60	RINGPHAS	Ringing Oscillator Initial Phase	RINGPHAS[15:3][4]																Init	0000		
Ring Trip Detection																						
66	RTACDB	AC Ring Trip Debounce Interval	RTACDB[15:0]																Init	0008	10	ms
64	RTACTH	AC Ring Trip Detect Threshold	RTACTH[15:0]																Init	1086		mA
61	RTCOUNT	Ring Trip Timeout Counter	RTCOUNT[15:0]																Init	0400	128	ms

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6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Example Hex	Example Dec	Unit
65	RTDCDB	DC Ring Trip Debounce Interval	RTDCDB[15:0]																Init	0008	10	ms
62	RTDCTH	DC Ring Trip Detect Threshold	RTDCTH[15:0]																Init	7FFF		mA
63	RTPER	Ring Trip Low Pass Filter Coeff Period	RTPER[15:0]																Init	0028	20	Hz
Receive Path Gain and Filters																						
81	RXIIRPOL	RX IIR Filter Pole Coeff	RXIIRPOL[15:3]																Init	3CCC	62256	
80	RXEQCO0	RX Equalizer Coeff 0	RXEQCO0[15:3]																Init	4000	65536	
79	RXEQCO1	RX Equalizer Coeff 1	RXEQCO1[15:3]																Init	0000	0	
78	RXEQCO2	RX Equalizer Coeff 2	RXEQCO2[15:3]																Init	0000	0	
77	RXEQCO3	RX Equalizer Coeff 3	RXEQCO3[15:3]																Init	0000	0	
71	RXGAIN	RX Gain Setting	RXGAIN[15:3]																Init	4000	1	
123	RXMODPWR	RX Path Modem Tone Power	RXMODPWR[15:3]																Init			
121	RXPWR	RX Path Input Signal Power	RXPWR[15:0]																Init			
DC Speedup																						
168	SPEEDUP	DC Speedup Timer	SPEEDUP[15:0]																Init	0000	60	ms
Test Diagnostic Filters																						
132	TESTA1H1	TX Diag Filter Coeff A1H1	TESTA1H1[15:3]																Diag			
142	TESTA1H2	TX Diag Filter Coeff A1H2	TESTA1H2[15:3]																Diag			
152	TESTA1H3	TX Diag Filter Coeff A1H3	TESTA1H3[15:3]																Diag			
131	TESTA1L1	TX Diag Filter Coeff A1L1	TESTA1L1[15:3]																Diag			
141	TESTA1L2	TX Diag Filter Coeff A1L2	TESTA1L2[15:3]																Diag			
151	TESTA1L3	TX Diag Filter Coeff A1L3	TESTA1L3[15:3]																Diag			
134	TESTA2H1	TX Diag Filter Coeff A2H1	TESTA2H1[15:3]																Diag			
144	TESTA2H2	TX Diag Filter Coeff A2H2	TESTA2H2[15:3]																Diag			
154	TESTA2H3	TX Diag Filter Coeff A2H3	TESTA2H3[15:3]																Diag			
133	TESTA2L1	TX Diag Filter Coeff A2L1	TESTA2L1[15:3]																Diag			
143	TESTA2L2	TX Diag Filter Coeff A2L2	TESTA2L2[15:3]																Diag			
153	TESTA2L3	TX Diag Filter Coeff A2L3	TESTA2L3[15:3]																Diag			
156	TESTAVO	TX Diag Filter Avg Output	TESTAVO[15:0]																Diag			V
158	TESTAVBW	TX Diag Filter Avg Bandwidth	TESTAVBW[15:3]																Diag			
160	TESTAVFL	TX Diag Filter Average Flag	TESTAVFL[15:3]																Diag			

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6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Example Hex	Example Dec	Unit
162	TESTAVTH	TX Diag Filter Avg Threshold	TESTAVTH[15:3]																Diag			
126	TESTB0H1	TX Diag Filter Coeff B0H1	TESTB0H1[15:3]																Diag			
136	TESTB0H2	TX Diag Filter Coeff B0H2	TESTB1H2[15:3]																Diag			
146	TESTB0H3	TX Diag Filter Coeff B0H3	TESTB0H3[15:3]																Diag			
125	TESTB0L1	TX Diag Filter Coeff B0L1	TESTB0L1[15:3]																Diag			
135	TESTB0L2	TX Diag Filter Coeff B0L2	TESTB0L2[15:3]																Diag			
145	TESTB0L3	TX Diag Filter Coeff B0L3	TESTB0L3[15:3]																Diag			
128	TESTB1H1	TX Diag Filter Coeff B1H1	TESTB1H1[15:3]																Diag			
138	TESTB1H2	TX Diag Filter Coeff B1H2	TESTB1H2[15:3]																Diag			
148	TESTB1H3	TX Diag Filter Coeff B1H3	TESTB1H3[15:3]																Diag			
127	TESTB1L1	TX Diag Filter Coeff B1L1	TESTB1L1[15:3]																Diag			
137	TESTB1L2	TX Diag Filter Coeff B1L2	TESTB1L2[15:3]																Diag			
147	TESTB1L3	TX Diag Filter Coeff B1L3	TESTB1L3[15:3]																Diag			
130	TESTB2H1	TX Diag Filter Coeff B2H1	TESTB2H1[15:3]																Diag			
140	TESTB2H2	TX Diag Filter Coeff B2H2	TESTB2H2[15:3]																Diag			
150	TESTB2H3	TX Diag Filter Coeff B2H3	TESTB2H3[15:3]																Diag			
129	TESTB2L1	TX Diag Filter Coeff B2L1	TESTB2L1[15:3]																Diag			
139	TESTB2L2	TX Diag Filter Coeff B2L2	TESTB2L2[15:3]																Diag			
149	TESTB2L3	TX Diag Filter Coeff B2L3	TESTB2L3[15:3]																Diag			
159	TESTPKFL	TX Diag Filter Peak Flag	TESTPKFL[15:3]																Diag			
155	TESTPKO	TX Diag Filter Peak Output	TESTPKO[15:3]																Diag			V
161	TESTPKTH	TX Diag Filter Peak Threshold	TESTPKTH[15:3]																Diag			
157	TESTWLN	TX Diag Filter	TESTWLN[15:3]																Diag			
Transmit Path Gain and Filters																						
76	TXEQCO0	TX Equalizer Coefficient 0	TXEQCO0[15:3]																Init	4A6A	76201	
75	TXEQCO1	TX Equalizer Coefficient 1	TXEQCO1[15:3]																Init	F84C	–7888	
74	TXEQCO2	TX Equalizer Coefficient 2	TXEQCO2[15:3]																Init	012C	1199	
73	TXEQCO3	TX Equalizer Coefficient 3	TXEQCO3[15:3]																Init	004C	302	
72	TXGAIN	TX Gain Setting	TXGAIN[15:3]																Init	4000	1	
163	TXHPF1	TX HPF Coefficient 1	TXHPF1[15:3]																Diag			
164	TXHPF2	TX HPF Coefficient 2	TXHPF2[15:3]																Diag			
165	TXHPF3	TX HPF Coefficient 3	TXHPF3[15:3]																Diag			

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6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.

RAM Addr	Mnemonic	Description	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type	Example Hex	Example Dec	Unit
124	TXMODPWR	TX Path Modem Tone Power	TXMODPWR[15:3]																Init			
122	TXPWR	TX Path Input Signal Power	TXPWR[15:0]																Init			
Loop Voltages																						
13	VBAT	Scaled Battery Voltage Measurement	VBAT[15:0]																Diag			V
4	VCM	Common Mode Voltage		VCM[14:0][2]															Init	0268	3	V
7	VLOOP	Loop Voltage	VLOOP[15:0][2]																Diag			V
0	VOC	Open Circuit Voltage		VOC[14:0][2]															Init	2668	48	V
1	VOCDELTA	VOC Delta for Off-Hook		VOCDELTA[14:0][2]															Init	059A	7	V
3	VOCHTH	VOC Delta Upper Threshold	VOCHTH[15:0][2]																Init	0198	2	V
2	VOCLTH	VOC Delta Lower Threshold	VOCLTH[15:0]																Init	F9A2	–8	V
10	VOCTRACK	Battery Tracking Open Circuit Voltage	VOCTRACK[15:0][2]																Diag			V
5	VOV	Overhead Voltage		VOV[14:0][2]															Init	0334	4	V
6	VOVRING	Ringing Overhead Voltage		VOVRING[14:0][2]															Init	0000	0	V
12	VRING	Scaled RING Voltage Measurement	VRING[15:0]																Diag			V
20	VRNGNG	External Ringing Generator Voltage Measurement		VRNGNG[14:7][3]															Diag			V
11	VTIP	Scaled TIP Voltage Measurement	VTIP[15:0]																Diag			V

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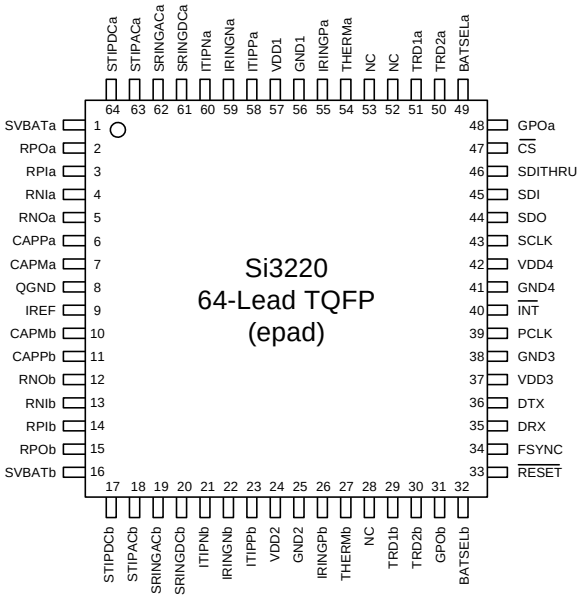
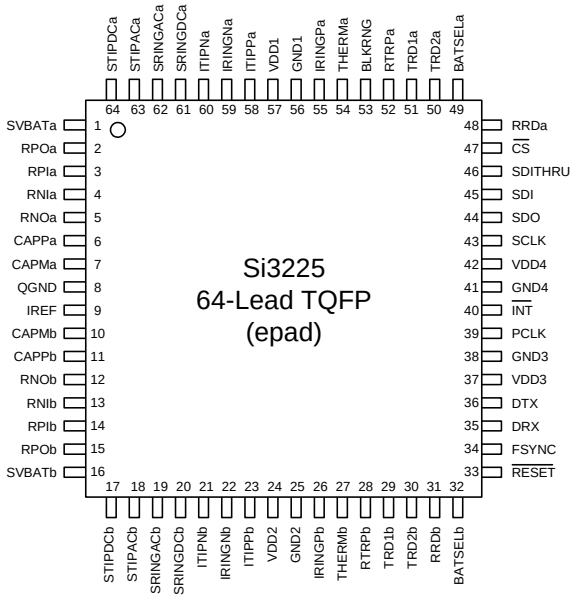
6. For the Si3220, the RINGAMP RAM address location is used to store the amplitude of the internal ringing signal. For the Si3225, this address location stores the desired time relay between the last zero current crossing and the next opportunity to open the ringing relay.
7. RAM address in decimal.

Pin Descriptions: Si3220/25





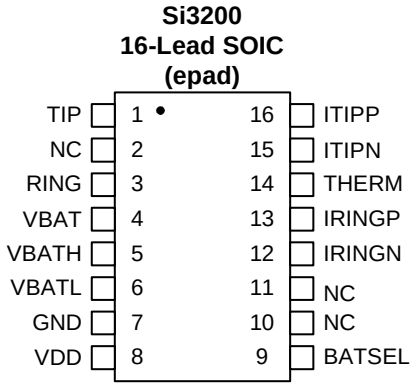
Pin Number(s)		Symbol	Input/ Output	Description
Si3220	Si3225			
1, 16	1, 16	SVBATa, SVBATb	I	**Battery Sensing Input.** Analog current input used to sense battery voltage.
2,15	2,15	RPOa, RPOb	O	**Transconductance Amplifier External Resistor Connection.**
3, 14	3, 14	RPIa, RPIb	I	**Transconductance Amplifier External Resistor Connection.**
4, 13	4, 13	RNIa, RNIb	I	**Transconductance Amplifier Resistor Connection.**
5, 12	5, 12	RNOa, RNOb	O	**Transconductance Amplifier Resistor Connection.**
6, 11	6, 11	CAPPa, CAPPb		**Differential Capacitor.** Capacitor used in low pass filter to stabilize SLIC feedback loops.
7, 10	7, 10	CAPMa, CAPMb		**Common Mode Capacitor.** Capacitor used in low pass filter to stabilize SLIC feedback loops.
8	8	QGND		**Component Reference Ground.** Return path for differential and common mode capacitors. Do not connect to system ground.

Pin Number(s)		Symbol	Input/ Output	Description
Si3220	Si3225			
9	9	IREF	I	**IREF Current Reference.** Connects to an external resistor to provide a high accuracy reference current. Return path for IREF resistor should be routed to QGND pin.
17, 64	17, 64	STIPDCb, STIPDCa	I	**TIP Sense.** Analog current input senses dc voltage on TIP side of subscriber loop.
18, 63	18, 63	STIPACb, STIPACa	I	**TIP Transmit Input.** Analog input senses ac voltage on TIP side of subscriber loop.
19, 62	19, 62	SRINGACb, SRINGACa	I	**RING Transmit Input.** Analog input senses ac voltage on RING side of subscriber loop.
20, 61	20, 61	SRINGDCb, SRINGDCa	I	**RING Sense.** Analog current input senses dc voltage on RING side of subscriber loop.
21, 60	21, 60	ITIPNb, ITIPNa	O	**Negative TIP Current Control.** Analog current output provides dc current return path to V_{BAT} from TIP side of the loop.
22, 59	22, 59	IRINGNb, IRINGNa	O	**Negative RING Current Control.** Analog current output provides dc current return path to V_{BAT} from RING side of loop.
23, 58	23, 58	ITIPPb, ITIPPa	O	**Positive TIP Current Control.** Analog current output drives dc current onto TIP side of subscriber loop in normal polarity. Also modulates ac current onto TIP side of loop.
24, 37, 42, 57	24, 37, 42, 57	VDD2,VDD3, VDD4,VDD1		**Supply Voltage.** Power supply for internal analog and digital circuitry. Connect all VDD pins to the same supply and decouple to adjacent GND pin as close to the pins as possible.
25, 38, 41, 56	25, 38, 41, 56	GND2,GND3, GND4,GND1		**Ground.** Ground connection for internal analog and digital circuitry. Connect all pins to low-impedance ground plane.
26, 55	26, 55	IRINGPb, IRINGPa	O	**Positive RING Current Control.** Analog current output drives dc current onto RING side of subscriber loop in reverse polarity. Also modulates ac current onto RING side of loop.
27,54	27,54	THERMb, THERMa	I	**Temperature Sensor.** Senses Internal temperature of Si3200.
29, 51	29, 51	TRD1b, TRD1a	O	**Test Relay Driver Output.** Drives test relays for connecting loop test equipment.
28, 52, 53		NC		**No Internal Connection.** Leave unconnected or connect to ground plane.

Pin Number(s)		Symbol	Input/ Output	Description
Si3220	Si3225			
	28, 52	RTRPb, RTRPa	I	**External Ring Trip Sensing Input.** Used to sense ring-trip condition when using centralized ring generator. Connect to low side of ring sense resistor.
30, 50	30, 50	TRD2b, TRD2a	O	**Test Relay Driver Output.** Drives test relays for connecting loop test equipment.
	31, 48	RRDb, RRDa	O	**Ring Relay Driver Output.** Connects an external centralized ring generator to the subscriber loop.
31, 48		GPOb, GPOa	O	**General Purpose Output Driver.** Used as a relay driver or as a second battery select pin when using a third battery supply.
32, 49	32, 49	BATSELb, BATSELa	O	**Battery Voltage Select Pin.** Switches between high and low external battery supplies.
35	35	DRX	I	**Receive PCM Data.** Input data from PCM/GCI bus.
36	36	DTX	O	**Transmit PCM Data.** Output data to PCM/GCI bus.
39	39	PCLK	I	**PCM Bus Clock.** Clock input for PCM/GCI bus timing.
33	33	$\overline{\text{RESET}}$	I	**Reset.** Active low. Hardware reset used to place all control registers in known state. An internal pulldown resistor asserts this pin low when not driven externally.
34	34	FSYNC	I	**Frame Sync.** 8 kHz frame synchronization signal for PCM/GCI bus. May be short or long pulse format.
40	40	$\overline{\text{INT}}$	O	**Interrupt.** Maskable interrupt output. Open drain output for wire-ORed operation.
43	43	SCLK	I	**Serial Port Bit Clock Input.** Controls serial data on SDO and latches data on SDI.
44	44	SDO	O	**Serial Port Data Out.** Serial port control data output.
45	45	SDI	I	**Serial Port Data In.** Serial port control data input.
46	46	SDITHRU	O	**Serial Data Daisy Chain.** Enables multiple devices to use a single CS for serial port control. Connect SDITHRU pin from master device to SDI pin of slave device. An internal pullup resistor holds this pin high during idle periods.

Pin Number(s)		Symbol	Input/ Output	Description
Si3220	Si3225			
47	47	$\overline{CS}$	I	**Chip Select.** Active low. When inactive, SCLK and SDI are ignored and SDO is high impedance. When active, serial port is operational.
	53	BLKRNG	I	**Ring Generator Sensing Input.** Senses ring-trip condition when using centralized ring generator. Connect to high side of ring sense resistor. Shared by channel a and b.
epad	epad	GND		**Exposed Die Paddle Ground.** Connect to a low-impedance ground plane via top side PCB pad directly under the part. See Package Outlines: 64-Pin TQFP for PCB pad dimensions.

Pin Descriptions: Si3200



Pin #(s)	Symbol	Input/ Output	Description
1	TIP	I/O	**TIP Output.** Connect to the TIP lead of the subscriber loop.
2, 10, 11	NC	—	**No Internal Connection.** Do not connect to any electrical signal.
3	RING	I/O	**RING Output.** Connect to the RING lead of the subscriber loop.
4	VBAT	—	**Operating Battery Voltage.** Si3200 internal system battery supply. Connect SVBATa/b pin from Si3220/25 and decouple with a 0.1 μF/100 V filter capacitor.
5	VBATH	—	**High Battery Voltage.** Connect to the system ringing battery supply. Decouple with a 0.1 μF/100 V filter capacitor.
6	VBATL	—	**Low Battery Voltage.** Connect to lowest system battery supply for off-hook operation driving short loops. An internal diode prevents leakage current when operating from VBATH.
7	GND	—	**Ground.** Connect to a low-impedance ground plane.
8	VDD	—	**Supply Voltage.** Main power supply for all internal circuitry. Connect to a 3.3 V or 5 V supply. Decouple locally with a 0.1 μF/10 V capacitor.
9	BATSEL	I	**Battery Voltage Select.** Connect to the BATSEL pin of the Si3220 or Si3225 through an external resistor to enable automatic battery switching. No connection is required when used with the Si3225 in a single battery system configuration.

Pin #(s)	Symbol	Input/ Output	Description
12	IRINGN	I	**Negative RING Current Control.** Connect to the IRINGN lead of the Si3220 or Si3225.
13	IRINGP	I	**Positive RING Current Drive.** Connect to the IRINGP lead of the Si3220 or Si3225.
14	THERM	O	**Thermal Sensor.** Connection to internal temperature sensing circuit. Connect to THERM pin of Si3220 or Si3225.
15	ITIPN	I	**Negative TIP Current Control.** Connect to the ITIPN lead of the Si3220 or Si3225.
16	ITIPP	I	**Positive TIP Current Control.** Connect to the ITIPP lead of the Si3220 or Si3225.
epad	GND		**Exposed Die Paddle Ground.** For adequate thermal management, the exposed die paddle should be soldered to a PCB pad that is connected to low-impedance inner and/or backside ground planes using multiple vias. See “Package Outline: 16-Pin SOIC” for PCB pad dimensions.

Dual ProSLIC Selection Guide

Part Number	Description	On-Chip Ringing	External Ringing Support	Pulse Metering	Temp Range	Package
Si3200-KS	Linefeed interface				0 to 70 °C	SOIC-16
Si3200-BS	Linefeed interface				–40 to 85 °C	SOIC-16
Si3220-KQ	Dual ProSLIC	•		•	0 to 70 °C	TQFP-64
Si3220-BQ	Dual ProSLIC	•		•	–40 to 85 °C	TQFP-64
Si3225-KQ	Dual ProSLIC		•		0 to 70 °C	TQFP-64
Si3225-BQ	Dual ProSLIC		•		–40 to 85 °C	TQFP-64

Package Outline: 64-Pin TQFP

Figure 65 illustrates the package details for the Dual ProSLIC. Table 48 lists the values for the dimensions shown in the illustration.

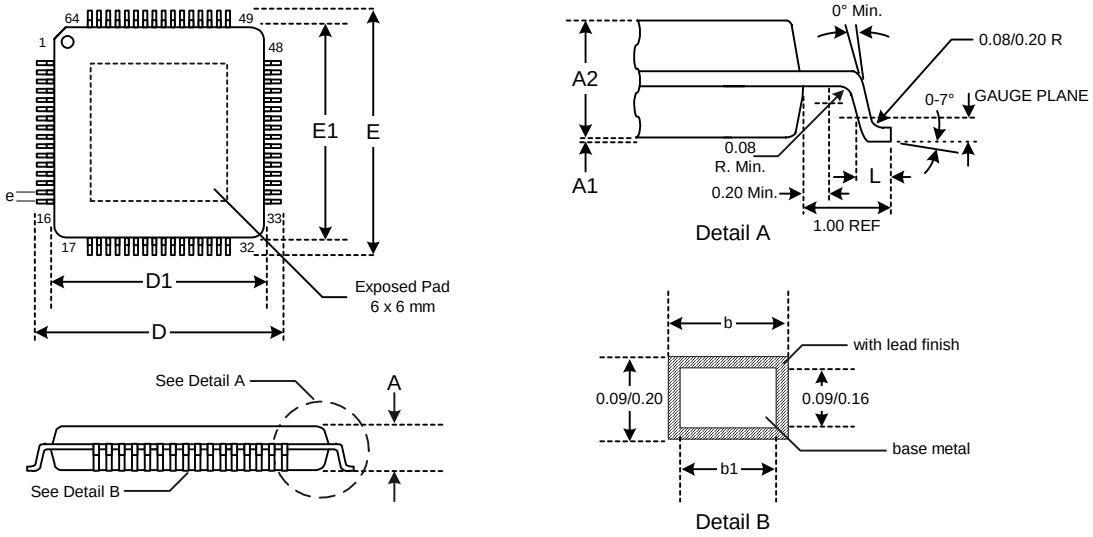


Figure 65. 64-Pin Thin Quad Flat Package (TQFP)

Table 48. 64-Pin Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
L	0.45	0.60	0.75
e		0.50 BSC	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23

Package Outline: 16-Pin SOIC

Figure 66 illustrates the package details for the Si3200. Table 49 lists the values for the dimensions shown in the illustration.

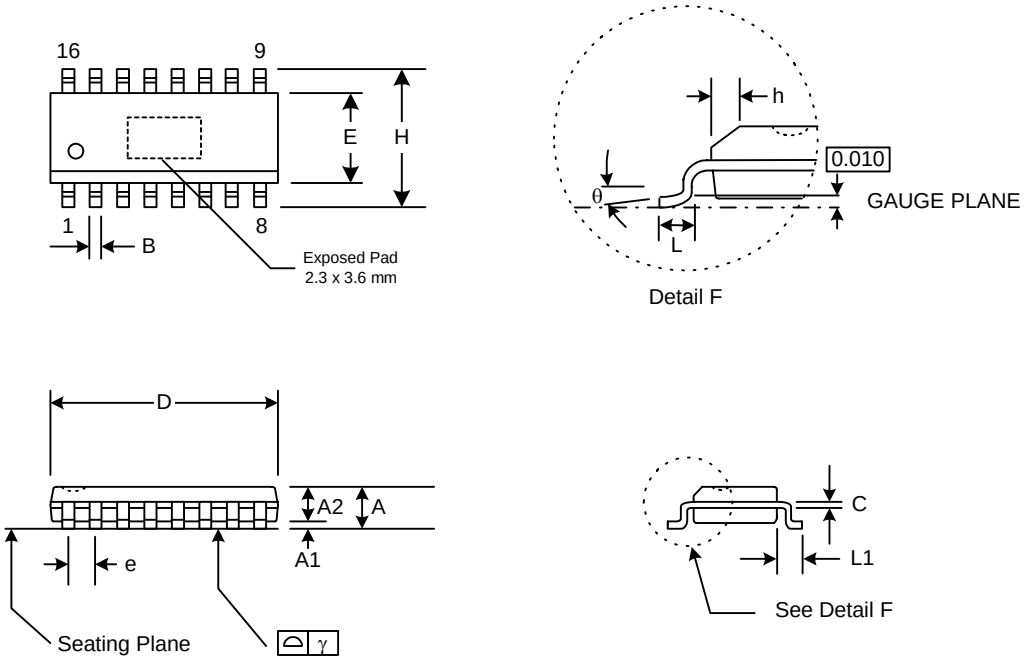


Figure 66. 16-Pin Small Outline Integrated Circuit (SOIC) Package

Table 49. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	.10	.25
A2	1.30	1.50
B	.33	.51
C	.19	.25
D	9.80	10.01
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	.25	.50
L	.40	1.27
L1	1.07 BSC	
γ	—	0.10
θ	0º	8º

Document Change List

Revision 0.9 to Revision 0.91

- Table 8 on page 12
  - TIP/RING Pulldown Transistor Saturation Voltage updated.
  - TIP/RING Pullup Transistor Saturation Voltage updated.
  - Note added.
- "Calculating Overhead Voltages" on page 27
  - Second paragraph updated.
- "Internal Trapezoidal Ringing" on page 42
  - RINGAMP equation updated.

Notes:

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