DTMF receiver for telephones

BU8872 / BU8872FS

The BU8872 and BU8872FS are DTMF receiver ICs developed for use in telephone answering machines, and convert 16 different types of DTMF signals into 4-bit binary serial data. In addition to a compact 8-pin DIP (BU8872) or 16-pin SSOP (BU8872FS) package, these receivers feature a wide dynamic range, eliminating the need for an external input amplifier. Expertise from a number of companies has been incorporated into these products to enable guard time control through a host microcomputer.

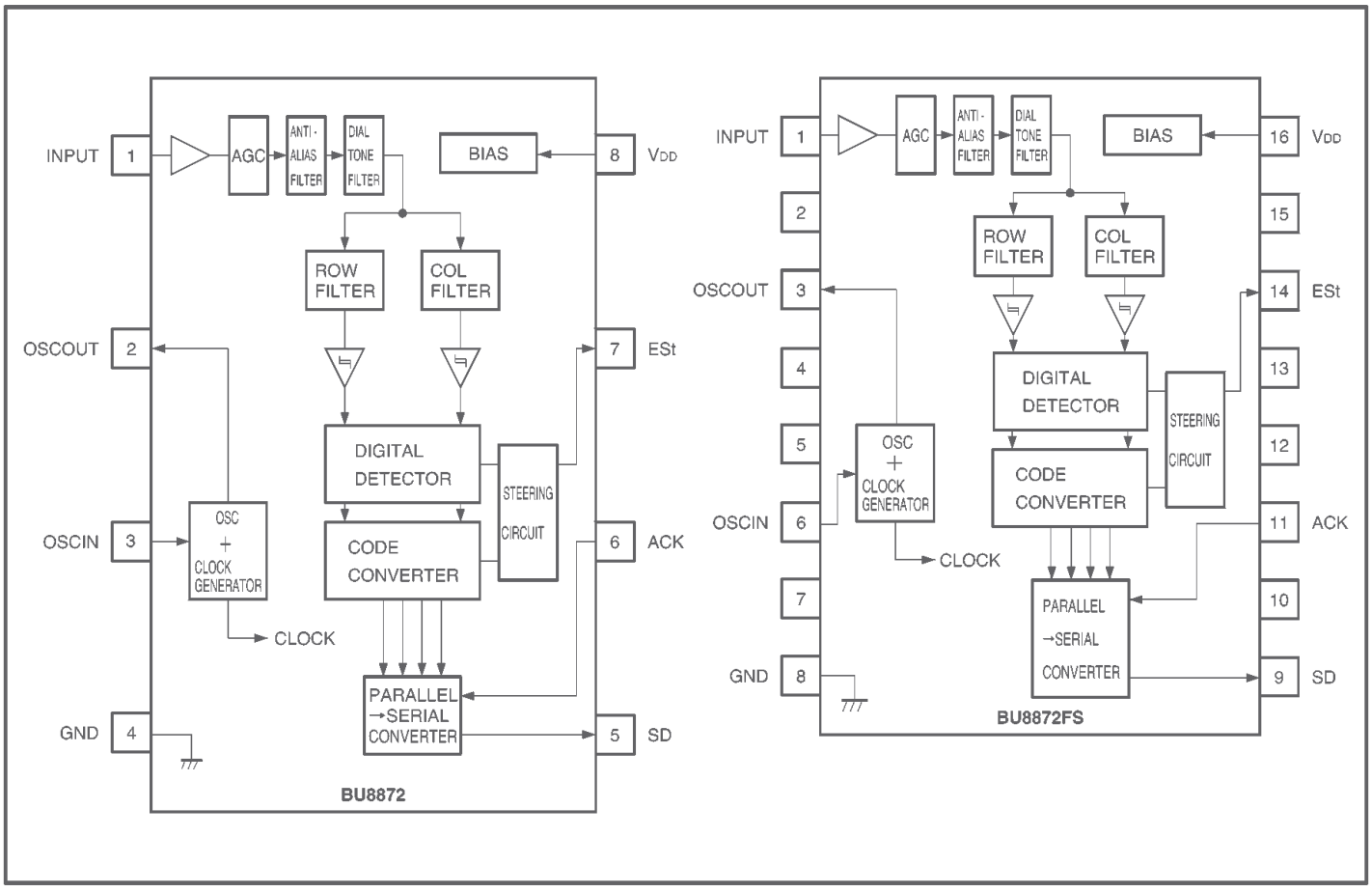
●Applications

Telephone answering machines

●Features

1) Dynamic range of 45dB. (internal AGC)
2) 4-bit binary serial data output.
3) Guard time can be controlled through host microcomputer.
4) Input pins equipped with hysteresis. (ACK pin)
5) 4.19MHz ceramic resonator or crystal resonator can be used.
6) 8-pin DIP package. (BU8872)
   16-pin SSOP package. (BU8872FS)

●Block diagram



●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage		V_{DD}	7	V
Input voltage		V_{IN}	GND−0.3～V_{DD}+0.3	V
Output voltage		V_{OUT}	GND−0.3～V_{DD}+0.3	V
Power dissipation	BU8872	Pd	500 *1	mW
	BU8872FS		650 *2	
Operating temperature		Topr	−40～+85	℃
Storage temperature		Tstg	−55～+125	℃

*1 Reduced by 5mW for each increase in Ta of 1℃ over 25℃.

*2 Reduced by 6.5mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	4.50～5.50	V
Oscillation frequency	fosc	4.194304	MHz
Oscillation frequency deviation	Δfosc	*3	%

*3 Recommended ceramic resonators:

MURATA MFG.:	CSA4.19MG CST4.19MGW213
Matsushita Electric:	EFOEN4194 EFOEC4194
TDK:	FCR4.19M5 FCR4.19MC5
KYOCERA:	KBR - 4.19MSK KBR - 4.19MKS
Fujitsu:	FAR - C4□B - 04194 - K00
ROHM:	SFR3AU 4194

●Electrical characteristics

DC characteristics (unless otherwise noted, Ta=25°C, V_{DD}=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply current	I_{DD}	1.0	3.4	4.4	mA	Operating state
Input high level voltage	V_{IH}	V_{DD}−0.8	−	V_{DD}	V	ACK pin
Input low level voltage	V_{IL}	GND	−	GND+0.8	V	ACK pin
Input high level current	I_{IH}	−	0.1	1.0	μA	ACK pin
Input low level current	I_{IL}	−	0.1	1.0	μA	ACK pin
Pin 1 input impedance	Z_{IH}	10	30	50	kΩ	ν in=dBm, fin=kHz
Output saturation high level voltage	V_{OH}	4.6	−	−	V	I_{OH}=0.4mA*4
Output saturation low level voltage	V_{OL}	−	−	0.4	V	I_{OL}=mA*4

AC characteristics (unless otherwise noted, Ta=25°C, V_{DD}=5.0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions	ν in (dBm)
Valid input level range		VIV	−42	−	3	dBm	*2, 3	−
Dual tone level difference	Positive	VTWP	−	−	6	dB	*3	−15
	Negative	VTWN	−	−	6	dB	*3	−15
Frequency detection		BWA	±1.5%±2Hz	−	−	−	*4	−27
Frequency rejection		BWR	−	−	±4	%	*4	−27
3rd tone tolerance		TTT	−	−	−6	dB	*4, 5	−27
Noise tolerance		TN	−	−12	−	dB		−27
Dial tone tolerance		TDT	−	14	7	dB	*6	−27
Signal presence detection time		tDP	5	12	20	ms		−27
Signal absence detection time		tDA	0.5	5	15	ms		−27
Data shift rate		fDS	−	−	1	MHz	ACK Duty 40～50%	−
Output delay time		tPAD	−	70	150	ns	ACK→SD	−
Setup time		tDL	0	−	−	ns		−
Hold time		tDH	30	60	−	ns		−

*1 Applies to ESt pin and SD pin.

*2 A DTMF signal is input, and the voltage level of the single tone component is set as VIV.

*3 Specified for a DTMF signal with a frequency deviation at the maximum standard frequency ±0.73%.

*4 No difference in level between the two tones.

*5 Composite signal consisting of DTMF signals and the third harmonics of each input.

*6 Specified for signals of 350 Hz and 440 Hz (±2%).

●Pin descriptions

Pin No. BU8872	Pin No. BU8872FS	Pin name	Function
1	1	INPUT	This is the audio signal input pin, and should be coupled.
2	3	OSCOUT	This is the output pin for the internal oscillator.
3	6	OSCIN	This is the input pin for the internal oscillator. Connect a 4.194304 MHz ceramic or crystal resonator between this pin and OSCOUT, or use input from an external oscillator.
4	8	GND	This is the ground pin.
5	9	SD	This is the serial data output pin. If a series of pulses is input to the ACK pin while the ESt pin is HIGH, the SD output pin outputs a 4-bit binary code corresponding to the DTMF signal shown in Table 1.
6	11	ACK	This is the acknowledgement pulse input pin. It is equipped with hysteresis. After the ESt pin goes HIGH, the four consecutive pulses input to the ACK pin cause the 4-bit data corresponding to the DTMF signal of the SD pin output to be output. The rising edge of the first pulse is latched before the data is shifted.
7	14	ESt	This is the steering signal output pin. When there is a valid DTMF signal, this pin goes HIGH.
8	16	V_{DD}	This is the power supply pin.
	2, 4, 5, 7, 10, 12, 13, 15	N.C.	This is the N.C. pin. It is not connected inside the IC.

●Input / output circuits

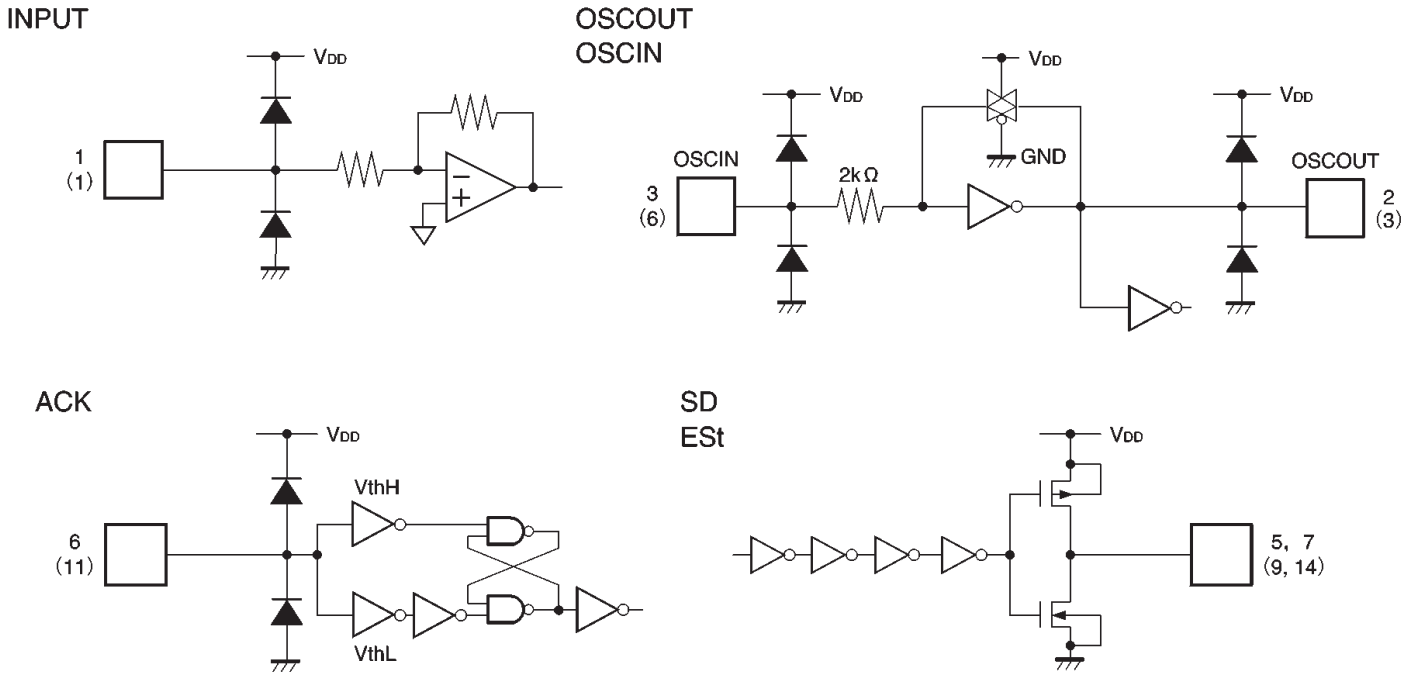


Fig.1

●Circuit operation

A DTMF signal is supplied to the INPUT pin and applied to a pair of 6th-order bandpass filters, which separate the DTMF signal into its high (COL) and low (ROW) frequencies. The separated tones are converted into square waves and fed to a digital detector. (See the block diagram.)

The digital detector checks the two tones to see if they are within the valid DTMF frequency bands. If they are, it sends a DETECT signal to the steering circuit, and sends the appropriate column and row address signals to a code converter.

The code converter encodes the received and detected DTMF signal, and outputs an ENABLE signal to the steering circuit.

Based on the DETECT and ENABLE signals, the steering circuit outputs an Early Steering (ESt) signal, which sets the ESt pin to HIGH, indicating that a valid DTMF signal has been detected.

If a series of pulses is input at the ACK pin while ESt is HIGH, a decoded DTMF signal is output to the SD pin as a binary code. (See Figure 2 for the overall timing.)

If a pulse sequence is input at the ACK pin, the data is latched at the rising edge of the first pulse by a parallel-serial converter, and at the same time, the LSB is output from the SD pin. Following this, three bits of data are output from the SD pin for each bit of each pulse in the pulse sequence input from the ACK pin. As a result, a total of four bits of data are output for the four pulses. (See Figure 3 for the ACK and SD timing.)

If the pulse sequence input to the ACK pin consists of three or fewer pulses, the next DTMF input cannot be decoded properly. Any ACK pulses in excess of four are ignored until ESt goes HIGH again.

Table 1 shows the format of serial data output from the SD pin.

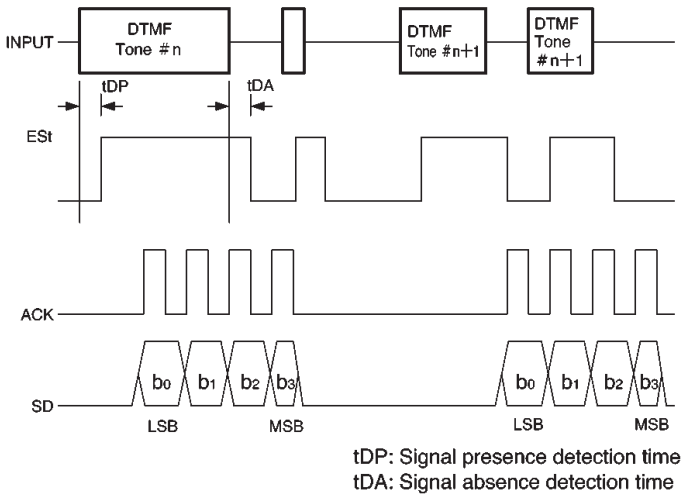


Fig 2 Overall timing chart

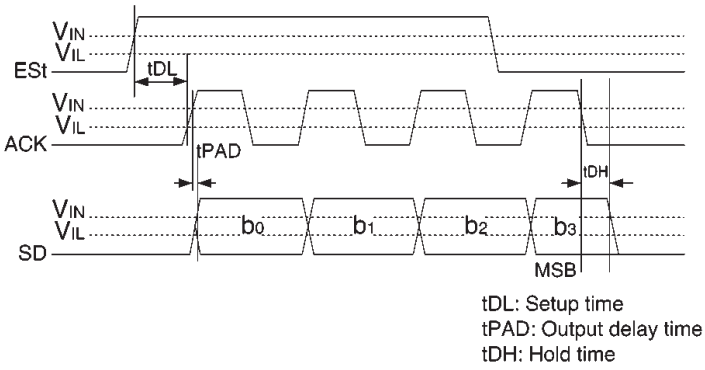


Fig. 3 ACK and SD timing

Table 1. Serial data correspondence table

ROW [Hz]	COL [Hz]	No.	b_3 (MSB)	b_2	b_1	b_0 (LSB)
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0= "L" level 1= "H" level

●Application example

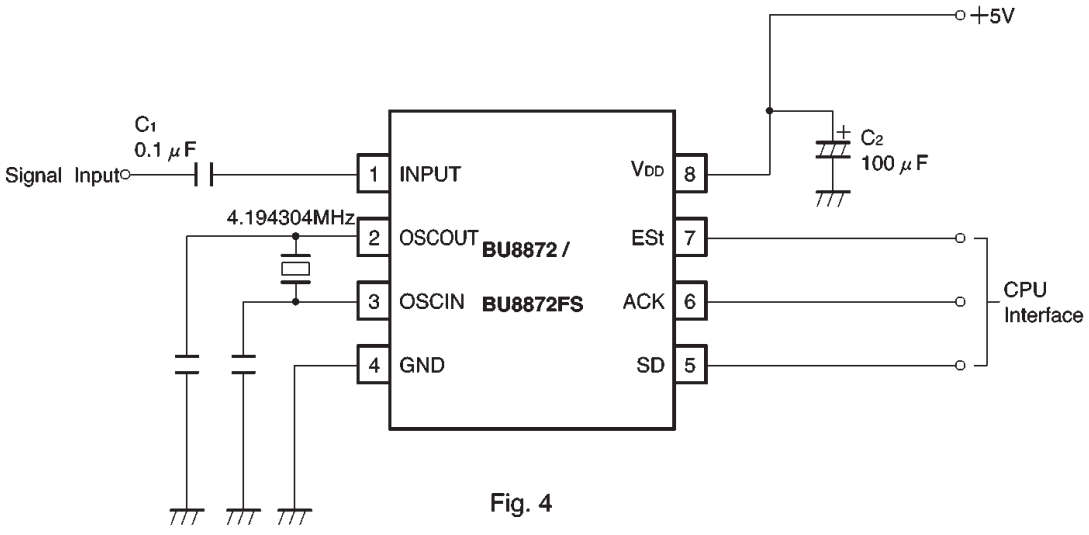


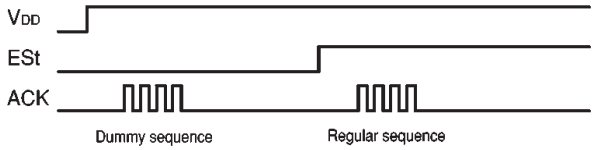
Fig. 4

●Operation notes

(1) To prevent latch-ups, we recommend inserting a bypass capacitor (a capacitor between V_{DD} and GND) close to the V_{DD} pin of the device.

(2) If using a pin-type ceramic resonator, connect a CH class capacitor between the OSCIN and OSCOUT pins and the GND.

(3) This LSI is not equipped with the power-on reset function. Also, since the internal circuit (flip-flop circuit) becomes unstable at the rising edge of the power supply, the internal circuit is initialized as shown below by the first DTMF sequence received after the rising edge of the power supply. Therefore, input four dummy ACK pulses before the DTMF reception.



●Selecting attached components

(1) Power supply components

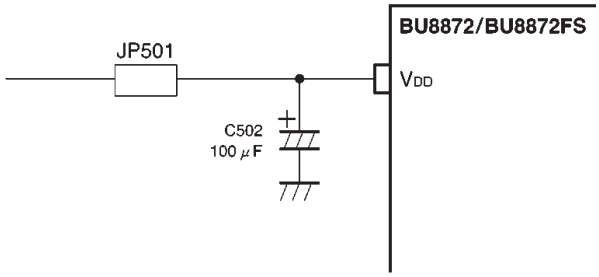


Fig. 5 Power supply circuit

C502 : This is the V_{DD} bypass capacitor, and is normally 100μF.

JP501 : This is normally shorted. To test the current consumption of the IC, insert a DC ammeter in place of JP501.

(2) Oscillation components

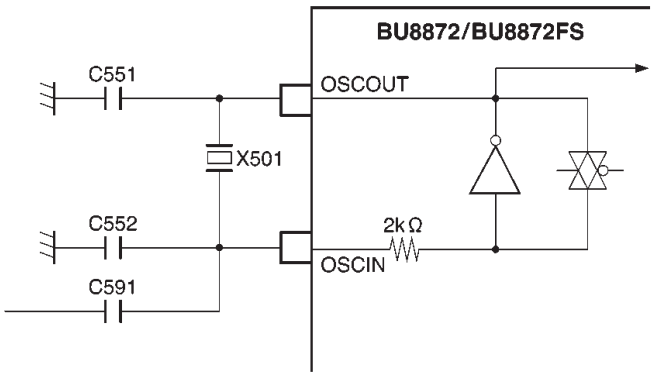


Fig. 6 Oscillation circuit

X501, C551, and C552 : Use a crystal or ceramic resonator with an oscillation frequency of 4.194304MHz. If using a ceramic resonator, there may be problems with the precision of the oscillation frequency, so we recommend using one of the ceramic resonators listed below.

	X501	C551	C552
Murata	CSA4.19MG	30pF	30pF
	CST4.19MGW213	(internal capacitors)	
Matsushita	EFOEN4194	33pF	33pF
	EFOEC4194	(internal capacitors)	
TDK	FCR4.19M5	33pF	33pF
	FCR4.19MC5	(internal capacitors)	
Kyocera	KBR-4.19MSK	33pF	33pF
	KBR-4.19MKS	(internal capacitors)	
Fujitsu	FAR-C4□	(internal capacitors)	
	B-04194-K00		
ROHM	SFR3AU 4194	(internal capacitors)	

C591 : If you are using a dedicated resonator designed for DTMF receivers, such as the X501, C551, or C552, capacitor C591 should be left open. If you are injecting an external clock, X501 should be omitted and capacitor C591 used in its place. Typically, this capacitor should be 47nF.

(3) DTMF input

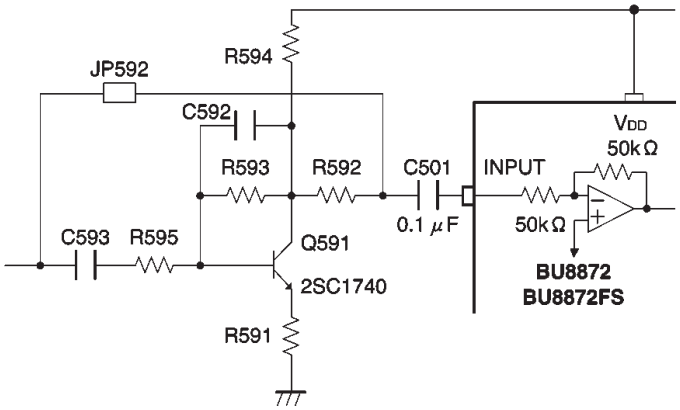


Fig. 7 DTMF input circuit

C501 : This is the DC blocking capacitor. Select a capacitor that will pass DTMF signals (greater than 697Hz) without significantly attenuating the signals.

JP592 : If DTMF signals are being input directly, both ends should be shorted.

C591
R591 ~ R595
C592, C593
Use these to increase the sensitivity of the DTMF receiver.

(4) ESt output

The ESt guard time is determined by the CPU of the host computer, but to reduce the load on the host computer, the guard time can be set using an external circuit, as shown below.

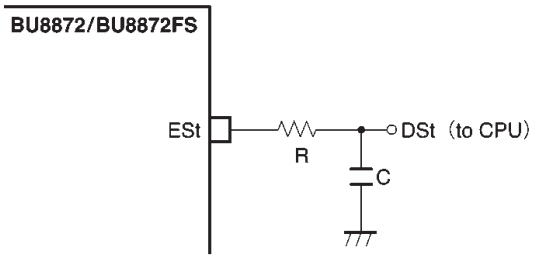


Fig. 8 Guard time setting circuit

The relation between a momentary falter in the ESt guard time (t_{GL}), a momentary HIGH level in the ESt guard time (t_{GH}), and the time constant is shown below. Figure 10 shows a timing diagram for guard times.

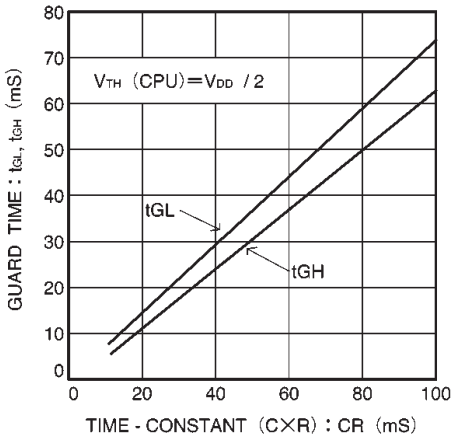


Fig. 9 Guard time vs. Time constant (C×R)

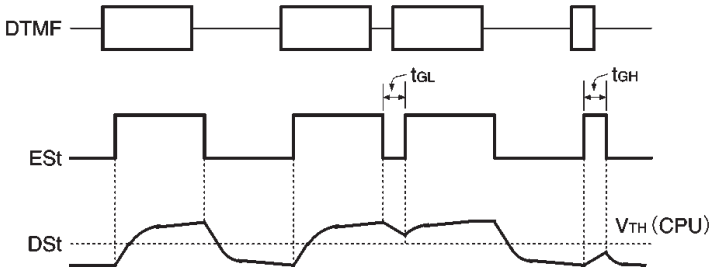


Fig. 10 Timing indicating guard times

●Electrical characteristic curves

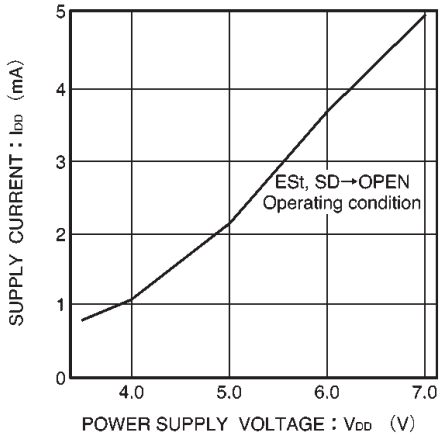


Fig. 11 Supply current vs. power supply voltage

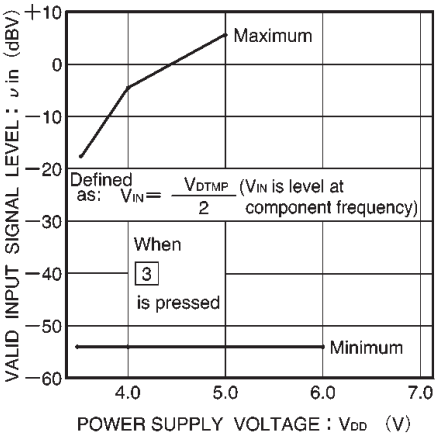


Fig. 12 Valid input level range vs. power supply voltage

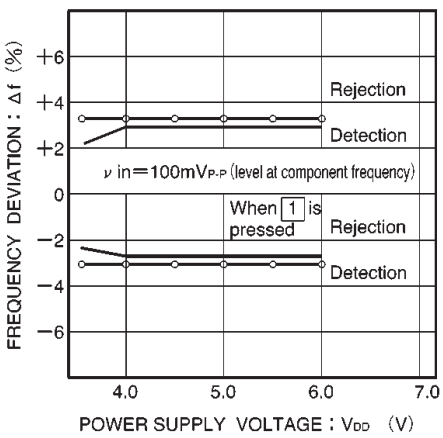


Fig. 13 Frequency detection/rejection ranges vs. power supply voltage

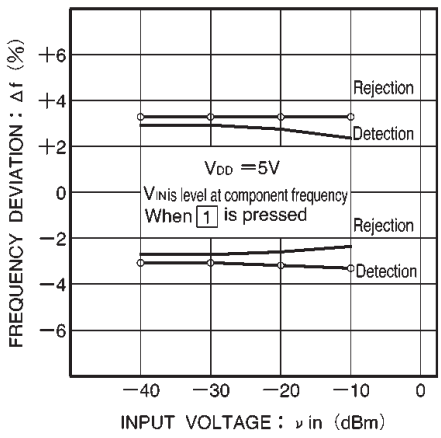


Fig. 14 Frequency detection/rejection ranges vs. input voltage

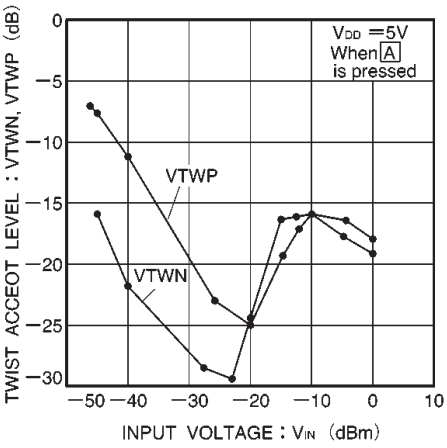


Fig. 15 2-frequency level vs. input voltage

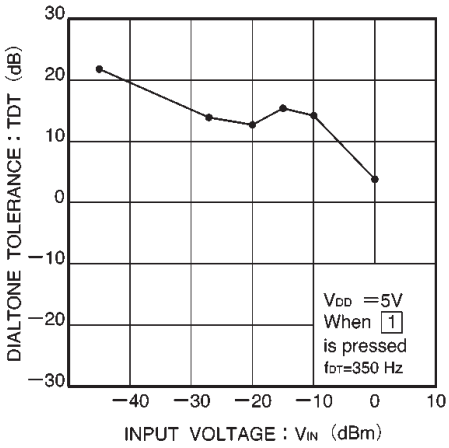


Fig. 16 Dial tone tolerance range vs. input voltage

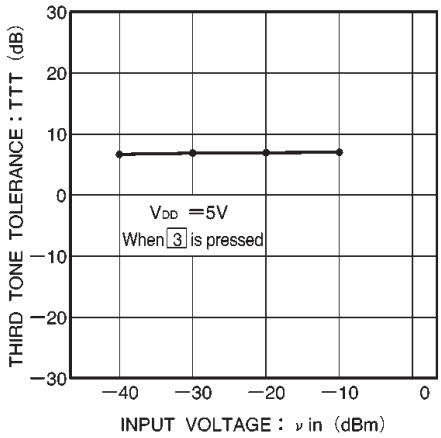


Fig. 17 3rd tone tolerance range vs. input voltage

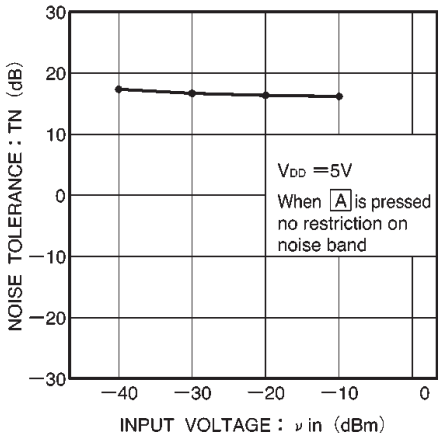
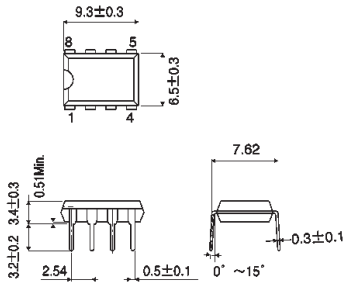


Fig. 18 Noise tolerance range vs. input voltage

●External dimensions (Units: mm)

BU8872



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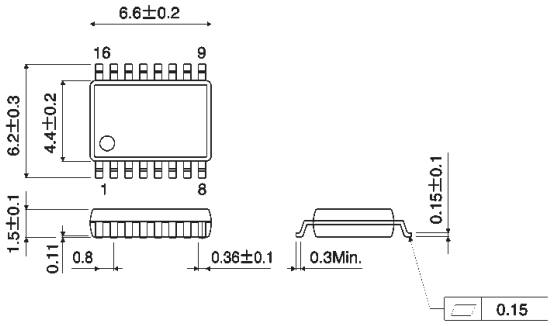
BU8872FS



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