

Bus-controlled audio matrix

Features

- Six stereo inputs
- Three stereo outputs
- Gain control 0 dB/Mute for each output
- Cascadable (2 different addresses)
- Serial bus controlled
- Very low noise
- Very low distortion
- Fully ESD protected
- Wide audio dynamic range (3 V_{RMS})



Table 1. Device summary

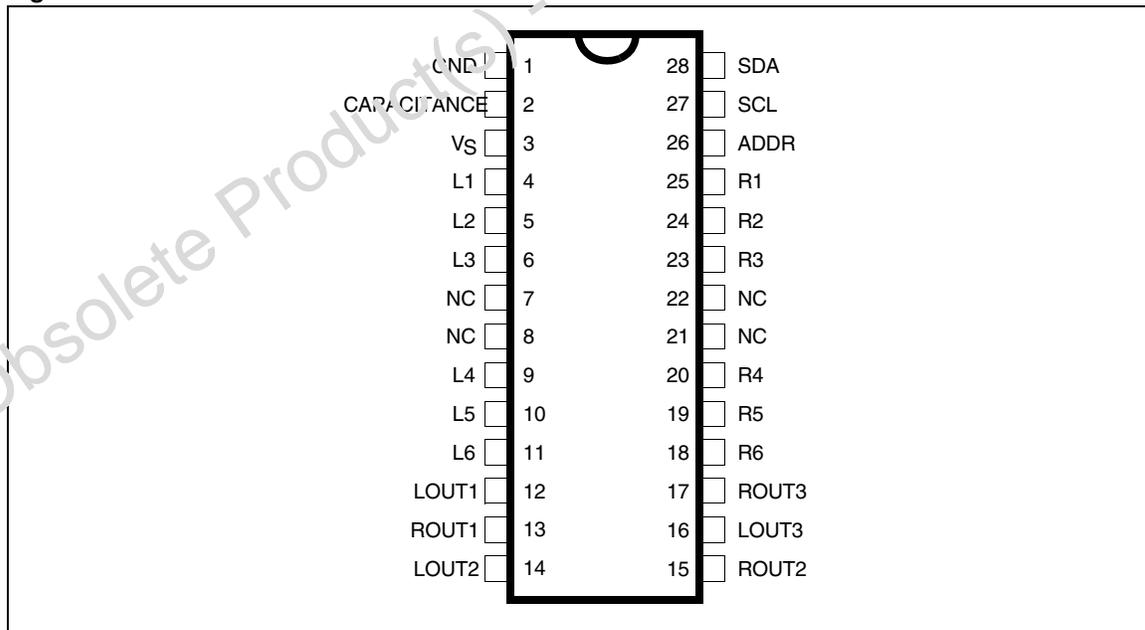
Order code	Packaging
E-TEA6422D	Tray

Description

The E-TEA6422D switches six stereo audio inputs on three stereo outputs.

All switching possibilities are controlled via the I²C bus.

Figure 1. Pinout

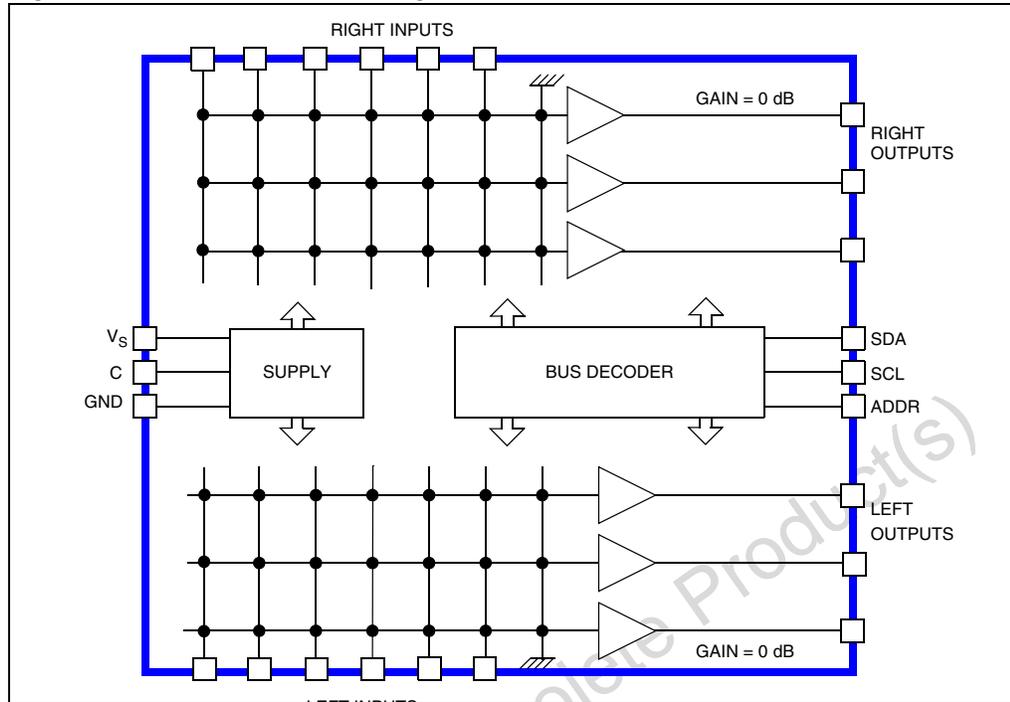


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1 Description

Figure 2. E-TEA6422D block diagram



2 Electrical characteristics

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (Pin 9)	12	V
T_{AMB}	Operating ambient temperature range	0, + 70	°C
T_{STG}	Storage temperature range	- 20, + 150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Junction-to-ambient thermal resistance	75	°C/W

Table 4. Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply						
V_S	Supply voltage		8	10	11	V
I_S	Supply current			3	8	mA
SVR	Ripple rejection	$V_{IN} = 500mV_{RMS}, f = 1kHz$	70	80		dB
Matrix						
V_{IN}	Input DC level			$V_{CC}/2$		V
R_I	Input resistance		30	50	100	k Ω
C_S	Channel separation	$V_{IN} = 2V_{RMS}, f = 1kHz$	80	90		dB
Output buffer						
V_{OUT}	Output DC level			$V_{CC}/2$		V
R_{OUT}	Output resistance			50	100	Ω
e_{NI}	Input noise	BW = 20 - 20kHz, flat		3		μ V
S/N	Signal to noise ratio	$V_{IN} = V_{OUT} = 1V_{RMS}$		110		dB
G	Gain		-1	0	+ 1	dB
d	Distortion	$V_{IN} = V_{OUT} = 1V_{RMS}$		0.01	0.05	%
V_{CL}	Clipping level	$d = 0.3\%, V_S = 10V$	2.8	3		V_{RMS}
R_L	Output load resistance		2			k Ω

Note: $T_{AMB} = 25\text{ }^\circ\text{C}, V_S = 9\text{ V}, R_L = 10\text{ k}\Omega, R_G = 600\text{ }\Omega, f = 1\text{ kHz}$ (unless otherwise specified)

Table 5. I²C bus characteristics

Symbol	Parameter	Test conditions	Min.	Max.	Unit
SCL					
V _{IL}	Low level input voltage		- 0.3	+ 1.5	V
V _{IH}	High level input voltage		3.0	V _{CC} + 0.5	V
I _{LI}	Input leakage current	V _I = 0 to V _{CC}	- 10	+ 10	μA
f _{SCL}	Clock frequency		0	100	kHz
t _R	Input rise time	1.5 V to 3 V		1000	ns
t _F	Input fall time	3 V to 1.5 V		300	ns
C _I	Input capacitance			10	pF
SDA					
V _{IL}	Low level input voltage		- 0.3	+ 1.5	V
V _{IH}	High level input voltage		3.0	V _{CC} + 0.5	V
I _{LI}	Input leakage current	V _I = 0 to V _{CC}	- 10	+ 10	μA
C _I	Input capacitance			10	pF
t _R	Input rise time	1.5 V to 3 V		1000	ns
t _F	Input fall time	3 V to 1.5 V		300	ns
V _{OL}	Low level output voltage	I _{OL} = 3mA		0.4	V
t _F	Output fall time	3 V to 1.5 V		250	ns
C _L	Load capacitance			400	pF
Timing					
t _{LOW}	Clock low period		4.7		μs
t _{HIGH}	Clock high period		4.0		μs
t _{SU, DAT}	Data set-up time		250		ns
t _{HD, DAT}	Data hold time		0	340	ns
t _{SU, STO}	Set-up time from clock high to stop		4.0		μs
t _{BUF}	Start set-up time following a stop		4.7		μs
t _{HD, STA}	Start hold time		4.0		μs
t _{SU, STA}	Start set-up time following clock low-to high transition		4.7		μs

Figure 3. I²C bus timing

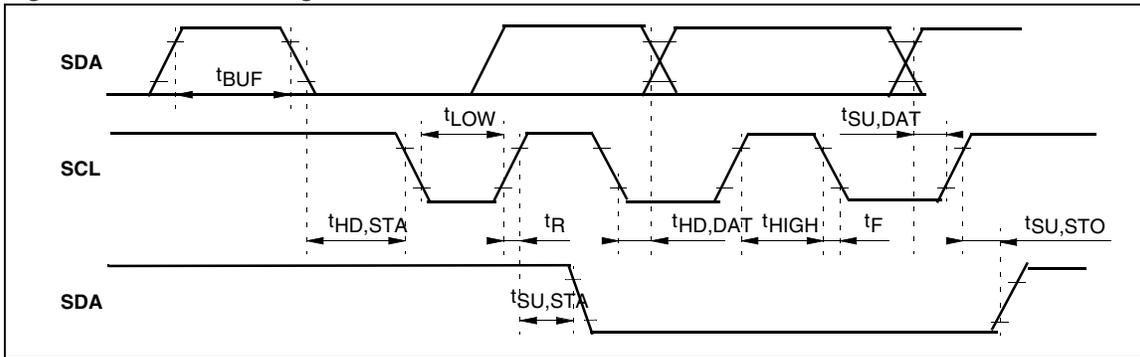


Table 6. Power on reset

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Reset	Start of Reset	Incr. V_{CC}			2.5	V
	End of Reset	Decr. V_{CC} Incr. V_{CC}	4.5		4.2	

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3 Software specification

3.1 Chip address

Table 7. Chip address

Address	HEX	Addr
1001 1000	98	0
1001 1010	9A	1

3.2 Data bytes

Output select

X	0	0	X	X	I_2	I_1	I_0	Output 1
	0	1						Output 2
	1	0						Output 3

Input select

X	Q_1	Q_0	X	X	0	0	0	Input 1
					0	0	1	Input 2
					0	1	0	Input 3
					0	1	1	Input 4
					1	0	0	Input 5
					1	0	1	Input 6
					1	1	0	Mute

X = don't care - MSB is transmitted first

Example: 010XX100 connects output 3 with input 5.

Figure 4. Distortion level vs input voltage

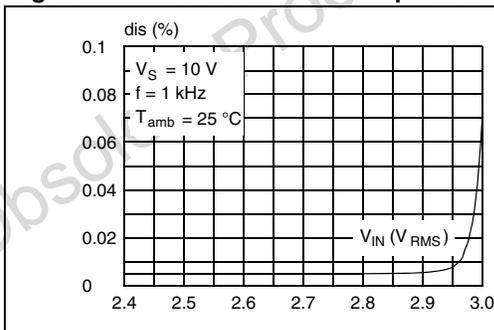


Figure 5. Clipping level vs supply voltage

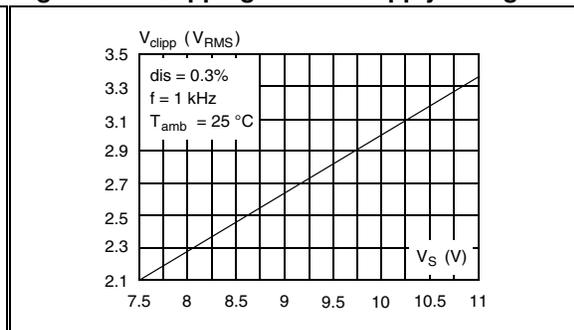
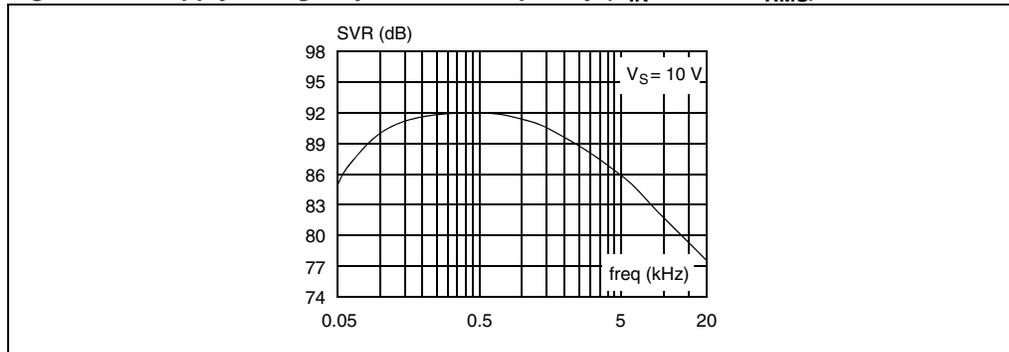


Figure 6. Supply voltage rejection vs frequency ($V_{IN} = 500 \text{ mV}_{RMS}$)

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4 Pin configurations

Figure 7. Audio IN

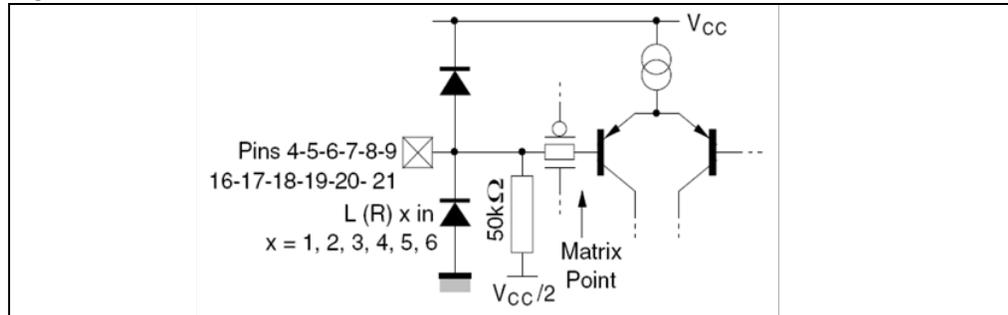


Figure 8. Addr

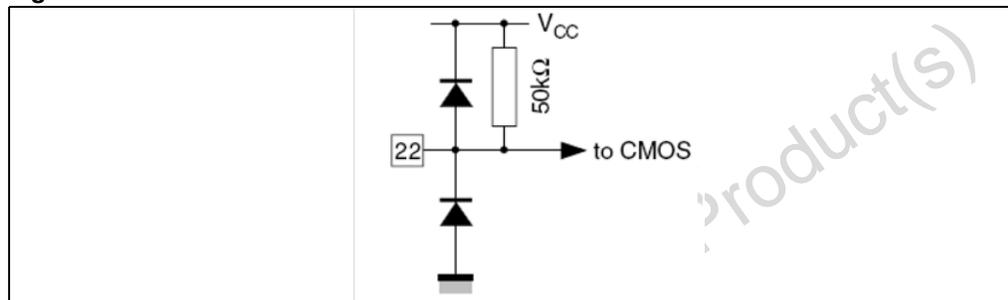


Figure 9. Bus inputs (SDA and SCL)

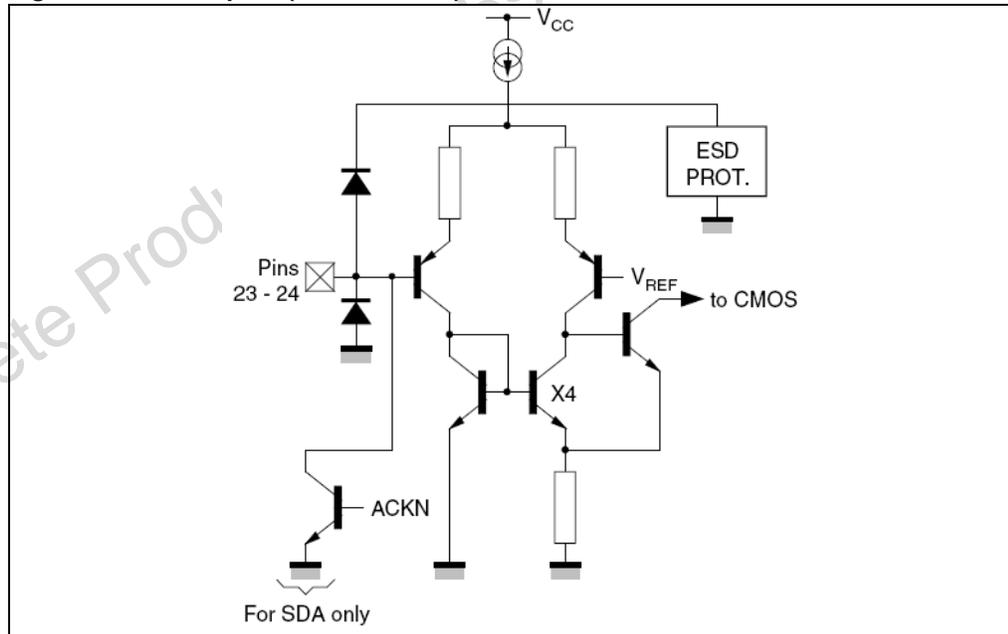


Figure 10. Audio out

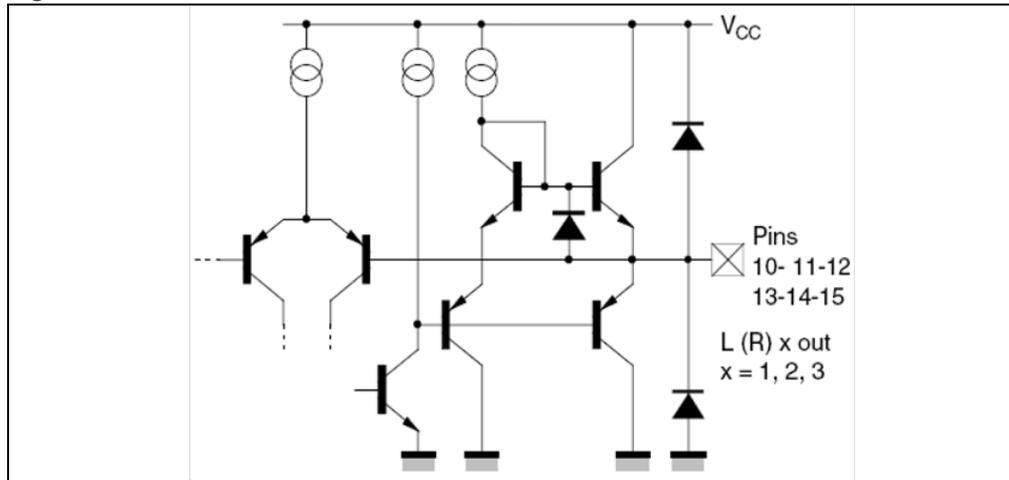
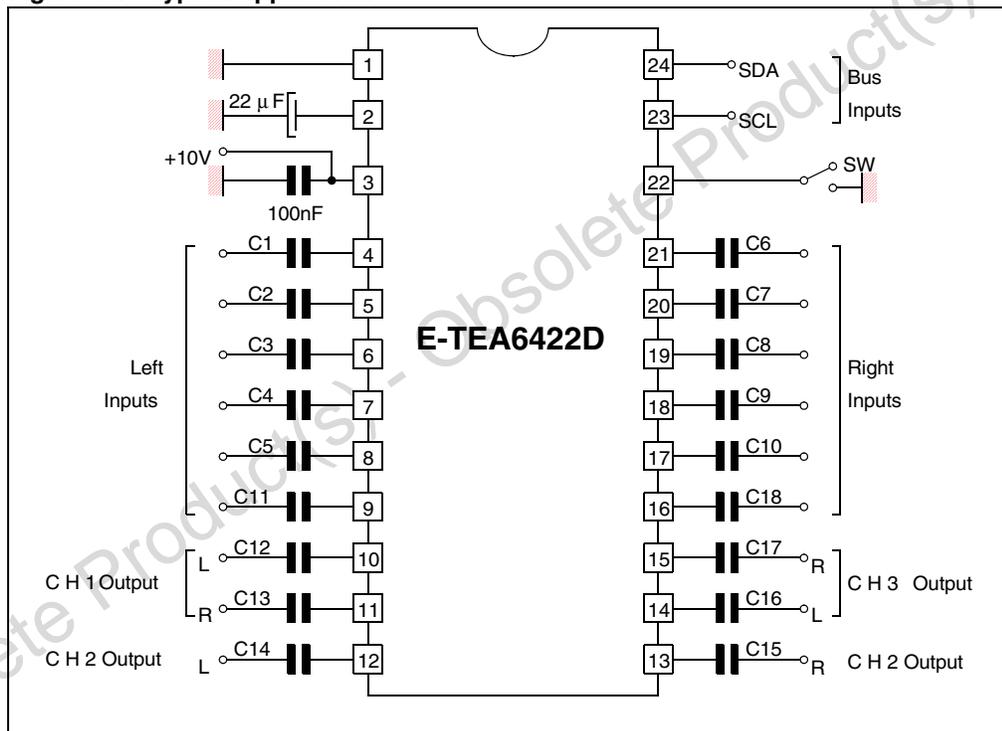


Figure 11. Typical application



5 Package mechanical data

Figure 12. 28-pin small outline plastic package (SO28)

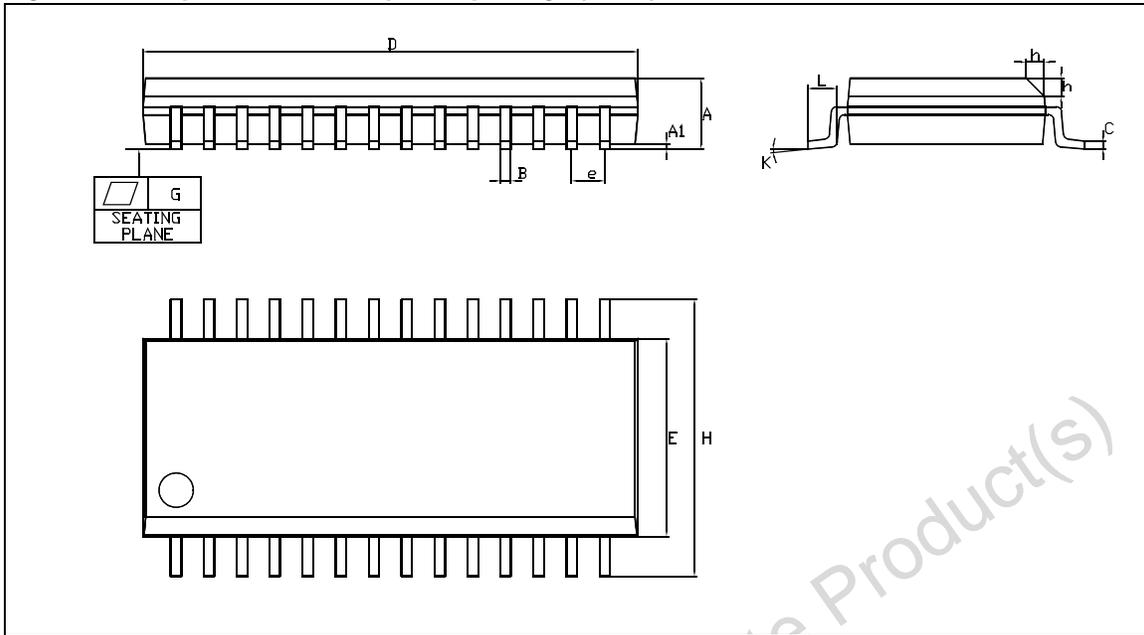


Table 8. SO28 dimensions

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.35		2.65	0.0926		0.1043
A1	0.10		0.30	0.0040		0.0118
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.0091		0.0125
D	17.70		18.10	0.6969		0.7125
E	7.40		7.60	0.2914		0.2992
e		1.27			0.0500	
H	10.01		10.64	0.394		0.419
h	0.25		0.74	0.010		0.029
K				0°		8°
L	0.41		1.27	0.016		0.050
G			0.10			0.004
	Number of Pins					
N	28					

5.1 Environmentally-friendly packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance.

ECOPACK specifications, grade definitions and product status are available at: www.st.com.
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6 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Feb-2005	1	Initial release
12-Mar-2009	2	New template applied, Section 5.1: Environmentally-friendly packages added

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