NB4L858M

2.5V/3.3V, 3 GHz Dual Differential Clock/Data 2x2 Crosspoint Switch with CML Output and Internal Termination

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Description

The NB4L858M is a high−bandwidth low voltage fully differential dual 2 x 2 crosspoint switch with CML outputs that is suitable for applications such as SDH/SONET DWDM and high speed switching applications. Design technique minimizes jitter accumulation, crosstalk, and signal skew which make this device ideal for loop−through and protection channel switching application. Each 2 x 2 crosspoint switch can fan out and/or multiplex up to 3 Gb/s data and 3 GHz clock signals.

Differential inputs incorporate a pair of internal 50 Ω termination resistors in a center−tapped configuration (V_{TDx} Pins) and can accept LVPECL (Positive ECL) or CML input signal without any external component. This feature provides transmission line termination on−chip, at the receiver end, eliminating external components. Differential 16 mA CML output provides matching internal 50 Ω terminations, and 400 mV output swings when externally terminated, 50 Ω to V_{CC}.

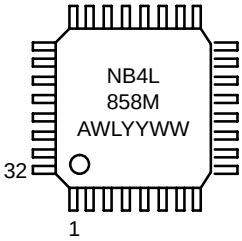
The SELECT inputs are single−ended and can be driven with either LVCMOS or LVTTL input levels. The device is housed in a low profile 7 x 7 mm 32−pin LQFP package.

Features

- Maximum Input Clock Frequency 3 GHz
- Maximum Input Data Frequency 3 Gb/s
- 350 ps Typical Propagation Delay
- 80 ps Typical Rise and Fall Times
- 12 ps Channel to Channel Skew
- 0.5 ps RMS Jitter
- 5 ps Deterministic Jitter @ 2.5 Gb/s
- Operating Range: V_{CC} = 2.3V to 3.6 V with GND = 0 V
- CML Output Level (400 mV Peak−to−Peak Output), Differential Output
- These are Pb−Free Devices

LQFP−32
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

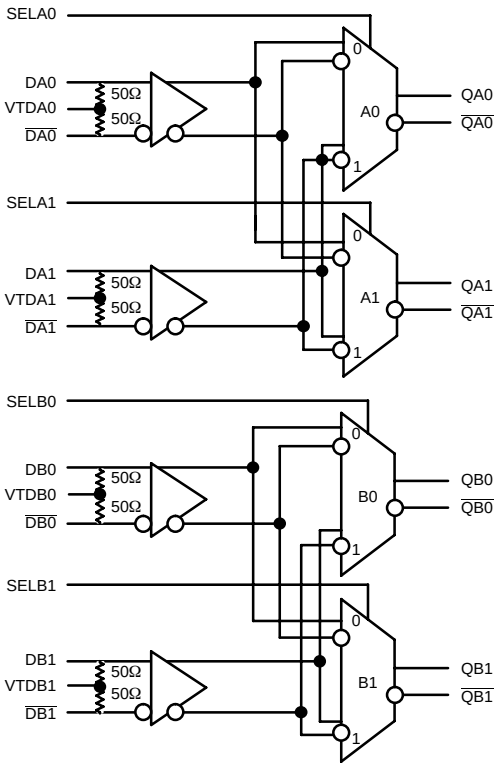


Figure 1. Functional Block Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

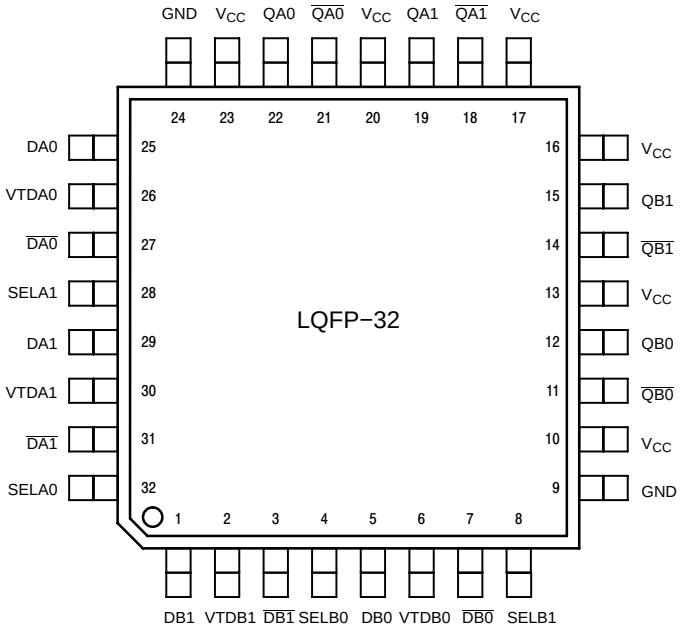


Figure 1. Pin Configuration (Top View)

Table 1. TRUTH TABLE

SELA0/SELB0	SELA1/SELB1	QA0/QB0	QA1/QB1	Function
L	L	DA0/DB0	DA0/DB0	1:2 Fanout or Redundant Distribution
L	H	DA0/DB0	DA1/DB1	Quad Repeater or Crosspoint Switch
H	L	DA1/DB1	DA0/DB0	Quad Repeater or Crosspoint Switch
H	H	DA1/DB1	DA1/DB1	1:2 Fanout or Redundant Distribution

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	DB1	LVPECL, CML Input	Channel B1 positive signal input.
2	VTDB1	−	Internal 100 Ω center−tapped termination pin for channel B1.
3	$\overline{DB1}$	LVPECL, CML Input	Channel B1 negative signal input.
4	SELB0	LVTTL / LVCMOS	Channel B0 Output Select. See Table 1.
5	DB0	LVPECL, CML Input	Channel B0 positive signal input.
6	VTDB0	−	Internal 100 Ω center−tapped termination pin for channel B0.
7	$\overline{DB0}$	LVPECL, CML Input	Channel B0 negative signal input.
8	SELB1	LVTTL / LVCMOS	Channel B1 output select. See Table 1.
9,24	GND	−	Supply ground. All GND pins must be externally connected to power supply to guarantee proper operation.
10, 13, 16, 17, 20, 23	V_{CC}	−	Positive Supply. All V_{CC} pins must be externally connected to power supply to guarantee proper operation.
11	$\overline{QB0}$	CML Output	Channel B0 negative signal output. Typically terminated with 50 Ω resistor to V_{CC}.
12	QB0	CML Output	Channel B0 positive signal output. Typically terminated with 50 Ω resistor to V_{CC}
14	$\overline{QB1}$	CML Output	Channel B1 negative signal output. Typically terminated with 50 Ω resistor to V_{CC}.
15	QB1	CML Output	Channel B1 positive signal output. Typically terminated with 50 Ω resistor to V_{CC}.
18	$\overline{QA1}$	CML Output	Channel A1 negative signal output. Typically terminated with 50 Ω resistor to V_{CC}.
19	QA1	CML Output	Channel A1 positive signal output. Typically terminated with 50 Ω resistor to V_{CC}.
21	$\overline{QA0}$	CML Output	Channel A0 negative signal output. Typically terminated with 50 Ω resistor to V_{CC}.
22	QA0	CML Output	Channel A0 positive signal output. Typically terminated with 50 Ω resistor to V_{CC}.
25	DA0	LVPECL, CML Input	Channel A0 positive signal input.
26	VTDA0	−	Internal 100 Ω center−tapped termination pin for channel A0.
27	$\overline{DA0}$	LVPECL, CML Input	Channel A0 negative signal input.
28	SELA1	LVTTL	Channel A1 output select. See Table 1.
29	DA1	LVPECL, CML Input	Channel A1 positive signal input.
30	VTDA1	−	Internal 100 Ω center−tapped termination pin for channel A1.
31	$\overline{DA1}$	LVPECL, CML Input	Channel A1 negative signal input.
32	SELA0	LVTTL	Channel A0 output select. See Table 1.

Table 3. Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2000 V >110 V
Moisture Sensitivity (Note 1)	32−LQFP	Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		380
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		3.8	V
V_I	Positive Input	GND = 0 V	GND ≤ V_I ≤ V_{CC}	3.8	V
V_{INPP}	Differential Input Voltage $\lvert D - \overline{D} \rvert$			3.8	V
I_{IN}	Input Current Through Internal R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{OUT}	Output Current	Continuous Surge		25 80	mA mA
T_A	Operating Temperature Range	LQFP−32		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 2)	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder Pb−Free	<3 sec @ 260°C		265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

2. JEDEC standard 51−6, multilayer board − 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS, CLOCK INPUTS, CML OUTPUTS V_{CC} = 2.3 V to 3.6 V, GND = 0 V T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current		130	190	mA
$V_{outdiff}$	CML Differential Output Swing (Note 3) No Load Loaded 50 Ω to V_{CC}	640	800 400	1000	mV
V_{OH}	Output HIGH Voltage (No Load)	V_{CC}−40	V_{CC}−10	V_{CC}	mV
V_{OL}	Output LOW Voltage (No Load)	V_{CC}−1000	V_{CC}−800	V_{CC}−650	mV
R_{TOUT}	Output Source Resistance Qx or $\overline{Qx}$	40	50	60	Ω
V_{IH}	Input HIGH Voltage	1600		V_{CC}	mV
V_{IL}	Input LOW Voltage	1500		V_{CC}−100	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	100		1600	mV
R_{TIN}	Input Termination Resistance D_x or $\overline{D_x}$ to V_{TDx}	40	50	60	Ω
LVTTL CONTROL INPUT PINS					
V_{IH}	Input HIGH Voltage (LVTTL Inputs)	2000			mV
V_{IL}	Input LOW Voltage (LVTTL Inputs)			800	mV
I_{IH}	Input HIGH Current (LVTTL inputs)	−10		10	μA
I_{IL}	Input LOW Current (LVTTL Inputs)	−10		10	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. CML outputs require 50 Ω receiver termination resistors to V_{CC} for proper operation.

Table 6. AC CHARACTERISTICS V_{CC} = 2.3 V to 3.6 V, GND = 0 V; (Note 4)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (See Figure 2) $f_{in} \le 2$ GHz $f_{in} \le 3$ GHz $f_{in} \le 3.5$GHz	280 235 170	365 310 220		280 235 170	365 310 220		280 235 170	365 310 220		mV
f_{DATA}	Maximum Operating Data Rate	3			3			3			Gb/s
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential D/$\overline{D}$ to Q/$\overline{Q}$	220	350	450	220	350	450	220	350	450	ps
t_{SWITCH}	SELyx to Valid Qyx Output (Note 9)		0.5	1.0		0.5	1.0		0.5	1.0	ns
t_{SKEW}	Within −Device Skew (Note 5) Within −Device Skew (Note 6) Device to Device Skew (Note 9)		12 25 100			12 25 100			12 25 100		ps
t_{JITTER}	RMS Random Clock Jitter (Note 8) f_{in} =2 GHz f_{in} =3 GHz Peak−to−Peak Data Dependent Jitter f_{in} =2.5Gb/s (Note 9) f_{in} =3.2Gb/s Crosstalk Induced RMS Jitter (Note 11)		0.5 1.0 2.0 10 0.5			0.5 1.0 5.0 10 0.5			0.5 1.0 2.0 10 0.5		ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration)	100		800	100		800	100		800	mV
t_r t_f	Output Rise/Fall Times @ 0.5 GHz Q_x, $\overline{Q_x}$ (20% − 80%)		80	120		80	120		80	120	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Measured by forcing V_{INPP} (MIN) from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC}. Input edge rates 40 ps (20% − 80%).
5. Worst−case difference between QA0 and QA1 from either DA0 or DA1 (or between QB0 and QB1 from either DB0 or DB1 respectively), when both outputs come from the same input.
6. Worst−case difference between QA and QB outputs, when DA or DB inputs are shorted.
7. Additive RMS jitter with 50% duty cycle input clock signal.
8. Additive peak−to−peak data dependent jitter with input NRZ data signal.
9. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.
10. LVTTL/LVCMOS input edge rate less than 1.5 ns
11. Data taken on the same device under identical condition.

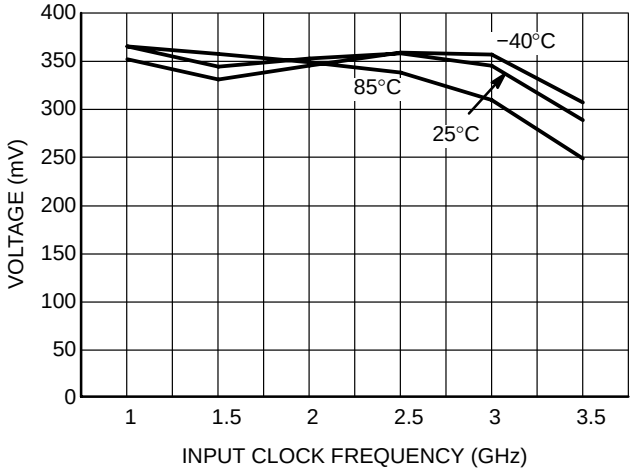


Figure 2. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (fin) and Temperature

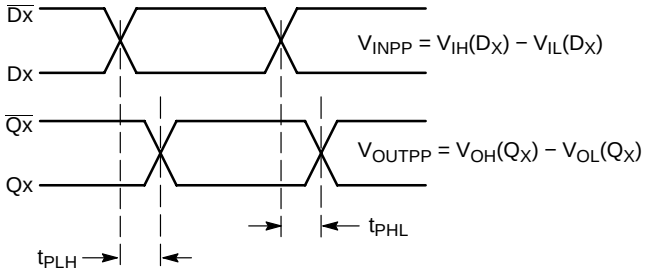


Figure 3. AC Reference Measurement

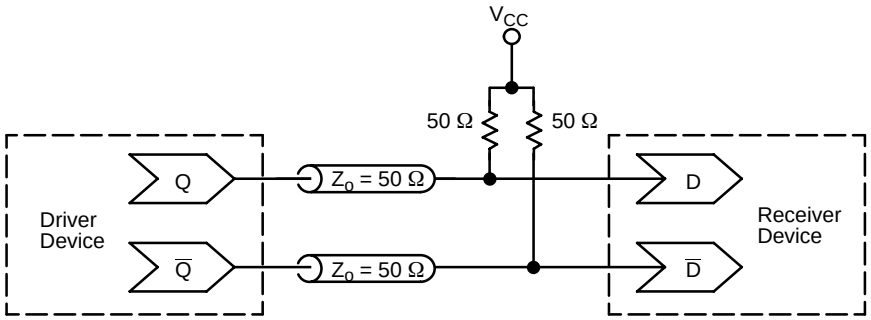


Figure 4. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8057/D)

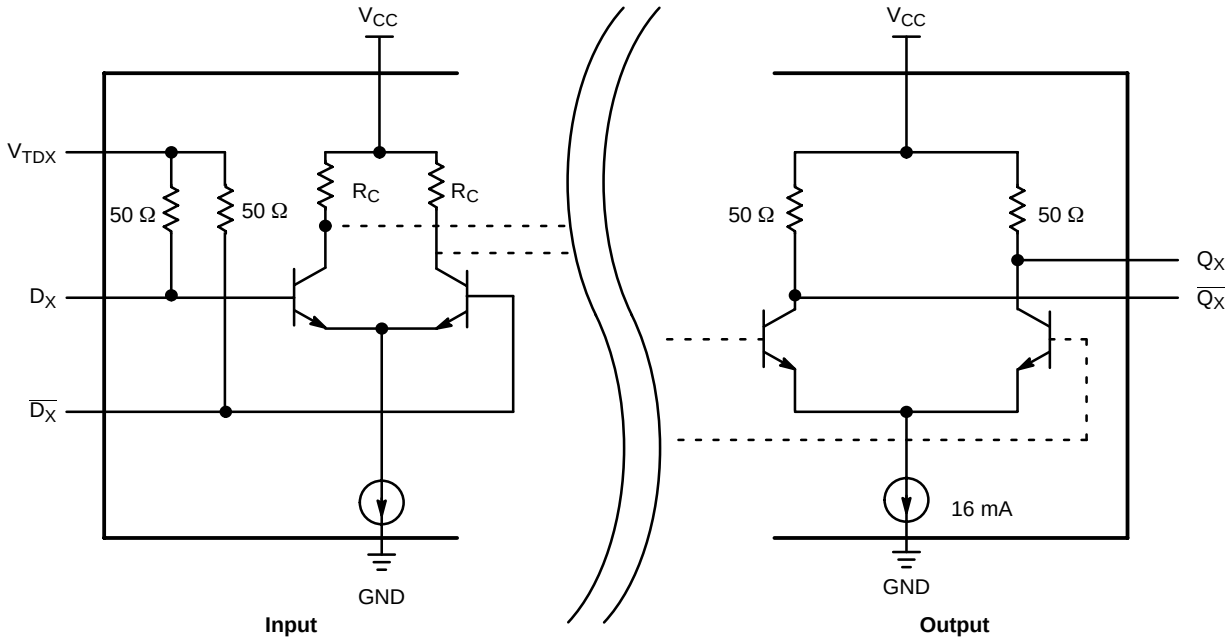


Figure 5. CML Input and Output Structure

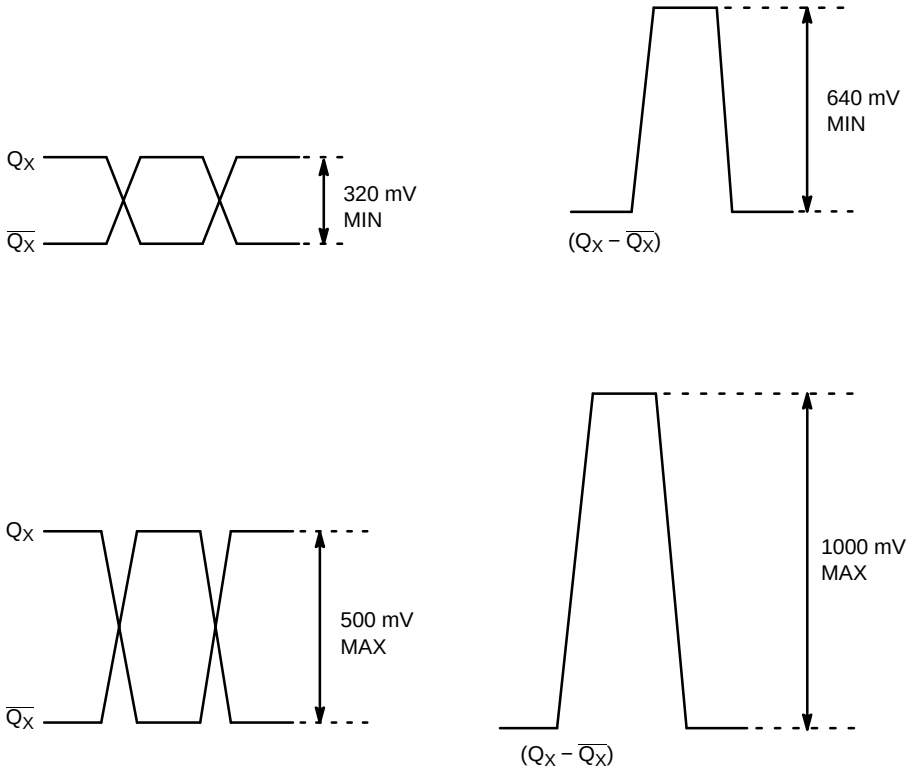


Figure 6. CML Output Levels

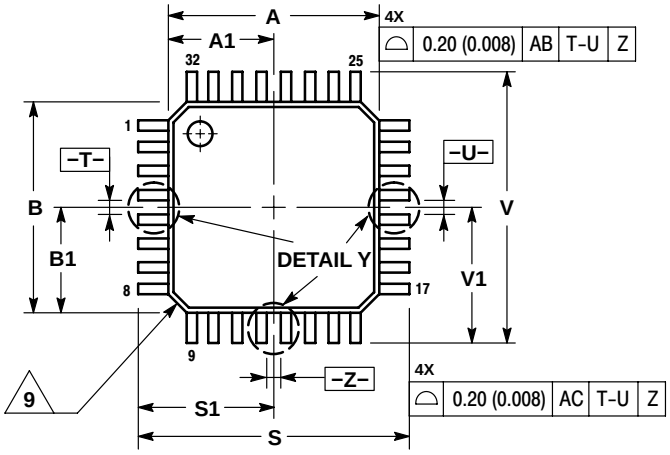
ORDERING INFORMATION

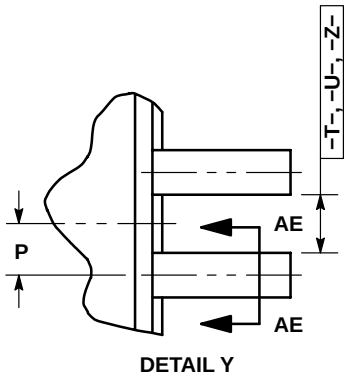
Device	Package	Shipping†
NB4L858MFAG	LQFP−32 (Pb−Free)	250 Units / Tray
NB4L858MFAR2G	LQFP−32 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

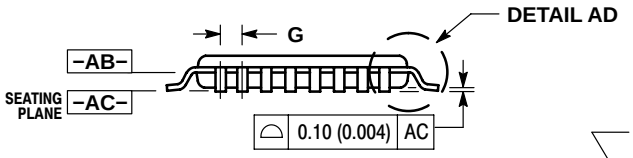
PACKAGE DIMENSIONS

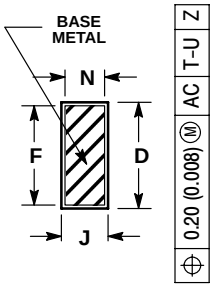
LQFP
FA SUFFIX
32−LEAD PLASTIC PACKAGE
CASE 873A−02
ISSUE B



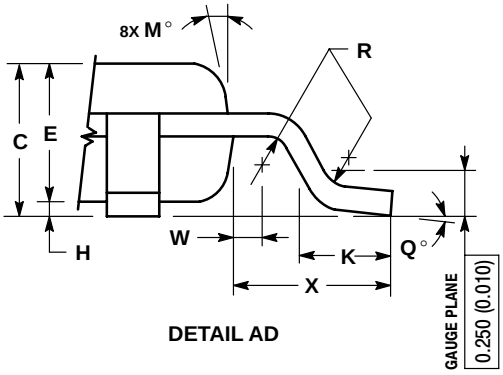


DETAIL Y





SECTION AE−AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −AB− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS −T−, −U−, AND −Z− TO BE DETERMINED AT DATUM PLANE −AB−.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE −AC−.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −AB−.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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