LOW POWER DUAL SPST HI-SPEED USB 2.0 (480MBPS) SWITCH

IDTUS8031

Description

The IDTUS8031 is a low power, dual SPST 2-port hi-speed USB 2.0 switch. This part is configured as a single pole, single throw switch and is optimized for switching or isolating a hi-speed (480 Mbps) source or a hi-speed and full-speed (12 Mbps) source. The IDTUS8031 is compatible with the requirements of USB2.0 and features an extremely low ON capacitance (C_{ON}) of 3.7 pF. The wide bandwidth of this device (>720 MHz) exceeds the bandwidth needed to pass the 3rd harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

The IDTUS8031 contains circuitry on the D+/D- pins which allows the device to withstand an overvoltage condition. This device is also designed to minimize current consumption even when the control voltage applied to the $\overline{OE}$ pin is lower than the supply voltage (V_{CC}). This feature is especially valuable to portable applications such as cell phones, allowing for direct interface with the general purpose I/Os of the baseband processor.

Applications

- Notebooks, PDAs
- Cellular phones, Digital cameras
- LCD monitors, TVs, Set-top Boxes
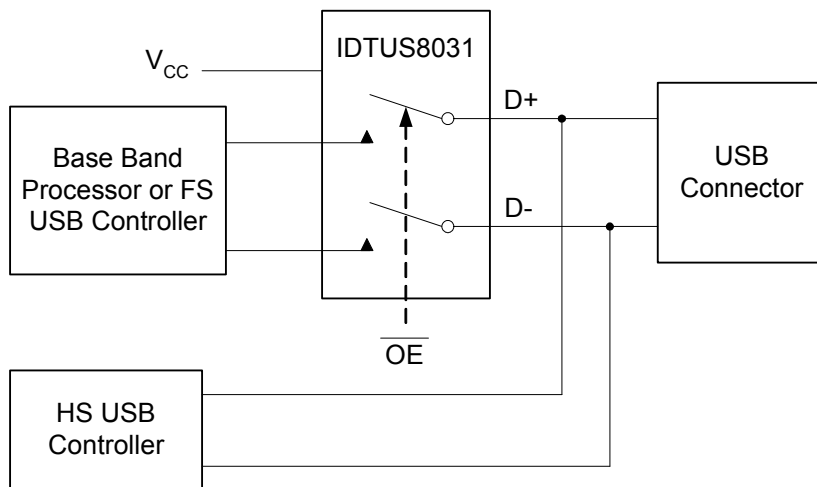
Features

- Low On capacitance, 3.7 pF (typical)
- Low On resistance, 6.5Ω (typical)
- Low power consumption (1 µA maximum)
    - 10 µA maximum ICCT over and expanded control voltage range (VIN=2.6 V, V_{CC}=4.3 V)
- Wide -3dB bandwidth, > 720 MHz
- 8K I/O to GND ESD protection
- Power OFF protection when V_{CC}= 0V, D+/D- pins can tolerate up to 4.3 V
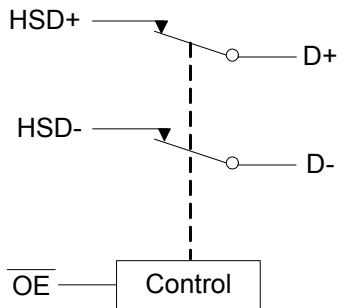- Packaged in RoHS compliant 8-pin MSOP and 10-lead µMLP (1.4 x1.8mm)

Block Diagram

Pin Assignment (MSOP)
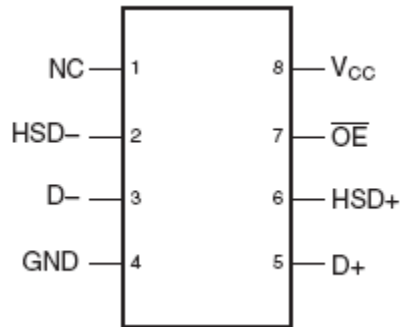
Pin Assignment (µMLP)
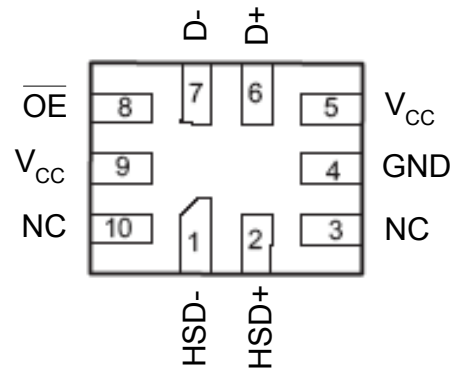
Analog Symbol

Truth Table

$\overline{OE}$	Function
H	Disconnect
L	D+, D- = HSD

Pin Descriptions

Pin Name	Pin Description
$\overline{OE}$	Bus switch enable.
D+, D-, HSD+, HSD-	Data ports.
NC	No connect.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDTUS8031. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range. All voltages referenced to ground.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5 V to 4.6 V
V_S	DC Input Voltage [1]	-0.5 V to 4.6 V
V_{IN}	DC Switch Voltage [1] HSD D+, D-	-0.5 V to V_{CC} to 0.3 V -0.5 V to 4.6 V
	DC Input Diode Current	-50 mA
	DC Output Current	50 mA
	Storage Temperature	-65°C to 150°C
	ESD (Human Body Mode) All Pins I/O to GND	 7.5 kV 8 kV

Recommended Operating Conditions [2]

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	3.0 V to 4.3 V
V_{IN}	DC Switch Voltage	0V to V_{CC}
	DC Input Diode Current	0V to V_{CC}
	Storage Temperature	-40°C to +85°C

Note 1: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed. DC switch voltage may never exceed 4.6V

Note 2: Control input must be held HIGH or LOW and it must not float.

DC Electrical Characteristics

Unless stated otherwise, typical values are at 25°C

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN} = -18 mA	3.0	0		-1.2	V
V_{IH}	Input Voltage HIGH		3.0 to 3.6	1.3			V
			4.3	1.7			
V_{IL}	Input Voltage LOW		3.0 to 3.6			0.5	V
			4.3			0.7	
I_{IN}	Control Input Leakage	V_{IN} = 0V to V_{CC}	4.3	-1.0		1.0	µA
I_{OZ}	OFF State Leakage	0 ≤ HSD ≤ V_{CC}	4.3	-2.0		2.0	µA
I_{OFF}	Power OFF Leakage Current (D+, D-)	V_{IN} = 0V to 4.3 V V_{CC} = 0V	0	-2.0		2.0	µA
R_{ON}	Switch On Resistance [1]	V_{IN} = 0.4 V, I_{ON} = -8 mA	3.0		6.5	10.0	Ω
$\triangle R_{ON}$	Delta R_{ON} [2]	V_{IN} = 0.4 V, I_{ON} = -8 mA	3.0		0.35		Ω
R_{ON} Flatness	R_{ON} Flatness [1]	V_{IN} = 0V to 1.0 V, I_{ON} = -8 mA	3.0		2.0		Ω
I_{CC}	Quiescent Supply Current	V_{IN} = 0V or V_{CC}, I_{OUT} = 0	4.3			1.0	µA
I_{CCT}	Increase in I_{CC} Current per Control voltage and V_{CC} levels	V_{IN} = 2.6 V, V_{CC} = 4.3 V	4.3			10.0	µA

Notes:

1. Measured by the voltage drop between Dn, HSD, Dn pins at the indicated current through the switch. On Resistance is determined by the lower of the voltage on the two ports.
2. Guaranteed by design.

AC Electrical Characteristics

Unless stated otherwise, typical values are for V_{CC} = 3.3 V at 25°C

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
t_{ON}	Turn ON Time, $\overline{OE}$ to output	V_{IN} = 0.8 V, R_L = 50Ω, C_L = 5 pF	3.0 to 3.6		15.0	30.0	ns
t_{OFF}	Turn OFF Time, $\overline{OE}$ to output	V_{IN} = 0.8 V, R_L = 50Ω, C_L = 5 pF	3.0 to 3.6		12.0	25.0	ns
t_{PD}	Propagation Delay [1]	R_L = 50Ω, C_L = 5 pF	3.3		0.25		ns
T_{BBM}	Break-Before-Make	V_{IN} = 0.8 V, R_L = 50Ω, C_L = 5 pF	3.0 to 3.6	2.0		6.5	ns
O_{IRR}	OFF Isolation (non-adjacent)	R_T = 50Ω, f = 240 MHz	3.0 to 3.6		-35.0		dB
Xtalk	Non-adjacent Channel Crosstalk	R_T = 50Ω, f = 240 MHz	3.0 to 3.6		-55.0		dB
BW	-3dB Bandwidth	R_T = 50Ω, C_L = 0 pF	3.0 to 3.6		720		MHz
		R_T = 50Ω, C_L = 5 pF			550		

Note 1: Guaranteed by design.

USB Hi-Speed Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
$t_{SK(O)}$	Channel-to-channel Skew [1]	C_L = 5 pF	3.0 to 3.6		50.0		ps
$t_{SK(P)}$	Skew of the Opposite Transitions of the Same Output [1]	C_L = 5 pF	3.0 to 3.6		20.0		ps
t_J	Total Jitter [1]	R_L = 50Ω, C_L = 5 pF, tR = tF = 500 ps at 480 Mbps (PRBS = 2^{15} - 1)	3.0 to 3.6		200		ps

Note 1: Guaranteed by design.

Capacitance

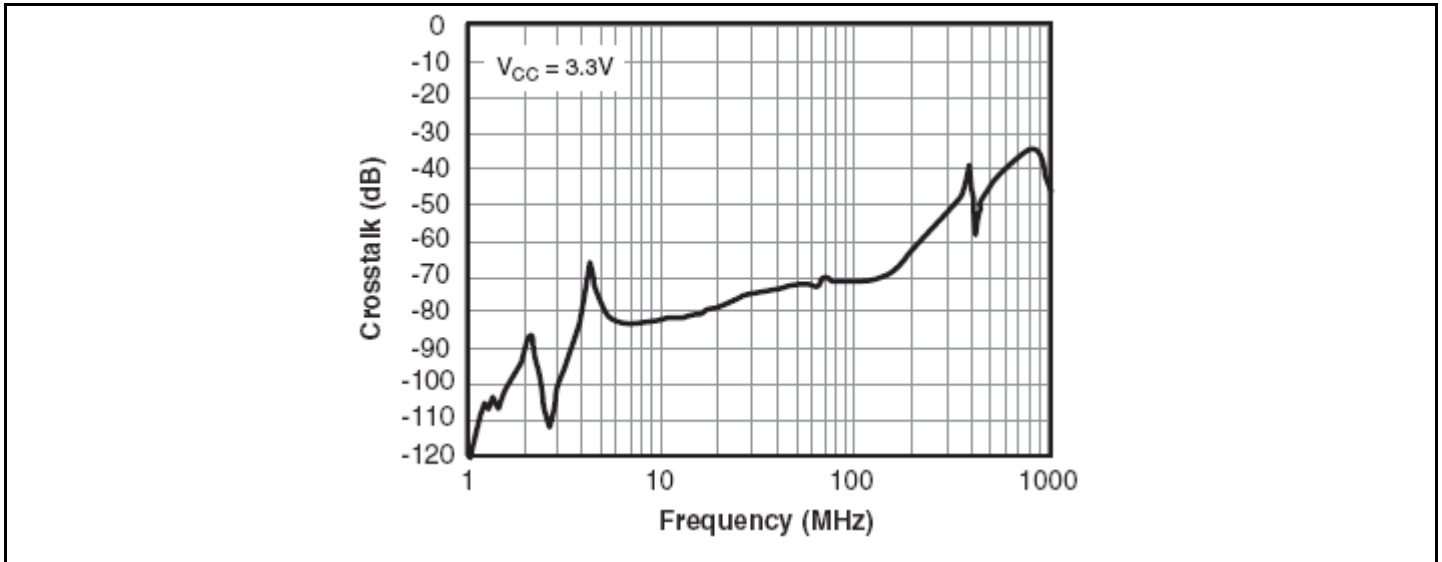| Symbol	Parameter	Conditions	T_A = -40°C to +85°C			Units
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance	V_{CC} = 0V		1.0		pF
C_{ON}	$D1_n$, $D2_n$, Dn ON Capacitance	V_{CC} = 3.3 V, $\overline{OE}$ = 0V		3.7		pF
C_{OFF}	$D1_n$, $D2_n$, OFF Capacitance	V_{CC} and $\overline{OE}$ = 3.3 V		1.7		pF

Test Circuits and Timing Diagrams
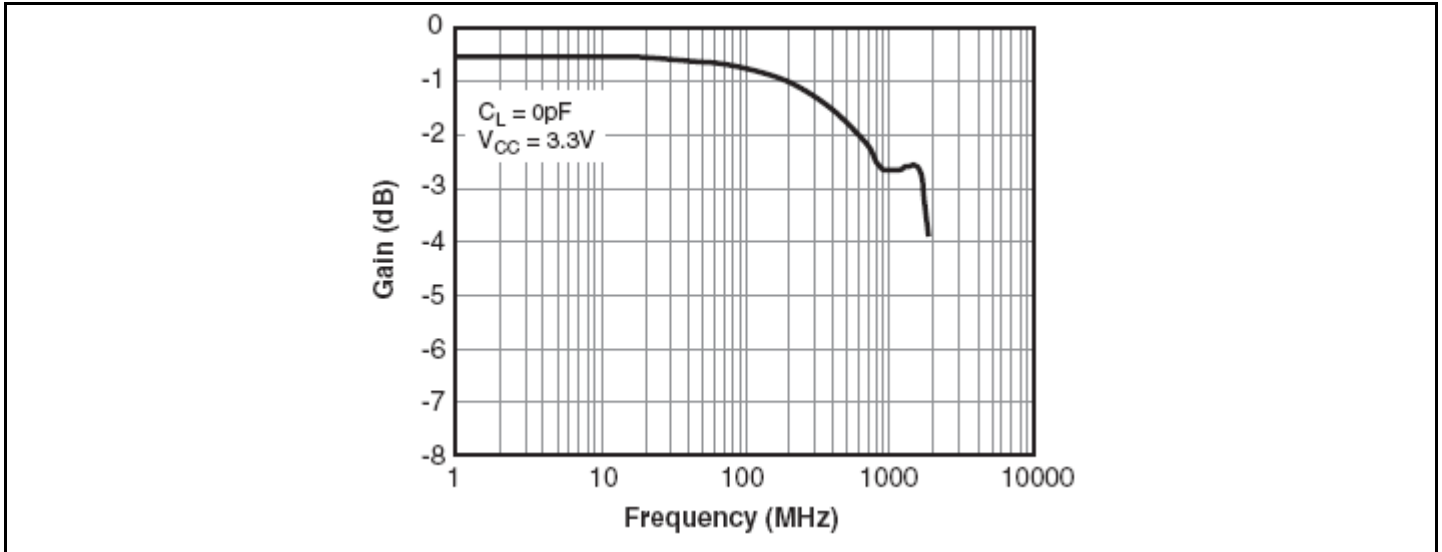
Gain vs. Frequency
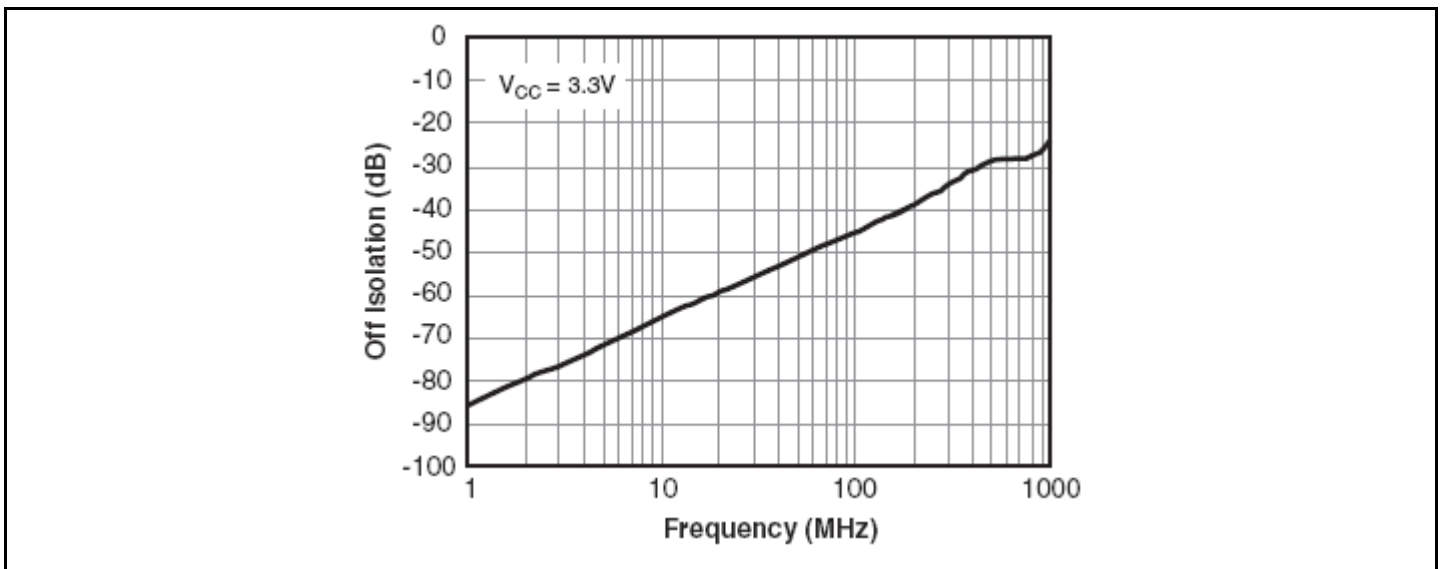
OFF Isolation

Crosstalk

On Resistance

NC

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$ID_{n(OFF)}$

$\overline{OE}$

$V_S = 0$ or V_{CC}

V_{IN}

GND
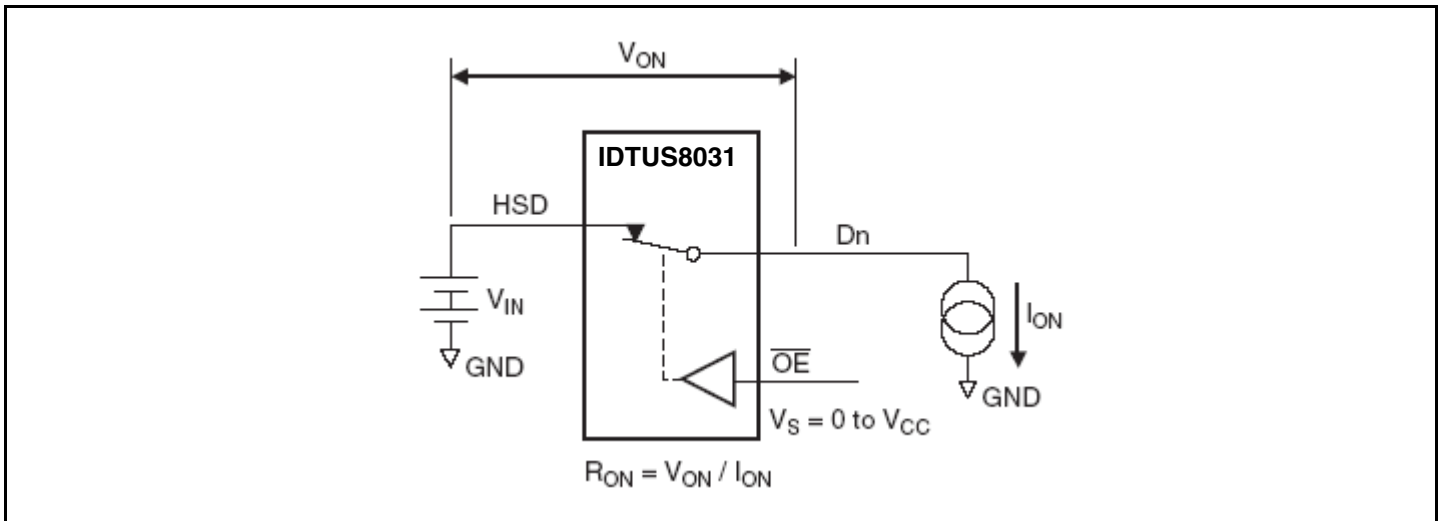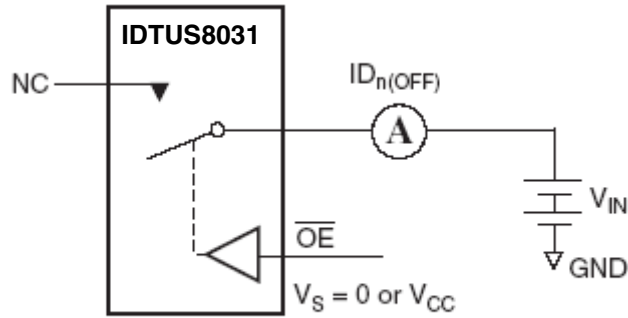
Each switch port is tested separately.

OFF Leakage

HSD

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V_{IN}

GND

R_S

D+, D−
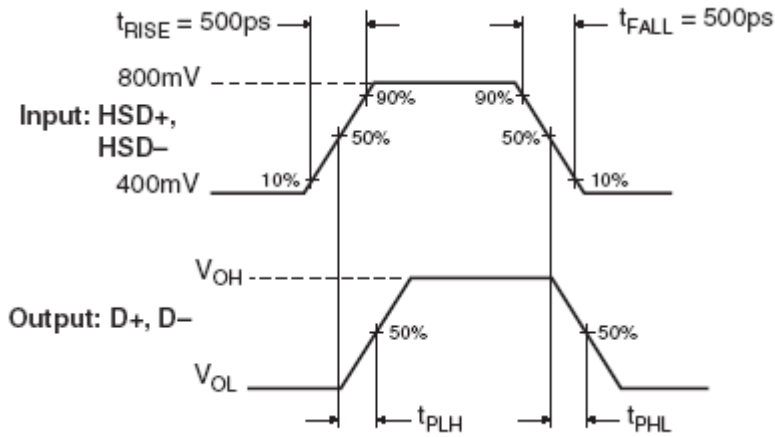
C_L^* R_L V_{OUT}

GND

$V_{\overline{OE}}$

GND
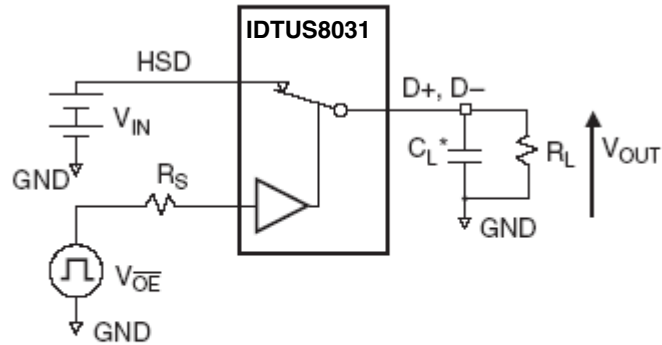
R_L, R_S, and C_L are functions of the application environment
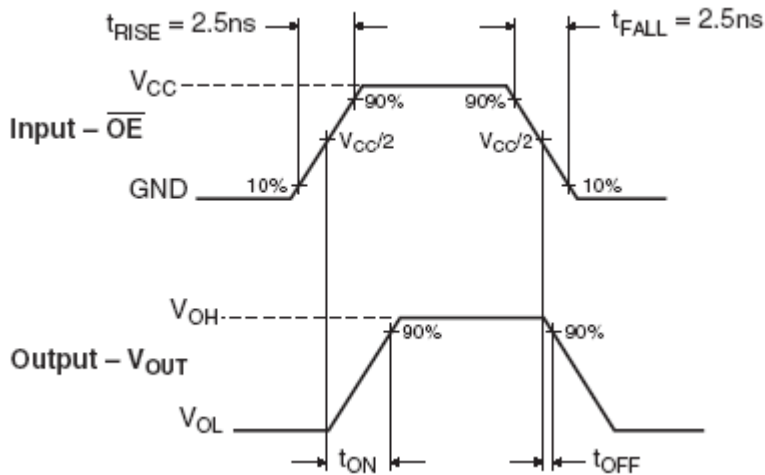(see AC Electrical tables for specific values).

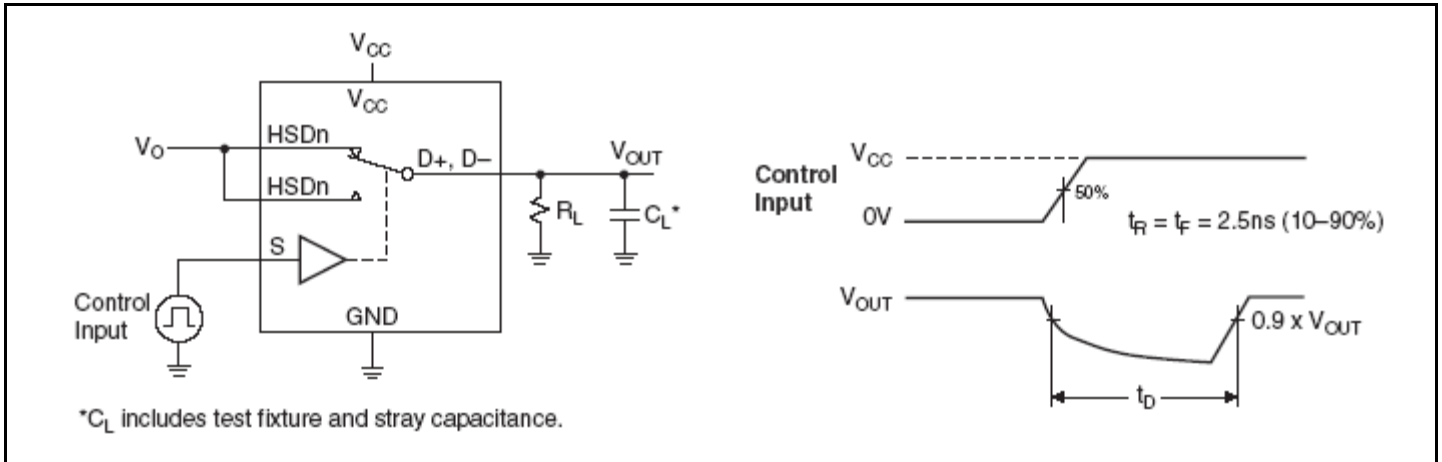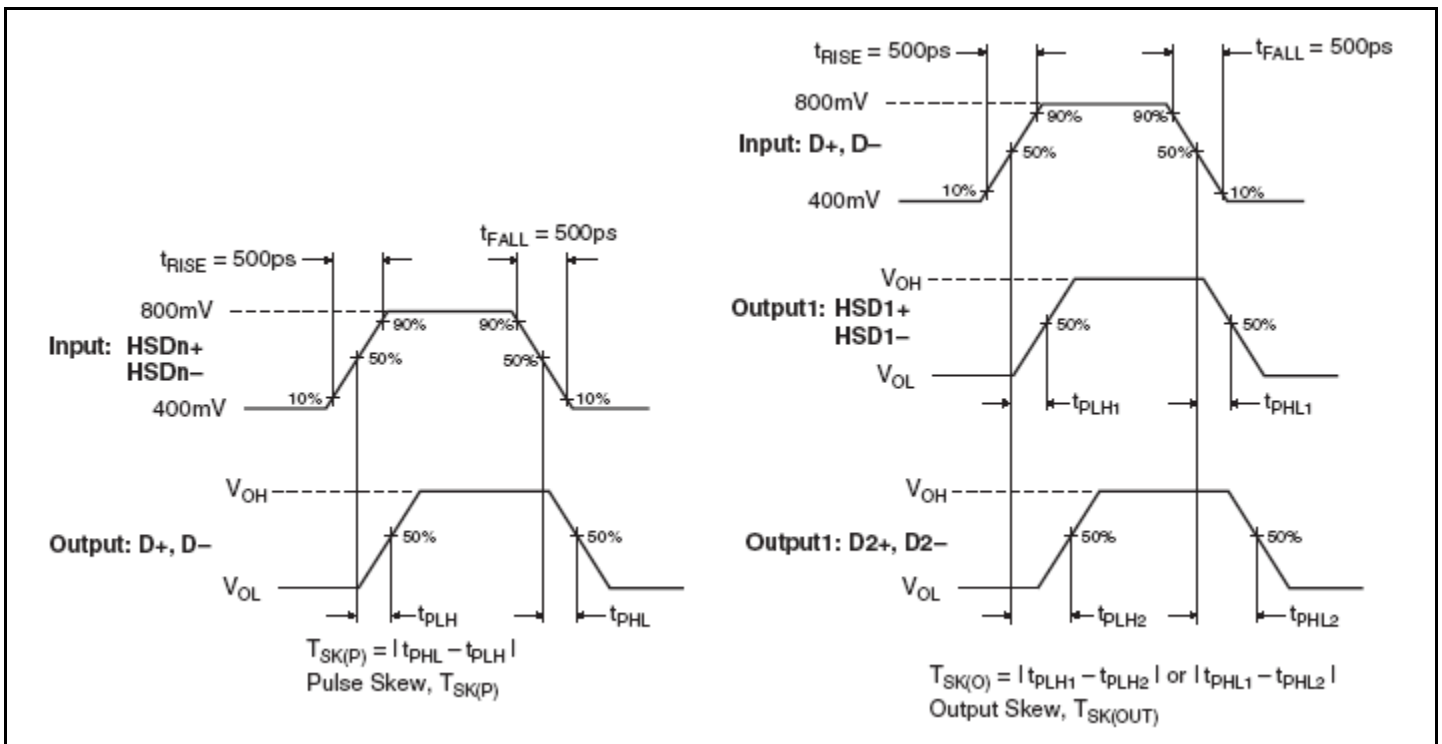*C_L includes test fixture and stray capacitance.

AC Test Circuit Load
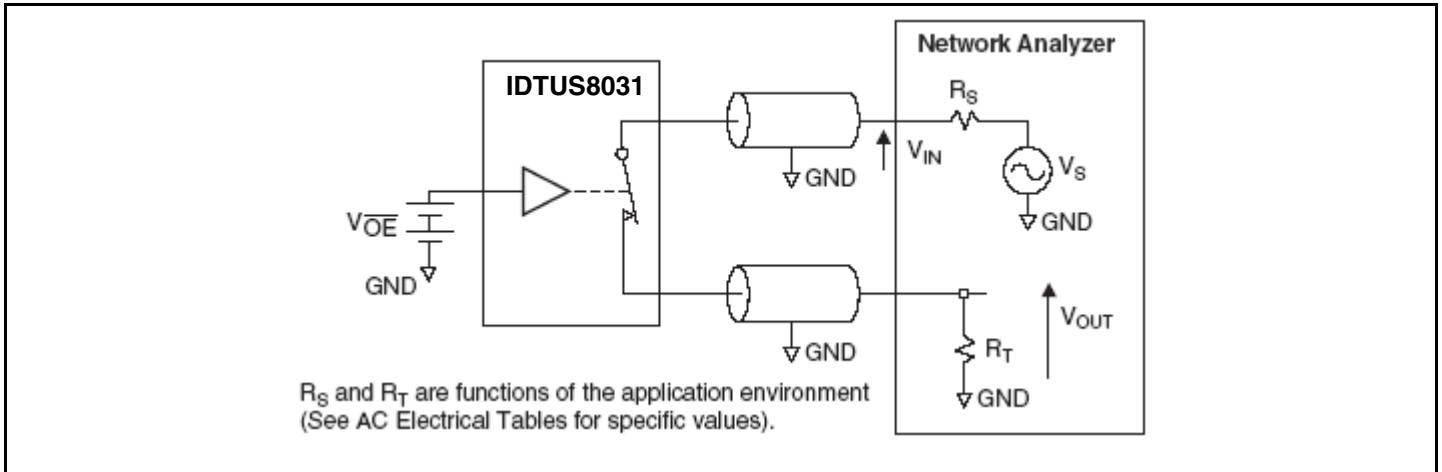
Switch Propagation Delay Waveforms (T$_{PD}$)

Turn ON / Turn OFF Waveform (T$_{ON}$ / T$_{OFF}$)
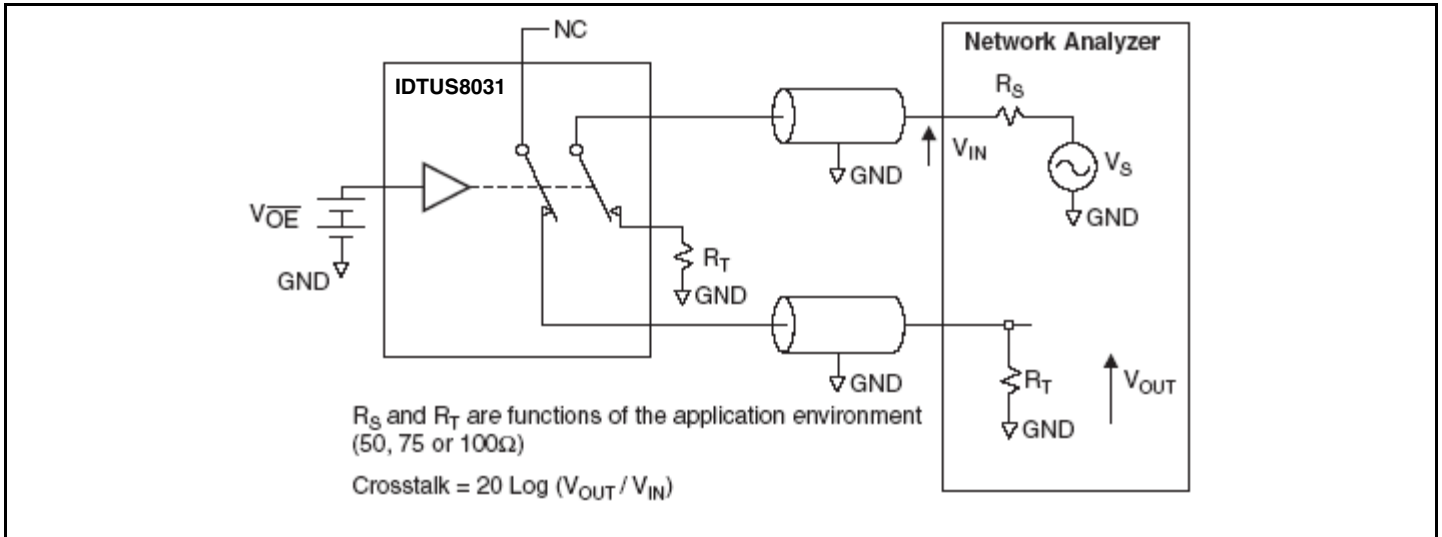
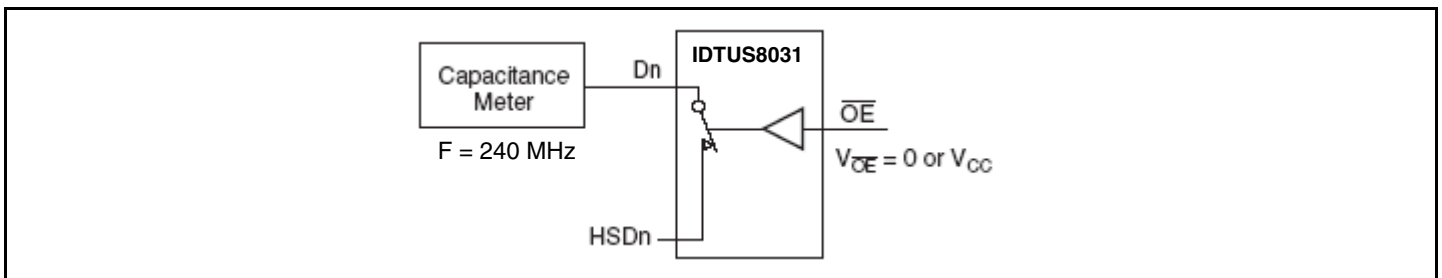**Break-Before-Make (T$_{BBM}$)**
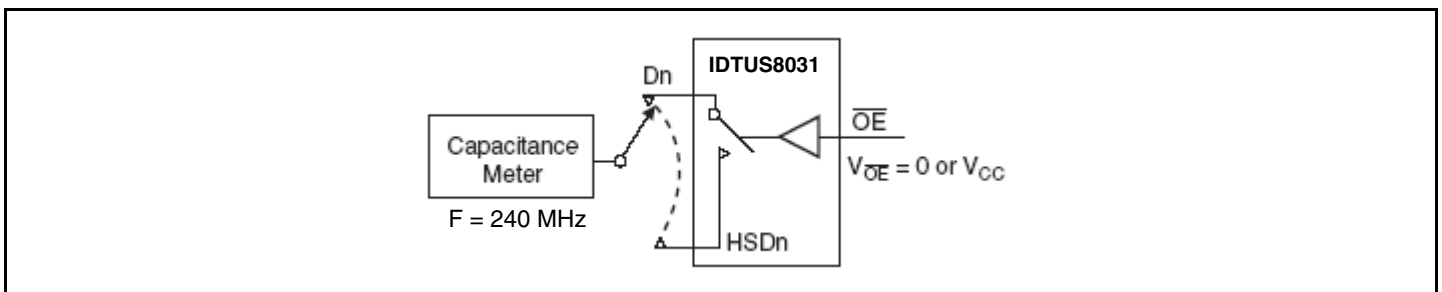

Switch Skew Tests

Bandwidth
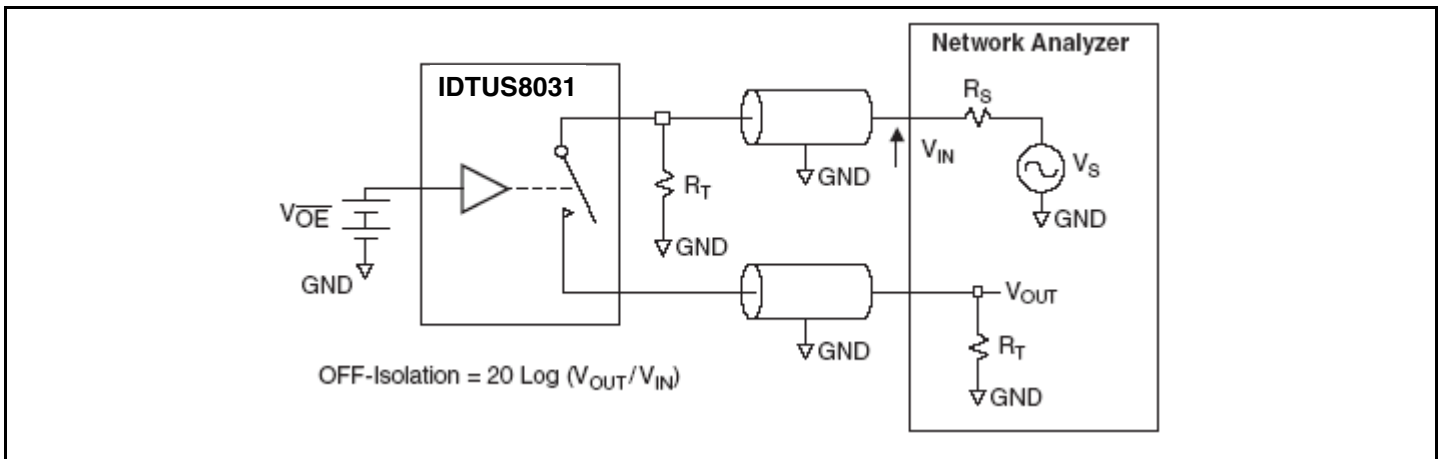
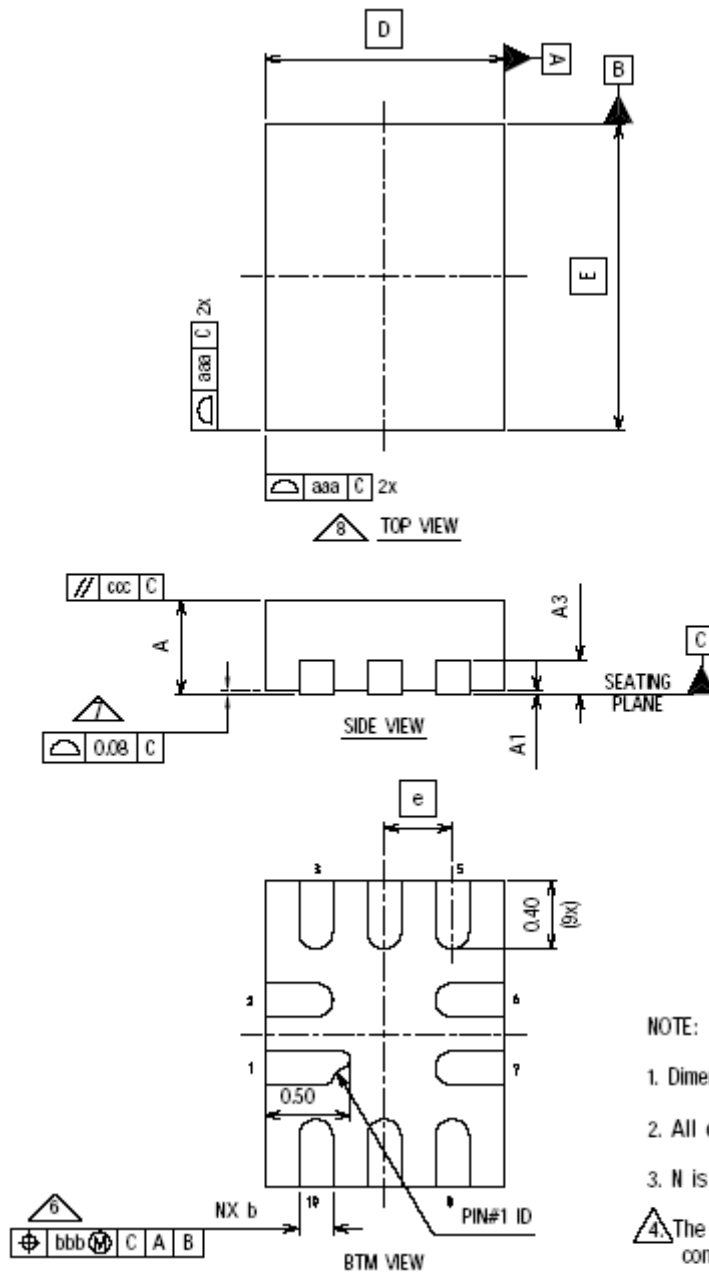**Channel OFF Isolation**

Non-Adjacent Channel-to-Channel Crosstalk

Channel ON Capacitance

Channel OFF Capacitance

Package Outline and Package Dimensions (10-pin µMLP)
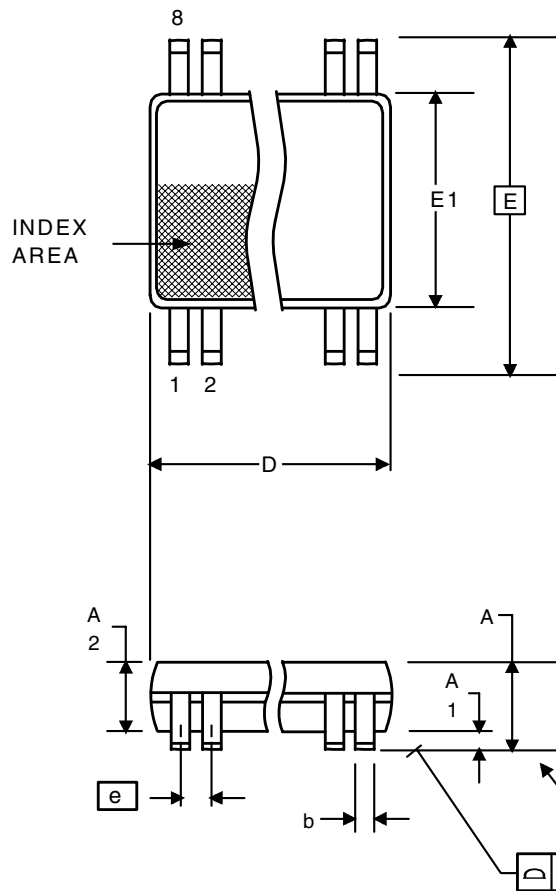
SYMBOL	Millimeters			
	MIN	NOM	MAX	Notes
A	0.51	0.55	0.60	1, 2
A1	0.00	0.02	0.05	1, 2
A3		0.15 ref		1, 2
b	0.15	0.20	0.25	
c	0.09		0.20	
D	1.40 BASIC			
E	1.80 BASIC			
E1	6.00		6.20	
N	10			3
ND	3			5
NE	2			5
e	0.40			
aaa	0.15			
bbb	0.10			

TOP VIEW

SIDE VIEW

BTM VIEW

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.

2. All dimensions are in millimeters, angles are in degrees(°).

3. N is the total number of terminals.

4. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.

5. ND and NE refer to the number of terminals on each D and E side respectively.

6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

7. Coplanarity applies to the terminals and all other bottom surface metallization.

8. Drawing shown are for illustration only.

Package Outline and Package Dimensions (8-pin MSOP, 3.00 mm Body)

Package dimensions are kept current with JEDEC Publication No. 95

Symbol	Millimeters		Inches*	
	Min	Max	Min	Max
A	--	1.10	--	0.043
A1	0	0.15	0	0.006
A2	0.79	0.97	0.031	0.038
b	0.22	0.38	0.008	0.015
C	0.08	0.23	0.003	0.009
D	3.00 BASIC		0.118 BASIC	
E	4.90 BASIC		0.193 BASIC	
E1	3.00 BASIC		0.118 BASIC	
e	0.65 Basic		0.0256 Basic	
L	0.40	0.80	0.016	0.032
α	0°	8°	0°	8°
aaa	-	0.10	-	0.004

*For reference only. Controlling dimensions in mm.
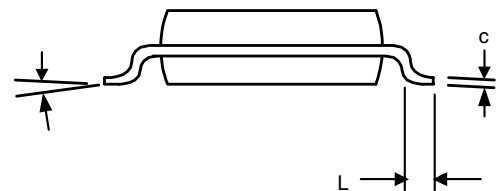
Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
US8031DVGI	TBD	Tubes	8-pin MSOP	-40°C to +85°C
US8031DVGI8	TBD	Tape and Reel	8-pin MSOP	-40°C to +85°C
US8031NDGI	TBD	Tubes	10-pin µMLP	-40°C to +85°C
US8031NDGI8	TBD	Tape and Reel	10-pin µMLP	-40°C to +85°C

Parts that are ordered with a "G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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Revision History

Rev.	Originator	Date	Description of Change
E		02/06/09	Added 10-pin MLP package.
F		03/02/09	Moved HSD-/+ pins on pinout diagram to pin 1 and 2 respectively.

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