

MC14016B

Quad Analog Switch/ Quad Multiplexer

The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise – $12 \text{ nV}/\sqrt{\text{Cycle}}$, $f \geq 1.0 \text{ kHz}$ typical
- Pin-for-Pin Replacements for CD4016B, CD4066B (Note improved transfer characteristic design causes more parasitic coupling capacitance than CD4016)
- For Lower R_{ON} , Use The HC4016 High-Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.
- These are Pb-Free Devices

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient) per Control Pin	± 10	mA
I_{SW}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$ From 65 $^{\circ}\text{C}$ To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

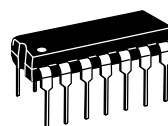
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



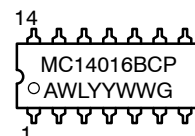
ON Semiconductor®

<http://onsemi.com>

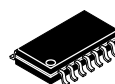
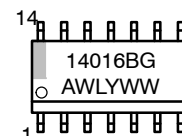
MARKING DIAGRAMS



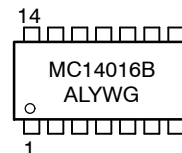
PDIP-14
P SUFFIX
CASE 646



SOIC-14
D SUFFIX
CASE 751A



SOEIAJ-14
F SUFFIX
CASE 965



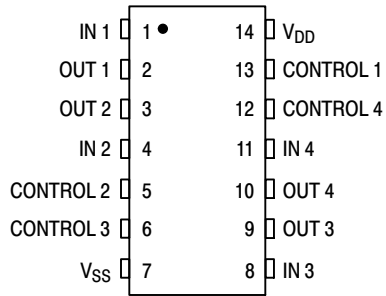
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

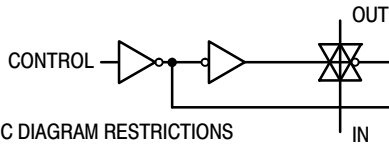
MC14016B

PIN ASSIGNMENT



LOGIC DIAGRAM

(1/4 OF DEVICE SHOWN)

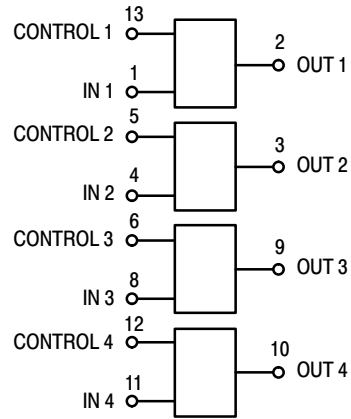


LOGIC DIAGRAM RESTRICTIONS

$$V_{SS} \leq V_{in} \leq V_{DD}$$

$$V_{SS} \leq V_{out} \leq V_{DD}$$

BLOCK DIAGRAM



$V_{DD} = \text{PIN } 14$
 $V_{SS} = \text{PIN } 7$

Control	Switch
0 = V_{SS}	Off
1 = V_{DD}	On

ORDERING INFORMATION

Device	Package	Shipping†
MC14016BCPG	PDIP-14 (Pb-Free)	25 / Tape & Ammo Box
MC14016BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14016BDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC14016BFELG	SOEIAJ-14 (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC14016B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Figure	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ ⁽²⁾	Max	Min	Max	
Input Voltage Control Input	1	V _{IL}	5.0	-	-	-	1.5	0.9	-	-	Vdc
			10	-	-	-	1.5	0.9	-	-	
15	-		-	-	-	-	1.5	0.9	-	-	
		V _{IH}	5.0	-	-	3.0	2.0	-	-	-	Vdc
			10	-	-	8.0	6.0	-	-	-	
			15	-	-	13	11	-	-	-	
Input Current Control	-	I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	± 1.0	µAdc
Input Capacitance Control Switch Input Switch Output Feed Through	-	C _{in}	-	-	-	-	5.0	-	-	-	pF
			-	-	-	-	5.0	-	-	-	
			-	-	-	-	5.0	-	-	-	
			-	-	-	-	0.2	-	-	-	
			-	-	-	-	0.2	-	-	-	
Quiescent Current (Per Package) ⁽³⁾	2,3	I _{DD}	5.0	-	0.25	-	0.0005	0.25	-	7.5	µAdc
			10	-	0.5	-	0.0010	0.5	-	15	
			15	-	1.0	-	0.0015	1.0	-	30	
"ON" Resistance (V _C = V _{DD} , R _L = 10 kΩ) (V _{in} = + 10 Vdc) (V _{in} = + 0.25 Vdc, V _{SS} = 0 Vdc) (V _{in} = + 5.6 Vdc) (V _{in} = + 15 Vdc) (V _{in} = + 0.25 Vdc, V _{SS} = 0 Vdc) (V _{in} = + 9.3 Vdc)	4,5,6	R _{ON}									Ohms
			10								
			15								
Δ "ON" Resistance Between any 2 circuits in a common package (V _C = V _{DD}) (V _{in} = + 5.0 Vdc, V _{SS} = - 5.0 Vdc) (V _{in} = + 7.5 Vdc, V _{SS} = - 7.5 Vdc)	-	ΔR _{ON}									Ohms
			5.0								
			7.5								
Input/Output Leakage Current (V _C = V _{SS}) (V _{in} = + 7.5, V _{out} = - 7.5 Vdc) (V _{in} = - 7.5, V _{out} = + 7.5 Vdc)	-	-									µAdc
			7.5		±0.1		±0.0015	±0.1		± 1.0	
			7.5		±0.1		±0.0015	±0.1		± 1.0	

NOTE: All unused inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. For voltage drops across the switch ($\Delta V_{\text{switch}} > 600 \text{ mV}$ ($> 300 \text{ mV}$ at high temperature), excessive V_{DD} current may be drawn; i.e., the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

MC14016B

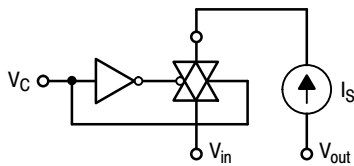
ELECTRICAL CHARACTERISTICS ⁽⁴⁾ ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Figure	Symbol	V _{DD} Vdc	Min	Typ ⁽⁵⁾	Max	Unit
Propagation Delay Time ($V_{SS} = 0 \text{ Vdc}$) V_{in} to V_{out} ($V_C = V_{DD}$, $R_L = 10 \text{ k}\Omega$)	7	t_{PLH} ,	5.0	–	15	45	ns
		t_{PHL}	10	–	7.0	20	
			15	–	6.0	15	
Control to Output ($V_{in} \leq 10 \text{ Vdc}$, $R_L = 10 \text{ k}\Omega$)	8	t_{PHZ} ,	5.0	–	34	120	ns
		t_{PLZ} ,	10	–	20	110	
		t_{PZH} ,	15	–	15	100	
		t_{PZL}					
Crosstalk, Control to Output ($V_{SS} = 0 \text{ Vdc}$) ($V_C = V_{DD}$, $R_{in} = 10 \text{ k}\Omega$, $R_{out} = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	9	–	5.0	–	30	–	mV
			10	–	50	–	
			15	–	100	–	
Crosstalk between any two switches ($V_{SS} = 0 \text{ Vdc}$) ($R_L = 1.0 \text{ k}\Omega$, $f = 1.0 \text{ MHz}$, crosstalk = $20 \log_{10} \frac{V_{out1}}{V_{out2}}$)	–	–	5.0	–	– 80	–	dB
Noise Voltage ($V_{SS} = 0 \text{ Vdc}$) ($V_C = V_{DD}$, $f = 100 \text{ Hz}$) ($V_C = V_{DD}$, $f = 100 \text{ kHz}$)	10,11	–	5.0	–	24	–	nV/ $\sqrt{\text{Cycle}}$
			10	–	25	–	
			15	–	30	–	
			5.0	–	12	–	
			10	–	12	–	
			15	–	15	–	
Second Harmonic Distortion ($V_{SS} = -5.0 \text{ Vdc}$) ($V_{in} = 1.77 \text{ Vdc}$, RMS Centered @ 0.0 Vdc , $R_L = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	–	–	5.0	–	0.16	–	%
Insertion Loss ($V_C = V_{DD}$, $V_{in} = 1.77 \text{ Vdc}$, $V_{SS} = -5.0 \text{ Vdc}$, RMS centered = 0.0 Vdc , $f = 1.0 \text{ MHz}$) $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$ ($R_L = 1.0 \text{ k}\Omega$) ($R_L = 10 \text{ k}\Omega$) ($R_L = 100 \text{ k}\Omega$) ($R_L = 1.0 \text{ M}\Omega$)	12	–	5.0				dB
				–	2.3	–	
				–	0.2	–	
				–	0.1	–	
				–	0.05	–	
Bandwidth (-3.0 dB) ($V_C = V_{DD}$, $V_{in} = 1.77 \text{ Vdc}$, $V_{SS} = -5.0 \text{ Vdc}$, RMS centered @ 0.0 Vdc) ($R_L = 1.0 \text{ k}\Omega$) ($R_L = 10 \text{ k}\Omega$) ($R_L = 100 \text{ k}\Omega$) ($R_L = 1.0 \text{ M}\Omega$)	12,13	BW	5.0				MHz
				–	54	–	
				–	40	–	
				–	38	–	
				–	37	–	
OFF Channel Feedthrough Attenuation ($V_{SS} = -5.0 \text{ Vdc}$) ($V_C = V_{SS}$, $20 \log_{10} \frac{V_{out}}{V_{in}} = -50 \text{ dB}$) ($R_L = 1.0 \text{ k}\Omega$) ($R_L = 10 \text{ k}\Omega$) ($R_L = 100 \text{ k}\Omega$) ($R_L = 1.0 \text{ M}\Omega$)	–	–	5.0				kHz
				–	1250	–	
				–	140	–	
				–	18	–	
				–	2.0	–	

4. The formulas given are for typical characteristics only at 25°C .

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14016B



V_{IL} : V_C is raised from V_{SS} until $V_C = V_{IL}$.
 at $V_C = V_{IL}$: $I_S = \pm 10 \mu A$ with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.
 V_{IH} : When $V_C = V_{IH}$ to V_{DD} , the switch is ON and the R_{ON} specifications are met.

Figure 1. Input Voltage Test Circuit

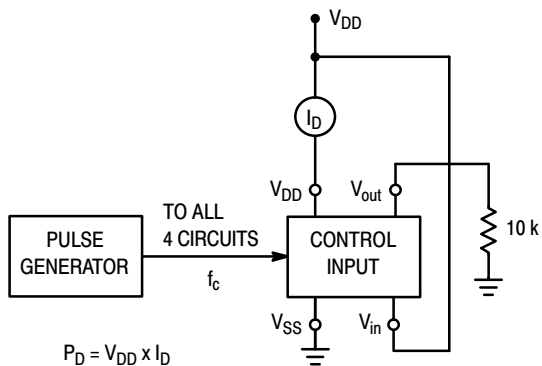


Figure 2. Quiescent Power Dissipation Test Circuit

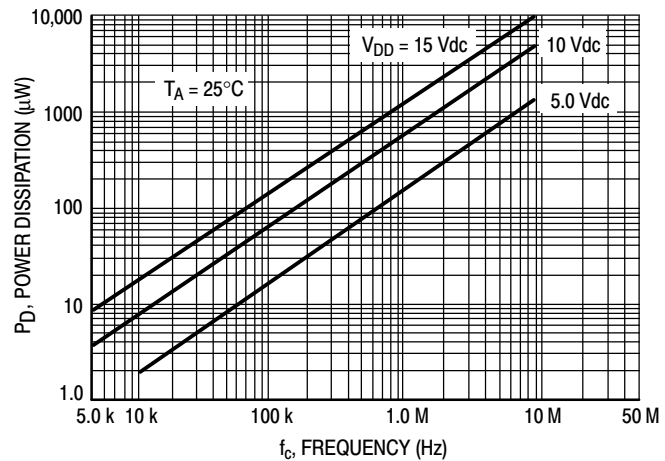


Figure 3. Typical Power Dissipation per Circuit (1/4 of device shown)

TYPICAL R_{ON} versus INPUT VOLTAGE

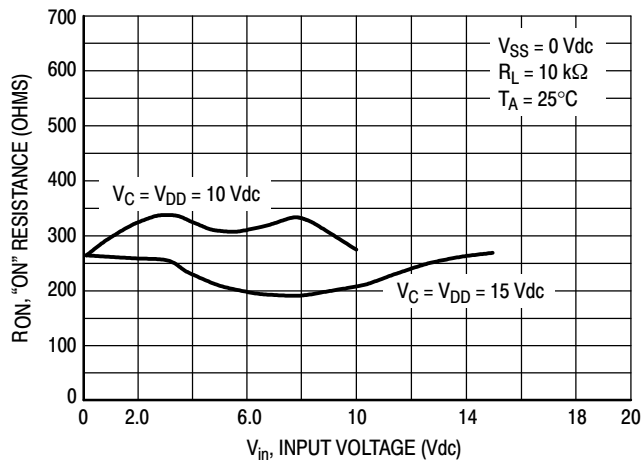


Figure 4. $V_{SS} = 0 V$

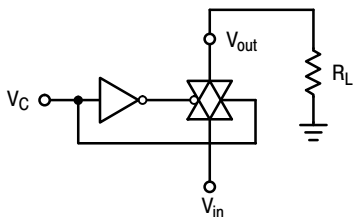


Figure 5. R_{ON} Characteristics Test Circuit

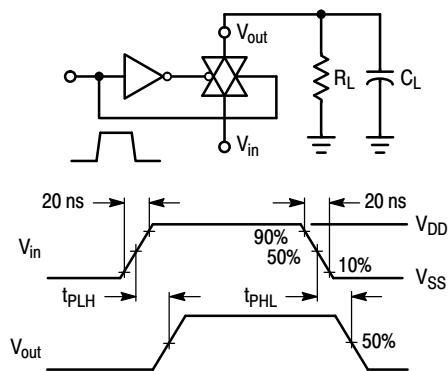


Figure 6. Propagation Delay Test Circuit and Waveforms

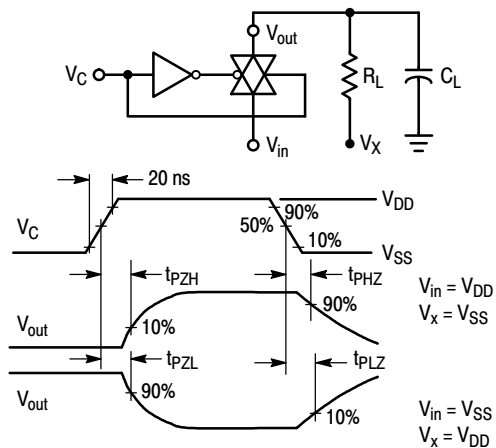


Figure 7. Turn-On Delay Time Test Circuit and Waveforms

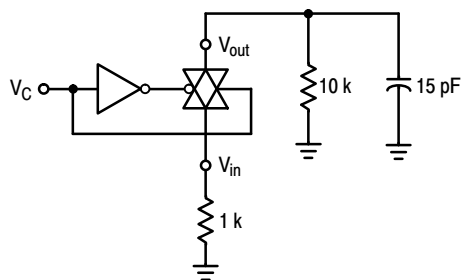


Figure 8. Crosstalk Test Circuit

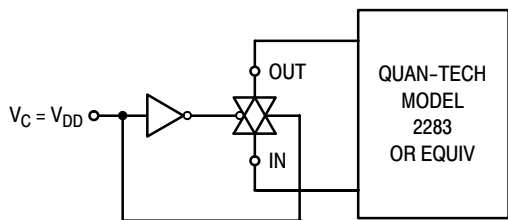


Figure 9. Noise Voltage Test Circuit

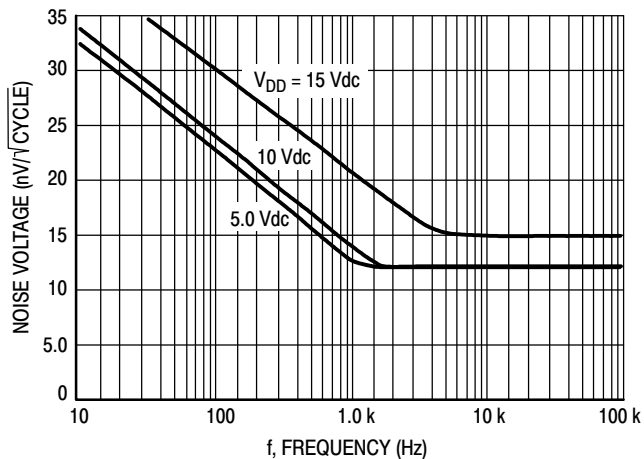


Figure 10. Typical Noise Characteristics

MC14016B

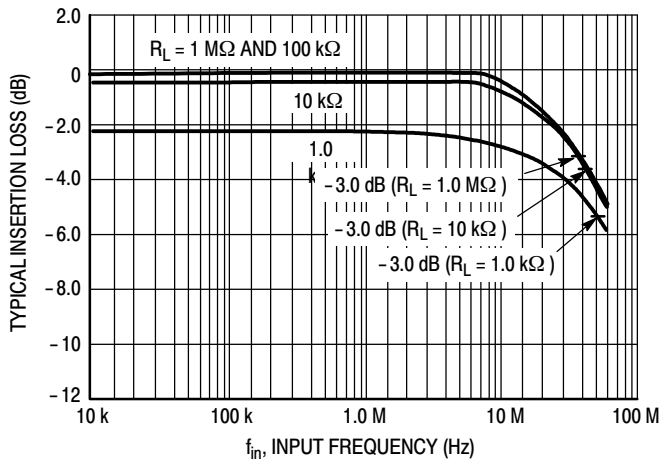


Figure 11. Typical Insertion Loss/Bandwidth Characteristics

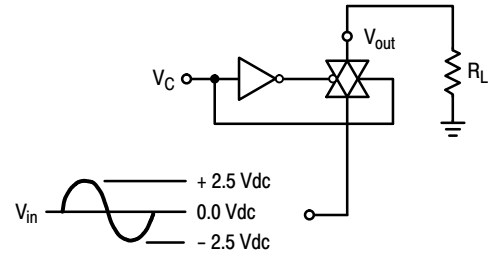


Figure 12. Frequency Response Test Circuit

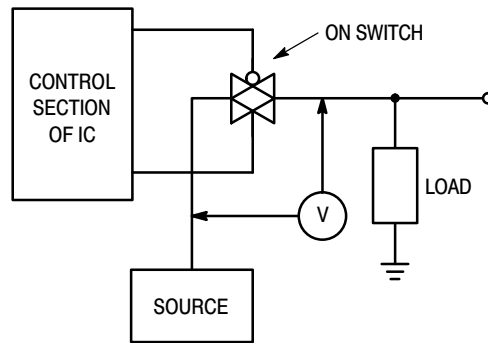


Figure 13. ΔV Across Switch

MC14016B

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 V Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V logic high at the control inputs; V_{SS} = GND = 0 V logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{SS}.

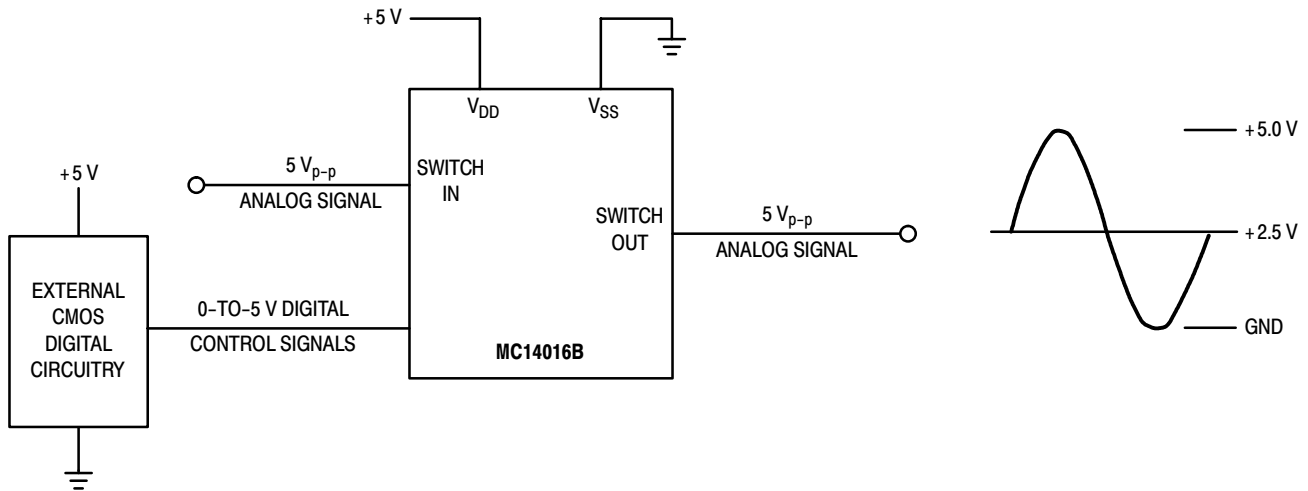


Figure A. Application Example

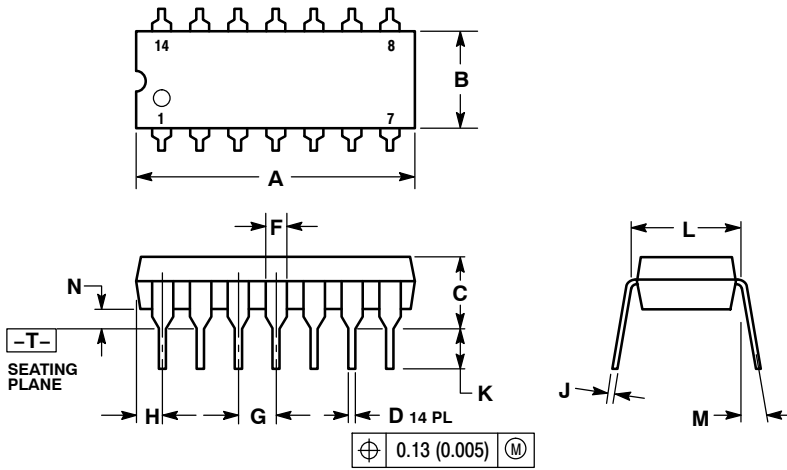


Figure B. External Germanium or Schottky Clipping Diodes

MC14016B

PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



NOTES:

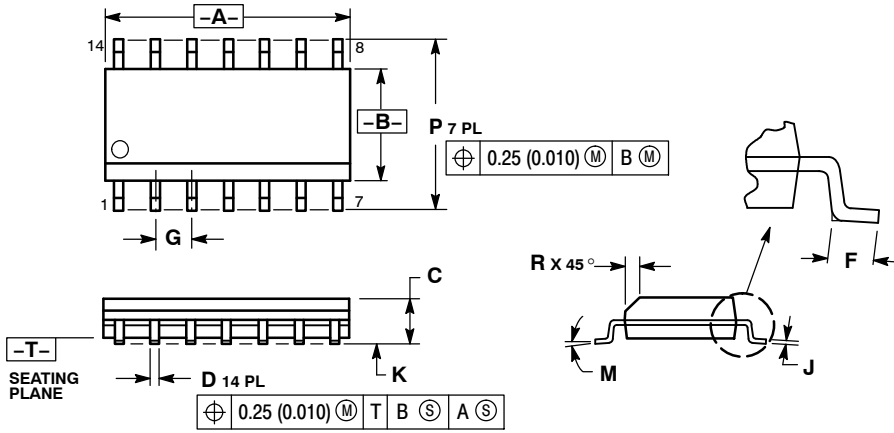
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

MC14016B

PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE J

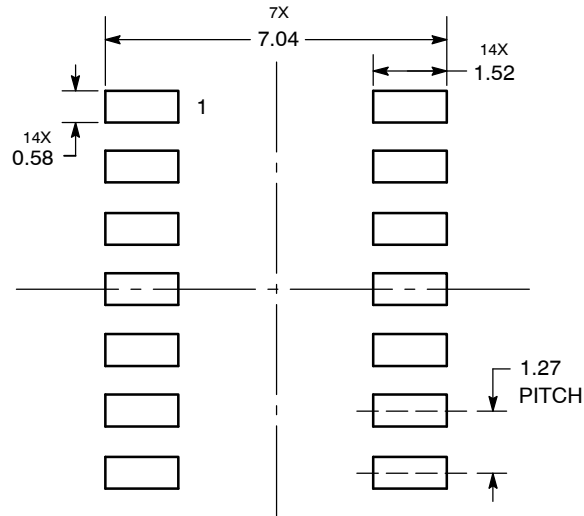


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° - 7°		0° - 7°	
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



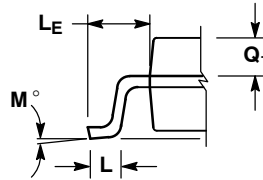
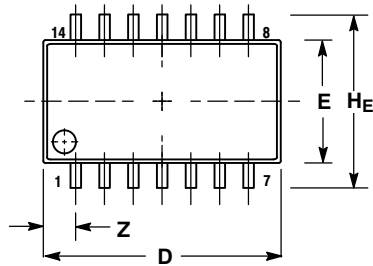
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

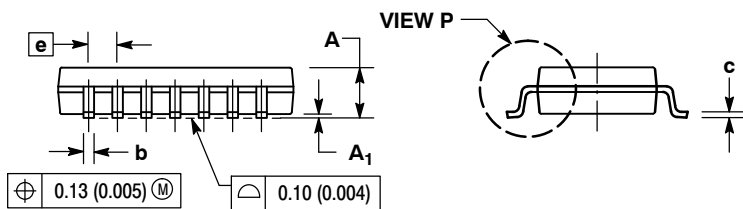
MC14016B

PACKAGE DIMENSIONS

SOEIAJ-14
CASE 965-01
ISSUE B



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

MC14016B/D