

# Low Voltage, 1-Ω Single SPDT Analog Switch (1:2 Multiplexer) with Power Down Protection

## DESCRIPTION

The DG4157 is a high performance single pole double throw analog switch designed for 1.65 V to 5.5 V operation with single power rail.

Fabricated with high density CMOS technology, the device achieves low on resistance as 1 Ω at 4.5 V power supply and fast switching speed. The - 3 dB bandwidth is typically 117 MHz.

The DG4157 features break before make switch performance, and guarantees logic high control input threshold as low as 1.4 V over the range up to 5.5 V.

It can handle both analog and digital signals and permits signals with amplitudes of up to  $V_{CC}$  to be transmitted in either direction.

Power down protection circuit is built in to prevent abnormal current path through signal pins during power down condition.

Each output pin (A,  $B_0$ , or  $B_1$ ) can withstand greater than 8 kV (human body model).

It is available in both SC-70-6 and miniQFN6 packages.

The features make it an ideal part for the switching of audio, video, and data stream.

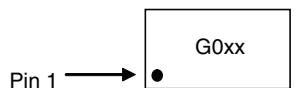
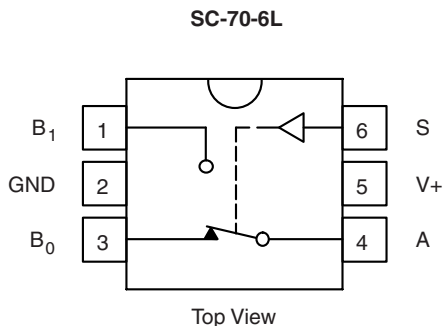
## FEATURES

- Direct cross of industry standard xxx4157
- 1.65 V to 5.5 V operation voltage range
- Guaranteed 1.4 V logic high input threshold at  $V_{CC} = 5.5$  V
- 117 MHz, - 3 dB bandwidth
- Low on-resistance
- Power down protection
- Compliant to RoHS directive 2002/95/EC

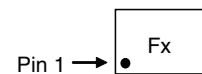
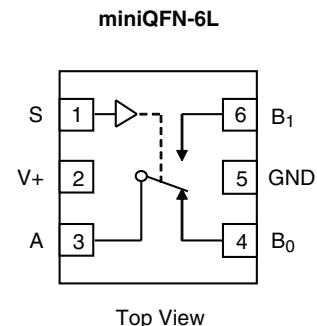


**RoHS\***  
COMPLIANT

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: G0xx  
xx = Date/Lot Traceability Code



Device Marking: Fx  
x = Date/Lot Traceability Code

TRUTH TABLE	
Logic Input (S)	Function
0	$B_0$ Connected to A
1	$B_1$ Connected to A

ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	SC-70-6L	DG4157DL-T1-E3
	miniQFN-6L	DG4157DN-T1-E4

\* Pb containing terminations are not RoHS compliant, exemptions may apply.

ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
S, A, B <sup>a</sup>		- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)		± 200	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 400	
Storage Temperature	D Suffix	- 65 to 150	°C
Power Dissipation (Packages) <sup>b</sup>	SC-70-6L <sup>c</sup>	250	mW
	miniQFN-6L <sup>d</sup>	160	

Notes:

- a. Signals on A, or B or S exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 3.1 mW/°C above 70 °C.
- d. Derate 2.0 mW/°C above 70 °C.

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3.0 V, V <sub>IN</sub> = 0 V or V+ <sup>e</sup>	Temp. <sup>a</sup>	Limits - 40 °C to 85 °C			Unit
				Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>	
<b>DC Characteristics</b>							
On Resistance	R <sub>ON</sub>	V+ = 2.7 V, B <sub>0</sub> or B <sub>1</sub> = 1.5 V, I <sub>O</sub> = 100 mA	Room		1.7	2.5	Ω
			Full			3	
		V+ = 4.5 V, B <sub>0</sub> or B <sub>1</sub> = 3.5 V, I <sub>O</sub> = 100 mA	Room		0.95	1.2	
			Full			1.4	
On Resistance Flatness	R <sub>FLATNESS</sub>	V+ = 2.7 V, B <sub>0</sub> or B <sub>1</sub> = 0.75 V, 1.5 V, I <sub>O</sub> = 100 mA	Room		0.2		
			Full				
		V+ = 4.5 V, B <sub>0</sub> or B <sub>1</sub> = 1 V, 3.5 V, I <sub>O</sub> = 100 mA	Room		0.14	0.3	
			Full			0.4	
On Resistance Match	ΔR <sub>ON</sub>	V+ = 2.7 V, B <sub>0</sub> or B <sub>1</sub> = 1.5 V, I <sub>O</sub> = 100 mA	Room		0.04		
			Full				
		V+ = 4.5 V, B <sub>0</sub> or B <sub>1</sub> = 3.5 V, I <sub>O</sub> = 100 mA	Room		0.05	0.12	
			Full			0.15	
Switch Off Leakage Current	I <sub>OFF</sub>	V+ = 5.5 V, A = 1 V, 4.5 V B <sub>0</sub> or B <sub>1</sub> = 4.5 V, 1 V or Floating	Room	- 2		2	nA
Switch On Leakage Current	I <sub>ON</sub>		Full	- 20		20	
			Room	- 4		4	
			Full	- 40		40	
<b>Digital Control</b>							
Input, High Voltage	V <sub>INH</sub>	V+ = 2.7 V to 5.5 V	Full	1.4			V
Input, Low Voltage	V <sub>INL</sub>		Full			0.4	
Input Current	I <sub>INH</sub> , I <sub>INL</sub>	V <sub>IN</sub> = 0 or V+	Full	- 1		1	μA
<b>Power Supply</b>							
Power Supply Range	V+		Full	1.65		5.5	V
Quiescent Supply Current	I+	V+ = 5.5 V, V <sub>IN</sub> = 0 V, 5.5 V	Room		0.05	0.5	μA
			Full			1	

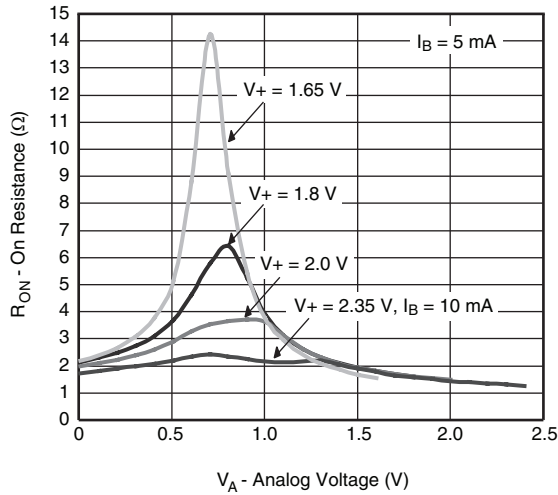
<b>SPECIFICATIONS</b>							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 3.0\text{ V}$ , $V_{IN} = 0\text{ V}$ or $V_+^e$	Temp. <sup>a</sup>	Limits - 40 °C to 85 °C			Unit
				Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>	
<b>AC Characteristics</b>							
Turn-On Time <sup>d</sup>	$t_{ON}$	$V_+ = 2.7\text{ V}$ , $B_0$ or $B_1 = 1.5\text{ V}$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$	Room		40	55	ns
			Full			60	
		$V_+ = 4.5\text{ V}$ , $B_0$ or $B_1 = 1.5\text{ V}$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$	Room		22	37	
			Full			40	
Turn-Off Time <sup>d</sup>	$t_{OFF}$	$V_+ = 2.7\text{ V}$ , $B_0$ or $B_1 = 1.5\text{ V}$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$	Room		12	27	
			Full			30	
		$V_+ = 4.5\text{ V}$ , $B_0$ or $B_1 = 1.5\text{ V}$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$	Room		8	23	
			Full			25	
Break-Before-Make Time <sup>d</sup>	$t_{BBM}$	$V_+ = 2.7\text{ V}$ , $B_0 = B_1 = 1.5\text{ V}$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$	Room	1	26		
		$V_+ = 4.5\text{ V}$ , $B_0 = B_1 = 1.5\text{ V}$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$		1	15		
Charge Injection <sup>d</sup>	Q	$C_L = 1\text{ nF}$ , $R_{GEN} = 0\ \Omega$ , $V_{GEN} = 0\text{ V}$	Room		50		pC
Off Isolation <sup>d</sup>	OIRR	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$	Room		- 58		dB
		$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$			- 31		
Crosstalk <sup>d</sup>	$X_{TALK}$	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$	Room		- 63		dB
		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$			- 36		
Bandwidth <sup>d</sup>	BW	$R_L = 50\ \Omega$	Room		117		MHz
Total Harmonic Distortion <sup>d</sup>	THD	$R_L = 600\ \Omega$ , $V_{IN} = 0.5\text{ V}$ , $f = 20\text{ to }20\text{ kHz}$	Room		0.02		%
<b>Capacitance</b>							
BX Port Off Capacitance <sup>d</sup>	$C_{B(OFF)}$	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$	Room		20		pF
A Port On Capacitance <sup>d</sup>	$C_{A(ON)}$				57		
Control Pin Capacitance <sup>d</sup>	$C_{IN}$				5		

Notes:

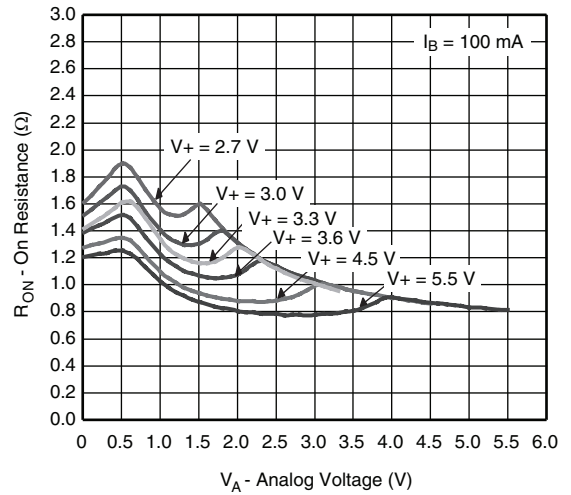
- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, nor subjected to production test.
- e.  $V_{IN}$  = input voltage to perform proper function.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

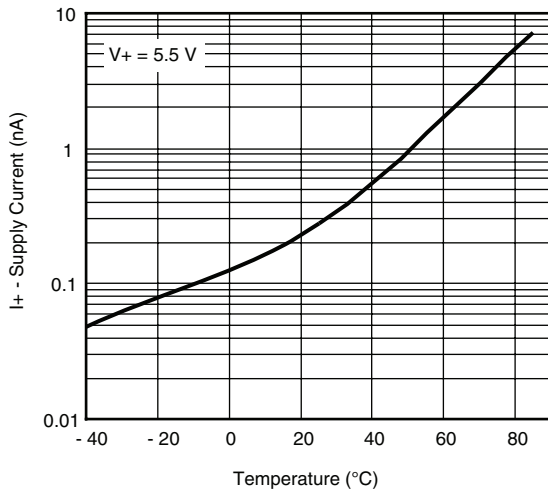
**TYPICAL CHARACTERISTICS**  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted



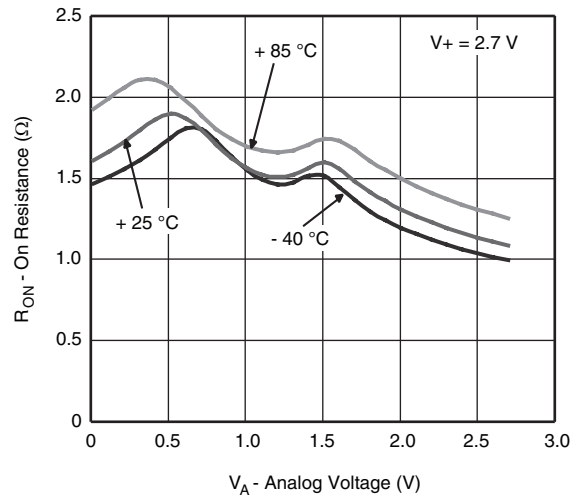
**$R_{ON}$  vs.  $V_A$  and Supply Voltage**



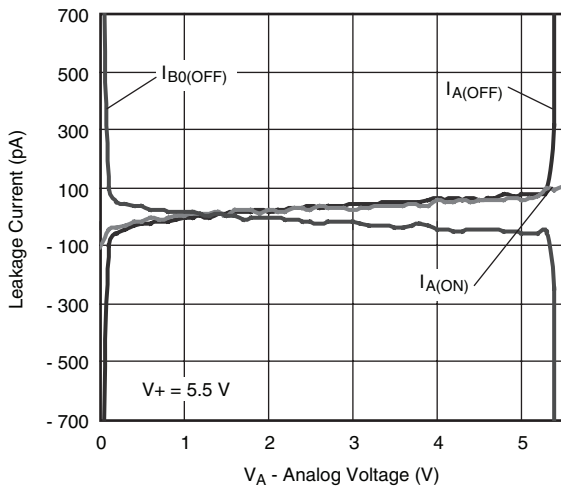
**$R_{ON}$  vs.  $V_A$  and Supply Voltage**



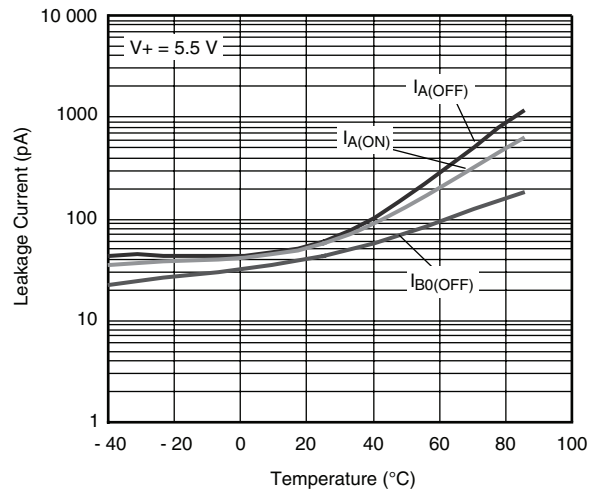
**Supply Current vs. Temperature**



**$R_{ON}$  vs.  $V_D$  and Temperature**

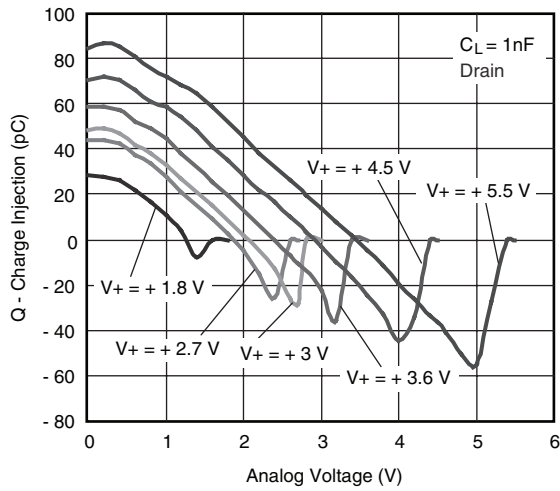


**Leakage vs. Analog Voltage**

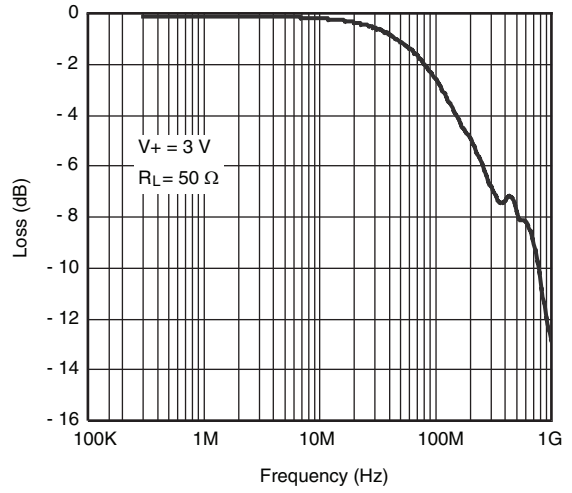


**Leakage Current vs. Temperature**

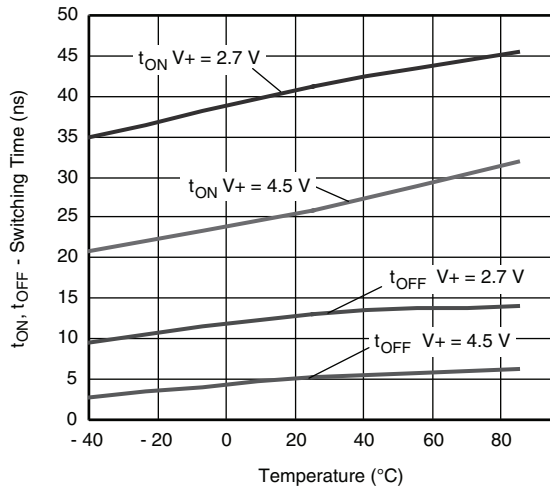
**TYPICAL CHARACTERISTICS**  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted



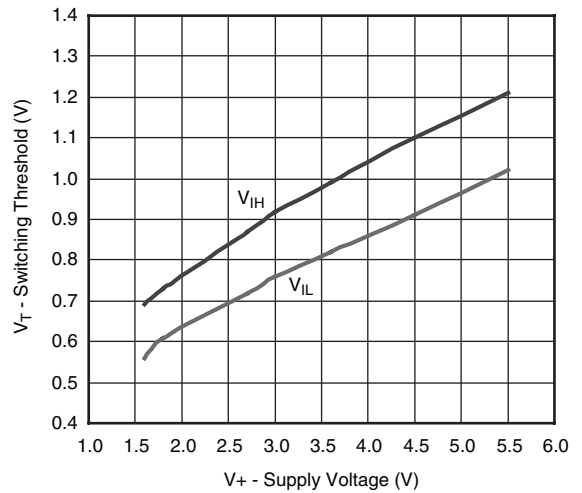
**Charge Injection vs. Analog Voltage**



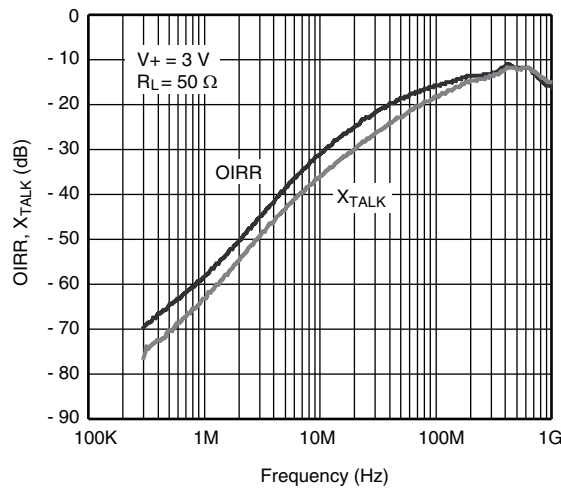
**Insertion Loss vs. Frequency**



**Switching Time vs. Temperature**

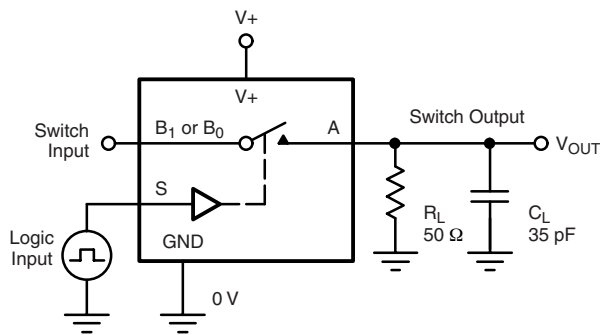


**Switching Threshold vs. Supply Voltage**



**Off-Isolation and Crosstalk vs. Frequency**

TEST CIRCUITS



$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_A \left( \frac{R_L}{R_L + R_{ON}} \right)$$

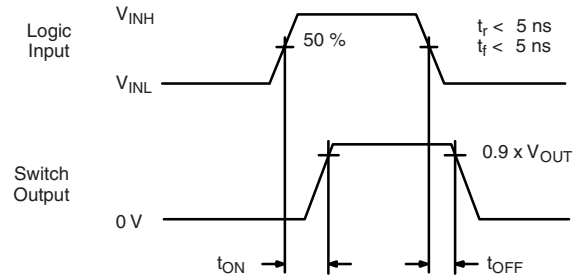
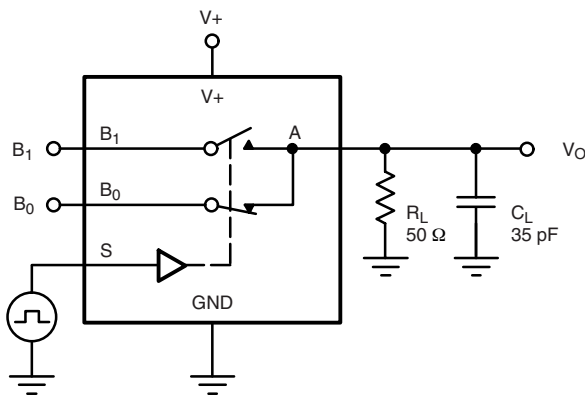


Figure 1. Switching Time



$C_L$  (includes fixture and stray capacitance)

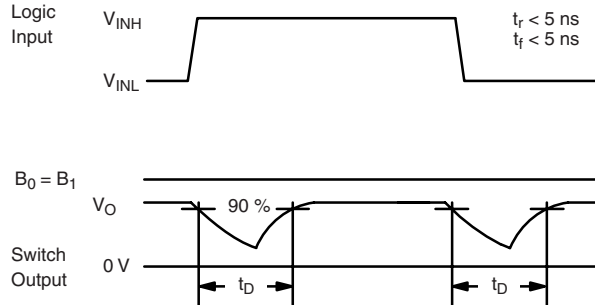
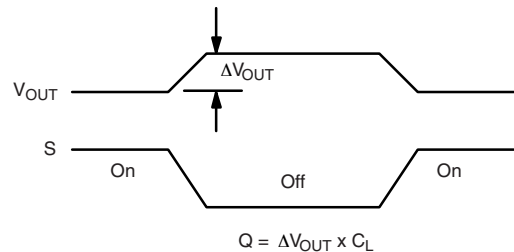
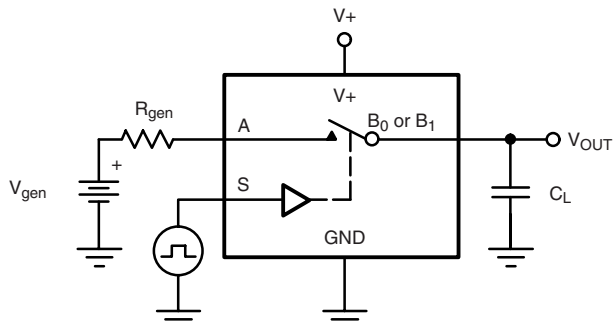


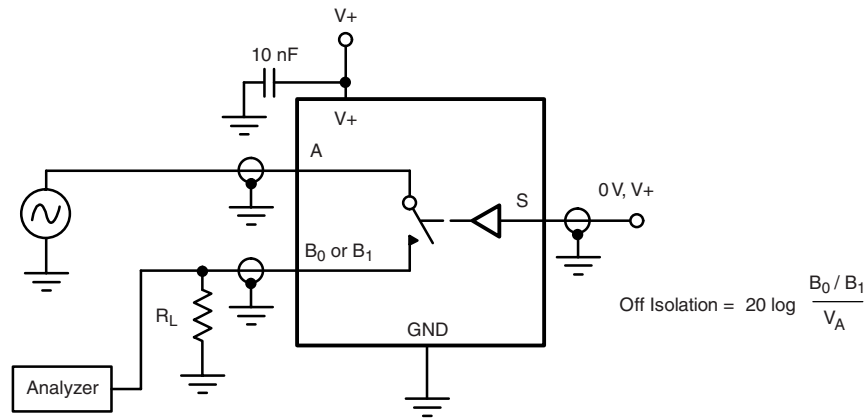
Figure 2. Break-Before-Make Interval



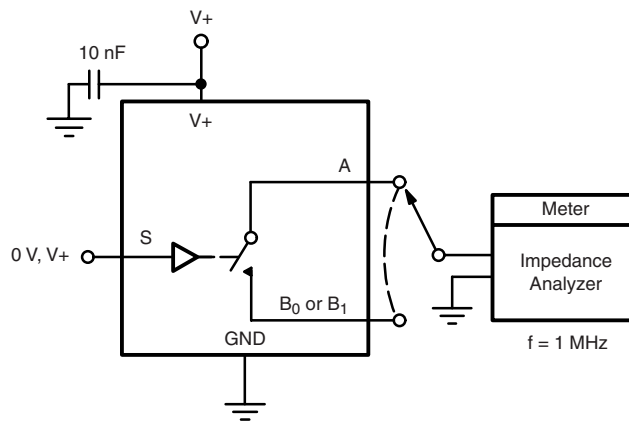
S depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

**TEST CIRCUITS**



**Figure 4. Off-Isolation**



**Figure 5. Channel Off/On Capacitance**

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