



0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

MAX4736

General Description

The MAX4736 is a low on-resistance, low-voltage, dual single-pole/double throw (SPDT) analog switch that operates from a single 1.6V to 4.2V supply. This device has fast switching speeds ($t_{ON} = 25ns$, $t_{OFF} = 20ns$ max), handles rail-to-rail analog signals, and consumes less than 4μW of quiescent power. The MAX4736 has break-before-make switching.

When powered from a 3V supply, the MAX4736 features low 0.6Ω on-resistance (R_{ON}), with 0.1Ω R_{ON} matching and 0.05Ω R_{ON} flatness. The digital logic input is 1.8V CMOS compatible when using a single 3V supply.

The MAX4736 has one normally open (NO) switch and one normally closed (NC) switch, and is available in 12-pin TQFN-EP (3mm x 3mm), 10-pin μMAX and 10 pin μDFN (2mm x 2mm) packages.

Applications

- Power Routing
- Battery-Powered Systems
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits
- PCMCIA Cards
- Cellular Phones
- Modems
- Hard Drives

Features

- ◆ **Low R_{ON}**
0.6Ω (3V Supply)
1.5Ω (1.8V Supply)
- ◆ **0.1Ω max R_{ON} Flatness (3V Supply)**
- ◆ **Single-Supply Operation Down to 1.6V**
- ◆ **Available in TQFN, μDFN and μMAX Packages**
- ◆ **1.8V CMOS Logic Compatible (3V Supply)**
- ◆ **Fast Switching: $t_{ON} = 25ns$, $t_{OFF} = 20ns$**

Ordering Information

PART	PIN-PACKAGE	PKG CODE
MAX4736EUB	10 μMAX	U10-2
MAX4736ETC	12 Thin QFN-EP*	T1233-1
MAX4736ELB	10 μDFN	L1022-1

Note: All devices operate over the -40°C to +55°C operating temperature range.

*EP = Exposed pad.

Pin Configurations/Functional Diagrams/Truth Table

TOP VIEW

TQFN

μMAX/μDFN

MAX4736		
IN_	NO_	NC_
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC 0 INPUT

NOTE: CONNECT EXPOSED PAD ON TQFN AND μDFN TO GND.

0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V+, IN_	-0.3V to +4.6V
COM_, NO_, NC_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current COM_, NO_, NC_	±300mA
Continuous Current (all other pins)	±20mA
Peak Current COM_, NO_, NC_ (pulsed at 1ms 10% duty cycle)	±500mA

Continuous Power Dissipation (T_A = +70°C)

10-Pin μDFN (derate 5.3mW/°C above +70°C)	423.7mW
10-Pin μMAX (derate 5.6mW/°C above +70°C)	444mW
12-Pin TQFN-EP (derate 14.7mW/°C above +70°C)	1176mW
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signals on COM_, NO_, or NC_ exceeding V+ or GND are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single 3V Supply

(V+ = 2.7V to 4.2V, V_{IH} = 1.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V+ = 3.0V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{COM_} , V _{NO_} , V _{NC_}			0		V+	V
On-Resistance (Note 4)	R _{ON}	V+ = 2.7V, I _{COM_} = 100mA; V _{NO_} or V _{NC_} = 1.5V	+25°C		0.6	0.8	Ω
			T _{MIN} to T _{MAX}			1	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR _{ON}	V+ = 2.7V, I _{COM_} = 100mA; V _{NO_} or V _{NC_} = 1.5V	+25°C		0.1	0.2	Ω
			T _{MIN} to T _{MAX}			0.3	
On-Resistance Flatness (Note 6)	R _{FLAT(ON)}	V+ = 2.7V, I _{COM_} = 100mA; V _{NO_} or V _{NC_} = 1V, 1.5V, 2V	+25°C		0.05	0.1	Ω
			T _{MIN} to T _{MAX}			0.2	
NO_ or NC_ Off-Leakage Current (Note 10)	I _{NO_ (OFF)} , I _{NC_ (OFF)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.3V; V _{NO_} or V _{NC_} = 3.3V, 0.3V	+25°C	-1	±0.002	+1	nA
			T _{MIN} to T _{MAX}		-5		
COM_ On-Leakage Current (Note 10)	I _{COM_(ON)}	V+ = 3.6V, V _{COM_} = 0.3V, 3.3V; V _{NO_} or V _{NC_} = 0.3V, 3.3V, or floating	+25°C	-2	±0.002	+2	nA
			T _{MIN} to T _{MAX}		-10		

0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

MAX4736

ELECTRICAL CHARACTERISTICS—Single 3V Supply (continued)

(V+ = 2.7V to 4.2V, V_{IH} = 1.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V+ = 3.0V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t _{ON}	V _{NO_} , V _{NC_} = 1.5V; R _L = 50Ω, C _L = 35pF, Figure 1	+25°C		20	25	ns
			T _{MIN} to T _{MAX}			30	
Turn-Off Time	t _{OFF}	V _{NO_} , V _{NC_} = 1.5V; R _L = 50Ω, C _L = 35pF, Figure 1	+25°C		15	20	ns
			T _{MIN} to T _{MAX}			25	
Break-Before-Make (Note 7)	t _{BBM}	V _{NO_} , V _{NC_} = 1.5V; R _L = 50Ω, C _L = 35pF, Figure 2	+25°C		5		ns
			T _{MIN} to T _{MAX}		1		
Charge Injection	Q	V _{GEN} = 0, R _{GEN} = 0, C _L = 1.0nF, Figure 3	+25°C		60		pC
NO_ or NC_ Off-Capacitance	C _{OFF}	f = 1MHz, Figure 4	+25°C		33		pF
COM_ Off-Capacitance	C _{COM(OFF)}	f = 1MHz, Figure 4	+25°C		60		pF
COM_ On-Capacitance	C _{COM(ON)}	f = 1MHz, Figure 4	+25°C		85		pF
-3dB On-Channel Bandwidth	BW	Signal = 0, R _{IN} = R _{OUT} = 50Ω, C _L = 5pF, Figure 5			130		MHz
Off-Isolation (Note 8)	V _{ISO}	f = 1MHz, V _{COM_} = 1V _{P-P} , R _L = 50Ω, C _L = 5pF, Figure 5	+25°C		-52		dB
Crosstalk (Note 9)	V _{CT}	f = 1MHz, V _{COM_} = 1V _{P-P} , R _L = 50Ω, C _L = 5pF, Figure 5	+25°C		-78		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, V _{COM_} = 2V _{P-P} , R _L = 32Ω	+25°C		0.018		%
LOGIC INPUT (A_, IN_)							
Input Logic High	V _{IH}			1.4			V
Input Logic Low	V _{IL}					0.5	V
Input Leakage Current	I _{IN}	V _{IN_} = 0 or 3.6V		-1	+0.005	+1	μA
POWER SUPPLY							
Power-Supply Range	V+			1.6		3.6	V
Positive Supply Current	I+	V+ = 3.6V, V _{IN_} = 0 or V+, all channels on or off			0.006	1	μA

0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

ELECTRICAL CHARACTERISTICS—Single 1.8V Supply

($V_+ = 1.8V$, $V_{IH} = 1.0V$, $V_{IL} = 0.4V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise specified. Typical values are at $T_A = +25^\circ C$.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$			0		V_+	V
On-Resistance	R_{ON}	$I_{COM_} = 10mA$; $V_{NO_}$ or $V_{NC_} = 1V$	+25°C	1.5	2		Ω
			T_{MIN} to T_{MAX}			3	
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO_}$ or $V_{NC_} = 1V$; $R_L = 50\Omega$, $C_L = 35pF$, Figure 1	+25°C	25	30		ns
			T_{MIN} to T_{MAX}			35	
Turn-Off Time	t_{OFF}	$V_{NO_}$ or $V_{NC_} = 1V$; $R_L = 50\Omega$, $C_L = 35pF$, Figure 1	+25°C	18	25		ns
			T_{MIN} to T_{MAX}			28	
Break-Before-Make (Note 7)	t_{BBM}	$V_{NO_}$ or $V_{NC_} = 1V$; $R_L = 50\Omega$, $C_L = 35pF$, Figure 2	+25°C	7			ns
			T_{MIN} to T_{MAX}	1			
Charge Injection	Q	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1nF$, Figure 3	+25°C		35		pC
Off-Isolation (Note 8)	V_{ISO}	$f = 1MHz$, $V_{NO_} = V_{NC_}$ $= 1V_{P-P}$, $R_L = 50\Omega$, $C_L = 5pF$, Figure 5	+25°C		-52		dB
Crosstalk (Note 9)	V_{CT}	$f = 1MHz$, $V_{COM_} = 1V_{P-P}$, $R_L = 50\Omega$, $C_L = 5pF$, Figure 5	+25°C		-78		dB
LOGIC INPUT (IN_)							
Input Logic High	V_{IH}			1			V
Input Logic Low	V_{IL}					0.4	V
Input Leakage Current	I_{IN}	$V_{IN_} = 0$ or $3.6V$				1	μA

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value is a maximum, is used in this data sheet.

Note 3: -40°C specifications are guaranteed by design.

Note 4: R_{ON} and ΔR_{ON} matching specifications for QFN packaged parts are guaranteed by design.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Guaranteed by design.

Note 8: Off-Isolation = $20\log_{10}(V_{COM_}/V_{NO_})$, $V_{COM_}$ = output, $V_{NO_}$ = input to OFF switch.

Note 9: Between two switches.

Note 10: Leakage parameters are 100% tested at hot temperature and guaranteed by correlation at room.

Note 11: Devices are guaranteed to 1 million cycles of operation. (Cycle = switch on → switch off → switch on)

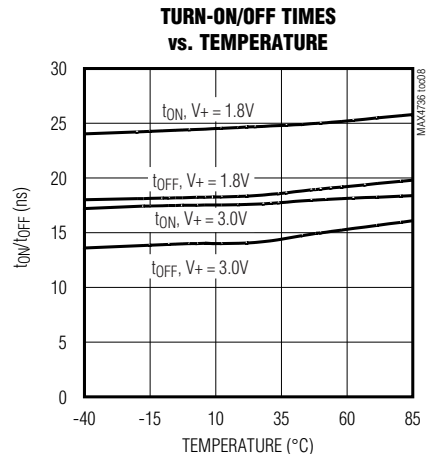
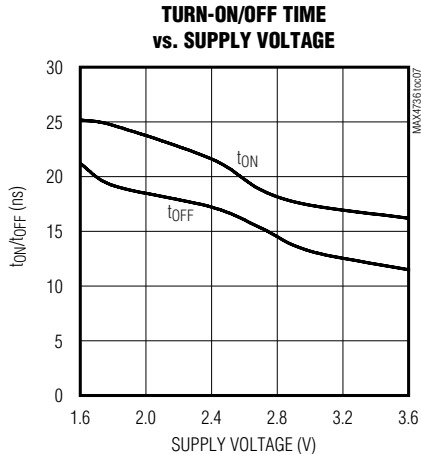
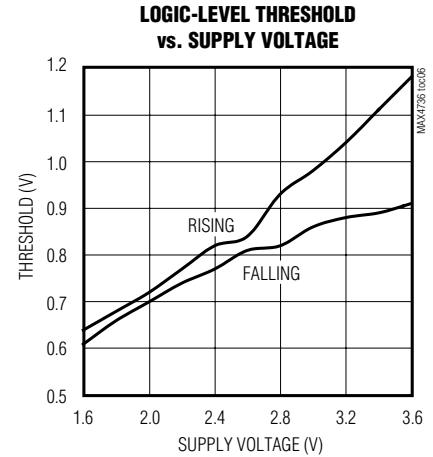
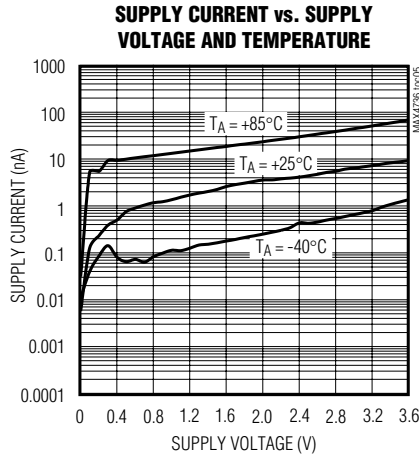
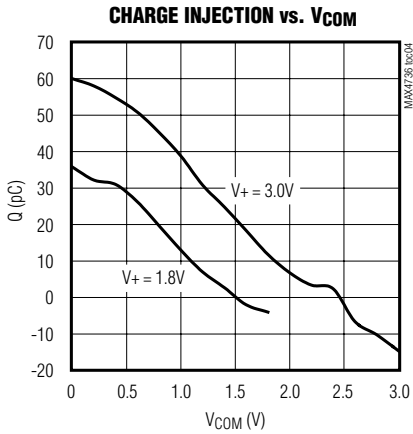
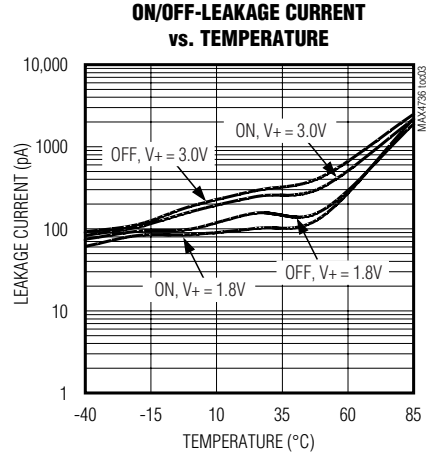
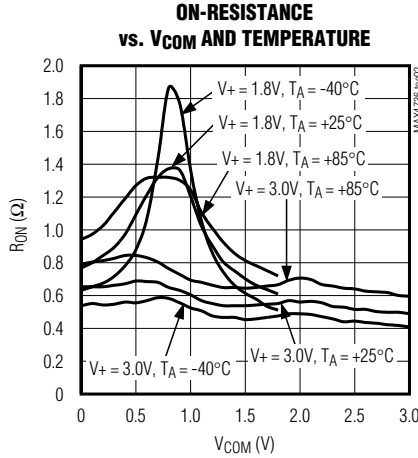
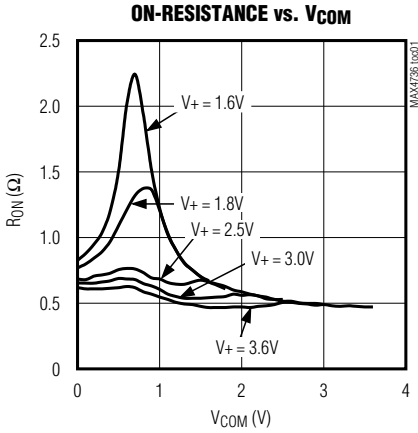
Note 12: The minimum load resistance is 8Ω.

0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

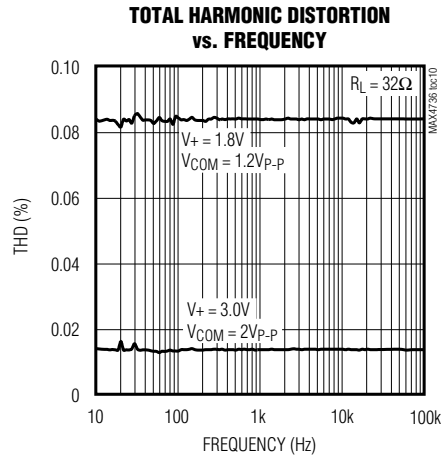
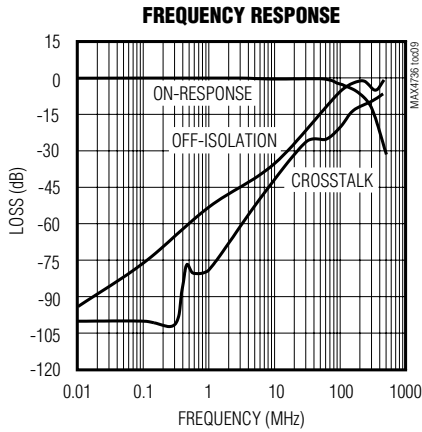
MAX4736



0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
μMAX/μDFN	TQFN		
1	12	IN1	Digital Control Input Switch 1
2	1	NO1	Analog Switch 1—Normally Open Terminal
3	2	GND	Ground
4	3	NO2	Analog Switch 2—Normally Open Terminal
5	4	IN2	Digital Control Input Switch 2
6	5	COM2	Analog Switch 2—Common Terminal
7	7	NC2	Analog Switch 2—Normally Closed Terminal
8	8	V+	Positive-Supply Voltage Input
9	9	NC1	Analog Switch 1—Normally Closed Terminal
10	11	COM1	Analog Switch 1—Common Terminal
—	6, 10	N.C.	No Connection
—	EP	EP	Exposed Pad. Connect to ground.

0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

Detailed Description

The MAX4736 is a low 0.8Ω max (at $V_+ = 2.7V$) on-resistance, low-voltage, dual SPDT analog switch that operates from a 1.6V to 4.2V single supply. CMOS switch construction allows switching analog signals that range from GND to V_+ .

When powered from a 2.7V supply, the 0.8Ω max R_{ON} allows high continuous currents to be switched in a variety of applications.

Applications Information

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings; stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_+ on first, followed by NO_+ , NC_+ , or COM_+ .

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_+ supply to other components. A 0.1μF capacitor, connected from V_+ to GND, is adequate for most applications.

Logic Inputs

The MAX4736 logic inputs can be driven up to 3.6V, regardless of the supply voltage. For example, with a 1.8V supply, IN_- can be driven low to GND and high to 3.6V. Driving IN_- rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V_+ to GND) can be passed with very little change in on-resistance (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO_- , NC_- , and COM_- pins can be used as either inputs or outputs.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

Test Circuits/Timing Diagrams

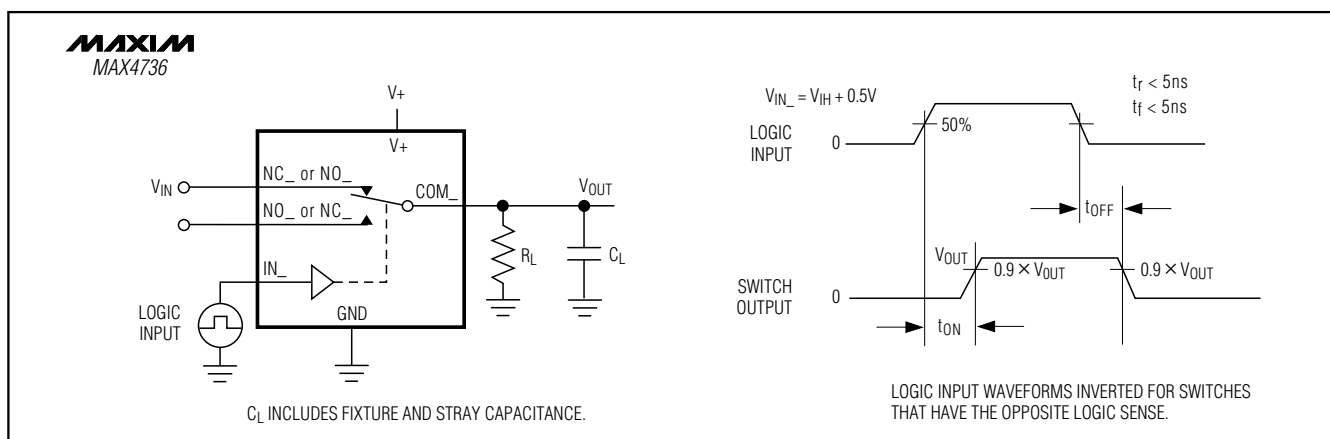


Figure 1. Switching Time

0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

Test Circuits/Timing Diagrams (continued)

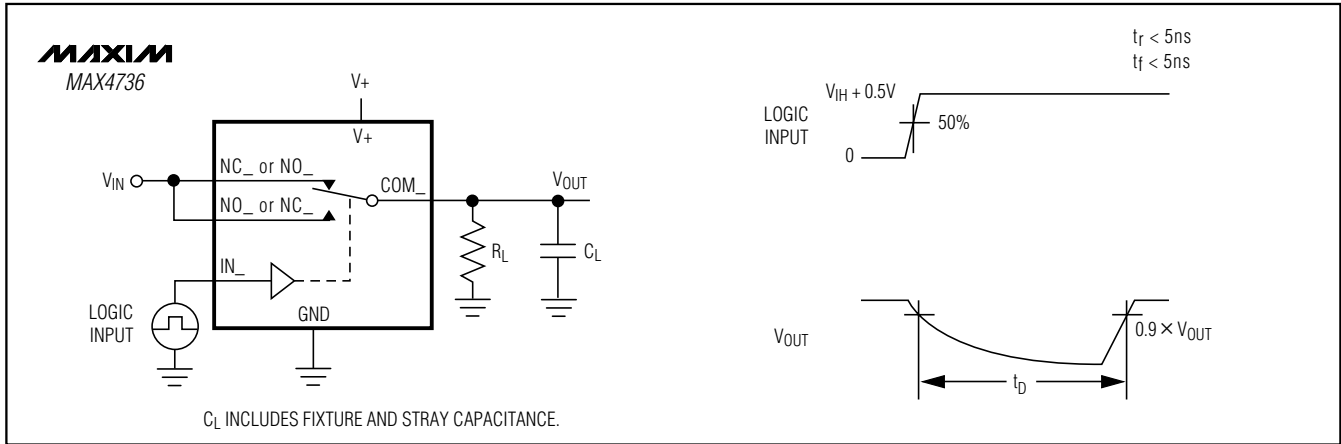


Figure 2. Break-Before-Make Interval

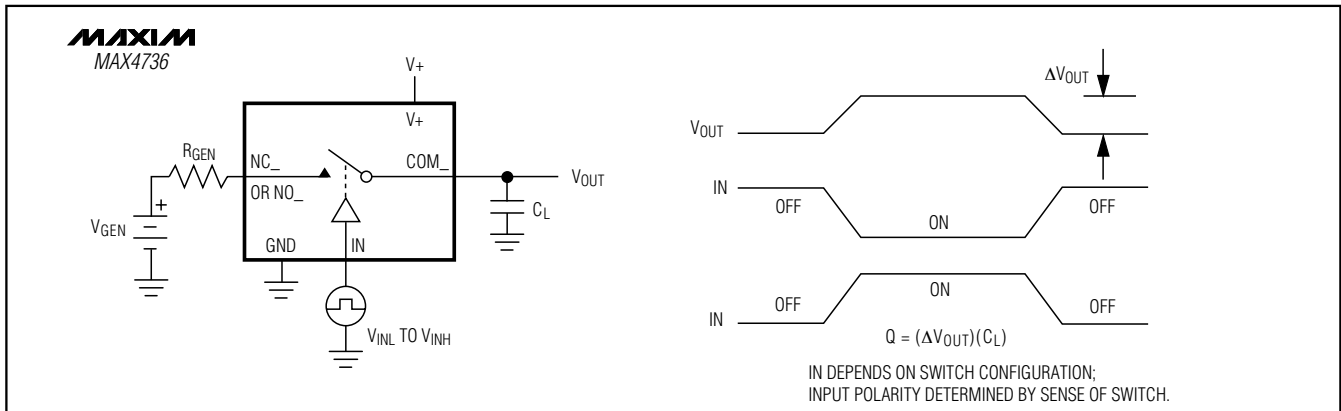


Figure 3. Charge Injection

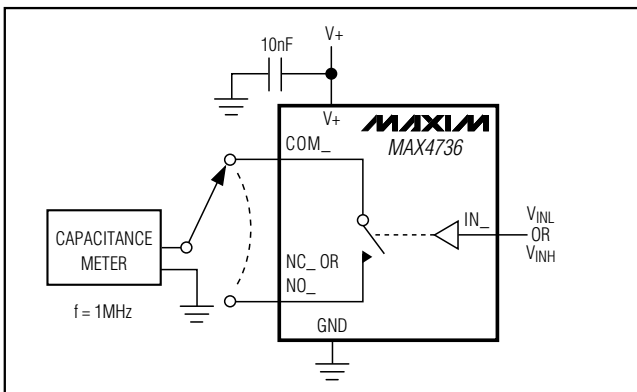


Figure 4. Channel Off/On-Capacitance

Chip Information

TRANSISTOR COUNT: 379

PROCESS: CMOS

0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

MAX4736

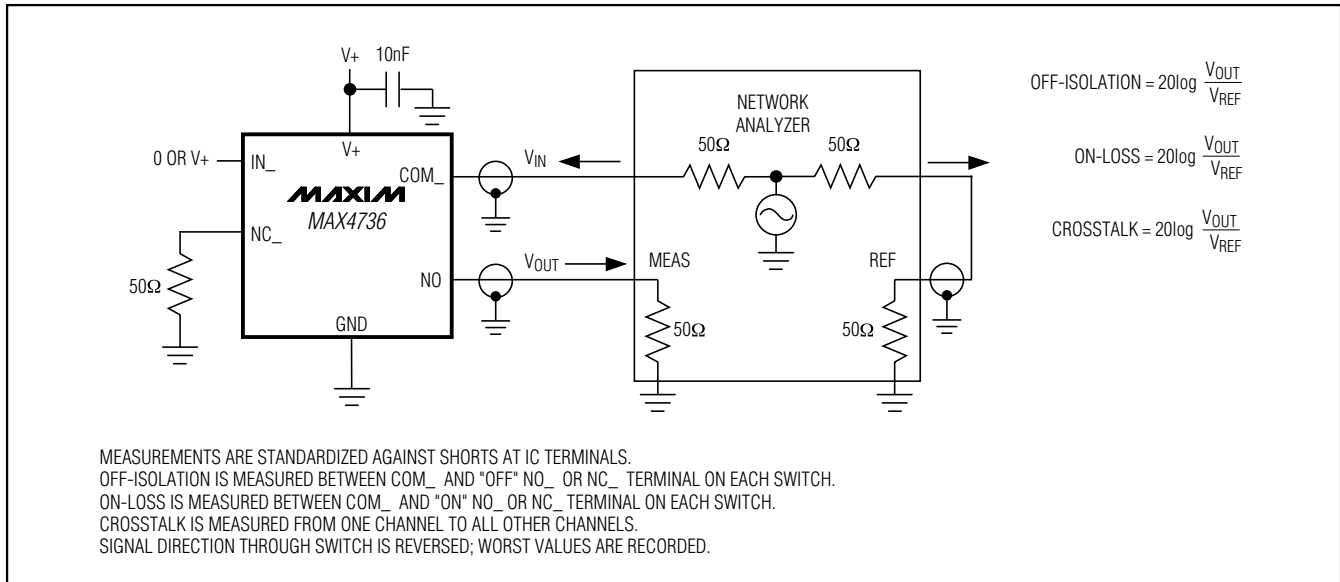
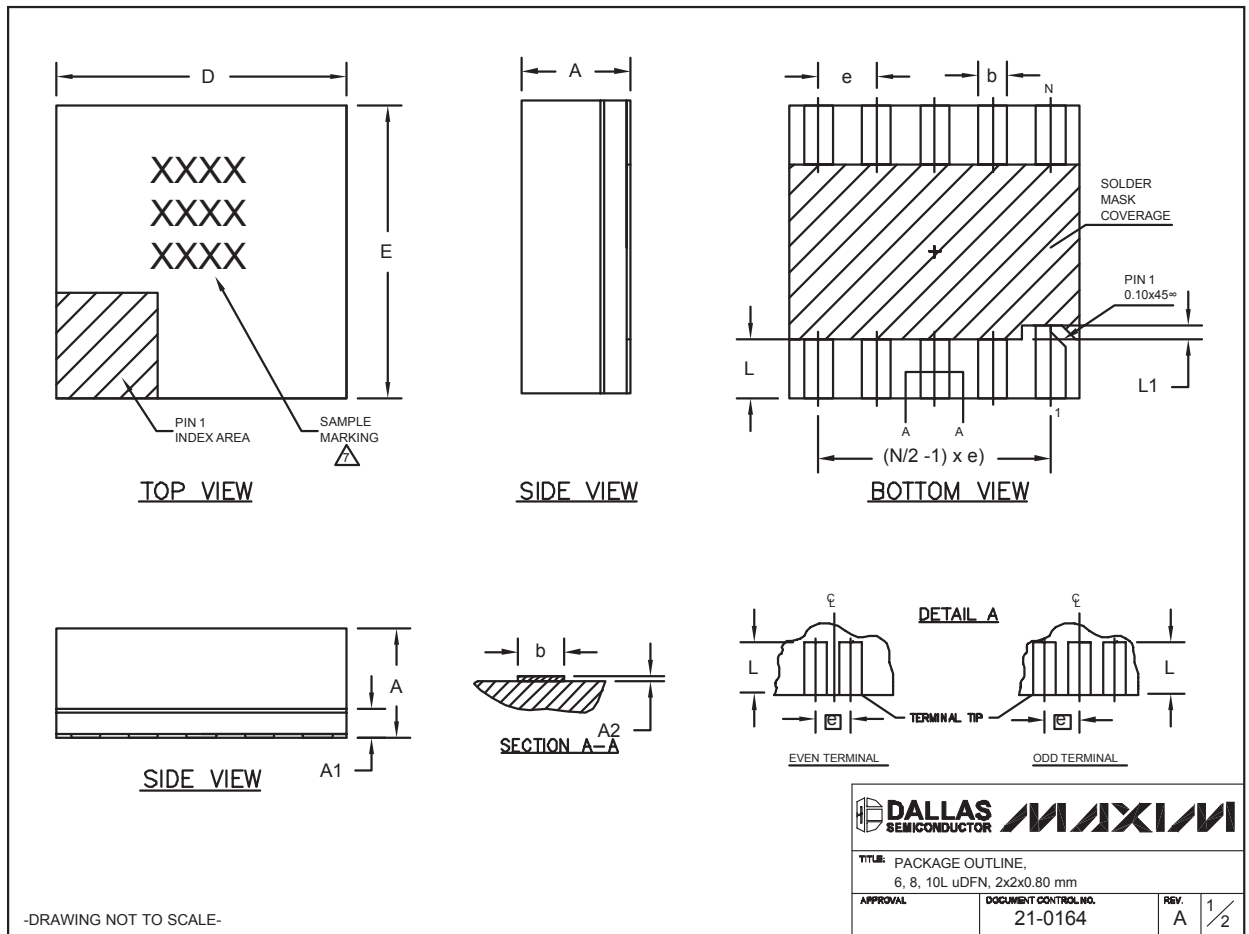


Figure 5. On-Loss, Off-Isolation, and Crosstalk

0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



6, 8, 10L UDFN:EPS

0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

MAX4736


Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.15	0.20	0.25
A2	0.020	0.025	0.035
D	1.95	2.00	2.05
E	1.95	2.00	2.05
L	0.30	0.40	0.50
L1	0.10 REF.		

PACKAGE VARIATIONS				
PKG. CODE	N	e	b	(N/2 - 1) x e
L622-1	6	0.65 BSC	0.30±0.05	1.30 REF.
L822-1	8	0.50 BSC	0.25±0.05	1.50 REF.
L1022-1	10	0.40 BSC	0.20±0.03	1.60 REF.

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
 2. COPLANARITY SHALL NOT EXCEED 0.08mm.
 3. WARPAGE SHALL NOT EXCEED 0.10mm.
 4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
 5. "N" IS THE TOTAL NUMBER OF LEADS.
 6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
-  MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

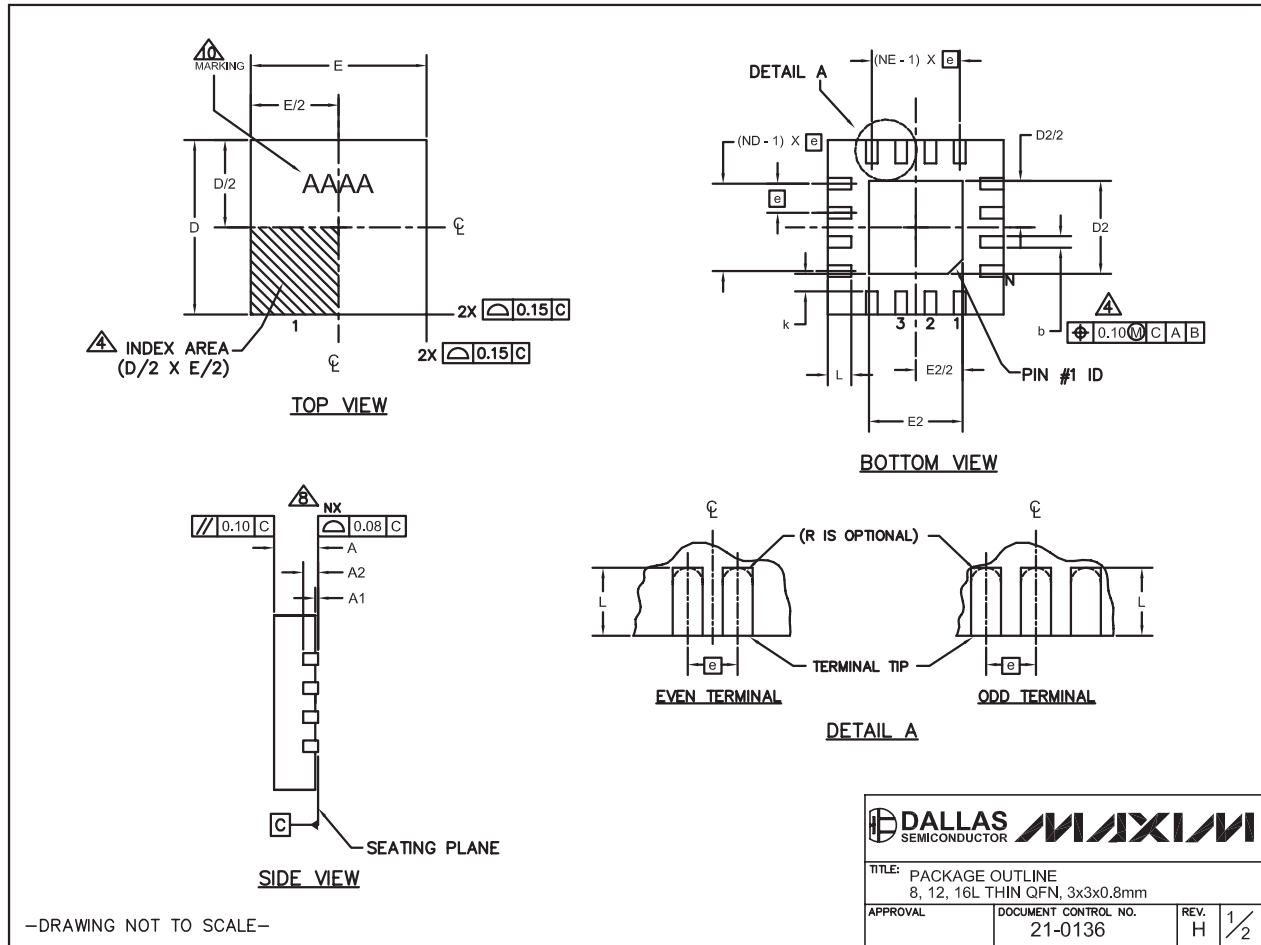
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TITLE: PACKAGE OUTLINE, 6, 8, 10L uDFN, 2x2x0.80 mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	2/2
	21-0164	A	

0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



0.6Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX4736

PKG REF.	8L 3x3			12L 3x3			16L 3x3		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

PKG. CODES	EXPOSED PAD VARIATIONS						PIN ID	JEDEC
	D2			E2				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220 REVISION C.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

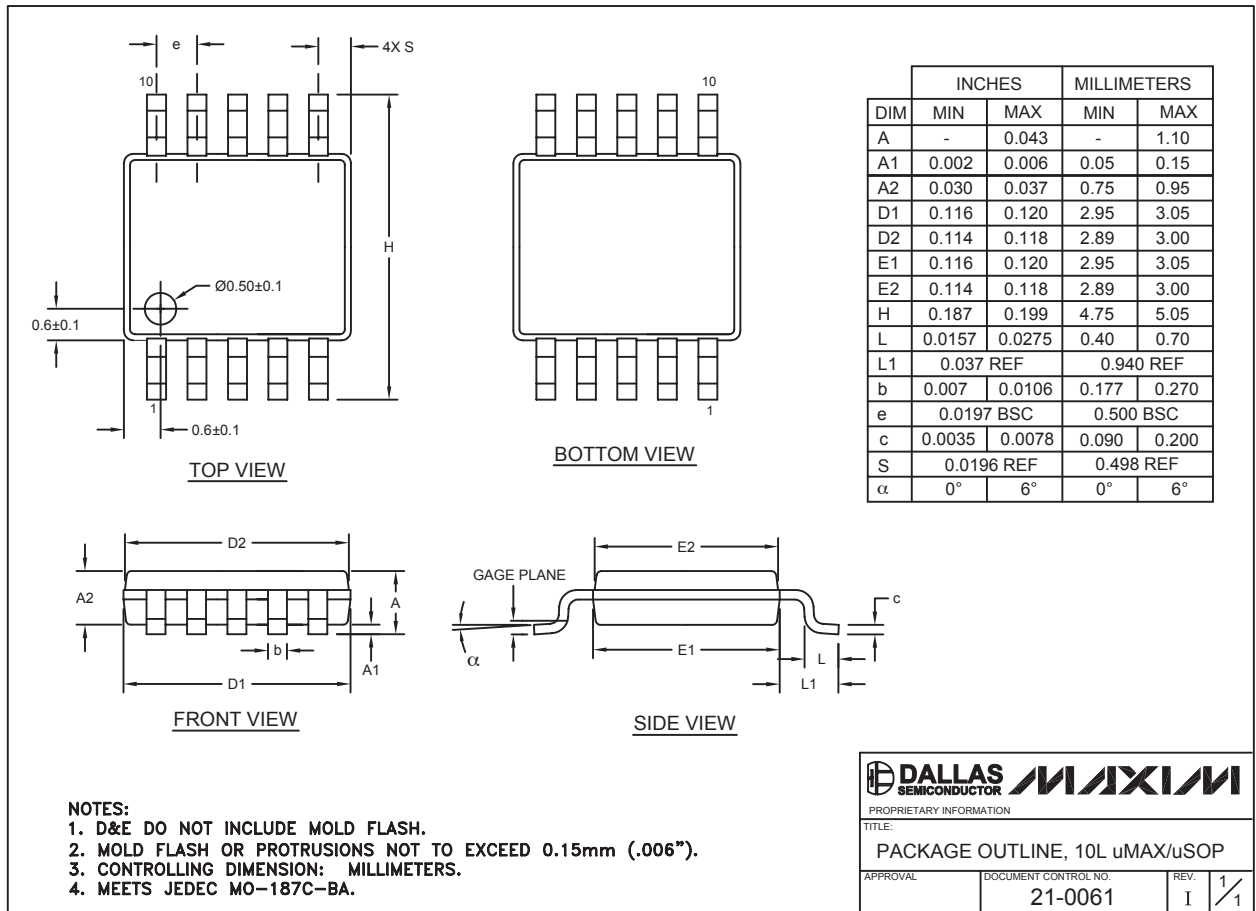
-DRAWING NOT TO SCALE-

			
TITLE: PACKAGE OUTLINE 8, 12, 16L THIN QFN, 3x3x0.8mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	H	2/2

0.8Ω, Low-Voltage, Single-Supply, Dual SPDT Analog Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



10LUMAX.EPS

Revision History

Pages changed at Rev 2: 1, 6, 10-14

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