Low-Voltage, Single and Dual Supply, Quad SPDT, High Performance Analog Switches

The Intersil ISL43240 device is a CMOS, precision, quad SPDT analog switches designed to operate from a single +2V to +12V supply or from a ±2V to ±6V supply. Targeted applications include battery powered equipment that benefit from the devices' low power consumption (5µW), low leakage currents (5nA max), and fast switching speeds (t_{ON} = 52ns, t_{OFF} = 40ns). A 5Ω maximum R_{ON} flatness ensures signal fidelity, while channel-to-channel mismatch is guaranteed to be less than 2Ω.

The ISL43240 is a quad single-pole / double-throw (SPDT) device and can be used as a quad SPDT, a quad 2:1 multiplexer, a single 4:1 multiplexer, or a dual 2-channel differential multiplexer.

Table 1 summarizes the performance of this family.

TABLE 1. FEATURES AT A GLANCE

CONFIGURATION	QUAD SPDT
±4.5V R_{ON}	18Ω
±4.5V t_{ON}/t_{OFF}	52ns/40ns
10.8V R_{ON}	14Ω
10.8V t_{ON}/t_{OFF}	40ns/27ns
4.5V R_{ON}	30Ω
4.5V t_{ON}/t_{OFF}	64ns/29ns
3V R_{ON}	51Ω
3V t_{ON}/t_{OFF}	120ns/50ns
Packages	20 Ld SSOP, 20 Ld QFN 4x4

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- AN557 "Recommended Test Procedures for Analog Switches"

Features

- Fully Specified for 10% Tolerances at V_S = ±5V and V+ = 12V, 5V and 3.3V
- Four Separately Controlled SPDT Switches
- ON Resistance (R_{ON}) 18Ω
- R_{ON} Matching Between Channels. . . . . <1Ω
- Low Charge Injection . . . . . 5pC (Max)
- Low Power Consumption (P_D) . . . . . <5µW
- Low Off Leakage Current (Max at 85°C) 2.5nA
- Fast Switching Action
  - t_{ON} 52ns
  - t_{OFF} 40ns
- Guaranteed Break-Before-Make
- Minimum 2000V ESD Protection per Method 3015.7
- TTL, CMOS Compatible
- Pb-free Available

Applications

- Battery Powered, Handheld, and Portable Equipment
  - Barcode Scanners
  - Laptops, Notebooks, Palmtops
- Communications Systems
  - Radios
  - XDSL and PBX / PABX
  - RF "Tee" Switches
  - Base Stations
- Test Equipment
  - Medical Ultrasound
  - Electrocardiograph
  - ATE
- Audio and Video Switching
- General Purpose Circuits
  - +3V/+5V DACs and ADCs
  - Digital Filters
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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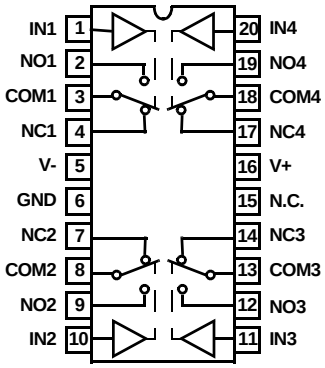
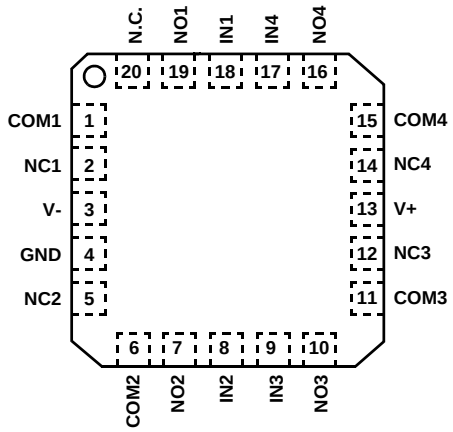
Pinouts (Note 1)

ISL43240 (SSOP)
TOP VIEW



ISL43240 (QFN)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	ISL43240 NO SW	ISL43240 NC SW
0	OFF	ON
1	ON	OFF

NOTE: Logic “0” ≤ 0.8V. Logic “1” ≥ 2.4V.

Pin Descriptions

PIN	FUNCTION
V+	Positive Power Supply Input
V-	Negative Power Supply Input. Connect to GND for Single Supply Configurations.
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Internal Connection

Ordering Information

PART NO. (BRAND)	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
ISL43240IA	-40 to 85	20 Ld SSOP	M20.209
ISL43240IA-T	-40 to 85	20 Ld SSOP Tape and Reel	M20.209
ISL43240IAZ (Note)	-40 to 85	20 Ld SSOP (Pb-free)	M20.209
ISL43240IAZ-T (Note)	-40 to 85	20 Ld SSOP Tape and Reel (Pb-free)	M20.209
ISL43240IR	-40 to 85	20 Ld QFN	L20.4x4
ISL43240IR-T	-40 to 85	20 Ld QFN Tape and Reel	L20.4x4
ISL43240IRZ (Note)	-40 to 85	20 Ld QFN (Pb-free)	L20.4x4
ISL43240IRZ-T (Note)	-40 to 85	20 Ld QFN Tape and Reel (Pb-free)	L20.4x4

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

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Absolute Maximum Ratings

V+ to V- . . . . . -0.3 to15V
V+ to GND . . . . . -0.3 to15V
V- to GND . . . . . -15 to 0.3V
All Other Pins (Note 2) . . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
Continuous Current (Any Terminal) 30mA
Peak Current, IN, NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) 100mA
ESD Rating (Per MIL-STD-883 Method 3015). . . . . >2kV

Operating Conditions

Temperature Range
ISL43240IX . . . . . -40^{o}C to 85^{o}C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (^{o}C/W)
20 Ld SSOP Package (Note 3)	150
20 Ld QFN Package (Note 4)	75

Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Moisture Sensitivity (See Technical Brief TB363)
All Packages . . . . . Level 1
Maximum Storage Temperature Range. . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Electrical Specifications: ±5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	V-	-	V+	V
ON Resistance, R_{ON}	V_S = ±4.5V, I_{COM} = 10mA, V_{NO} or V_{NC} = ±3.5V, See Figure 5	25	-	18	25	Ω
		Full	-	-	30	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V_S = ±4.5V, I_{COM} = 10mA, V_{NO} or V_{NC} = ±3V	25	-	0.5	2	Ω
		Full	-	-	4	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V_S = ±4.5V, I_{COM} = 10mA, V_{NO} or V_{NC} = 0V, ±3V, Note 7	25	-	-	5	Ω
		Full	-	-	5	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = $\overline{+}$4.5V, Note 6	25	-0.2	-	0.2	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V, Note 6	25	-0.4	-	0.4	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	2.4	1.6	-	V
Input Voltage Low, V_{INL}		Full	-	1.5	0.8	V
Input Current, I_{INH}, I_{INL}	V_S = ±5.5V, V_{IN} = 0V or V+	Full	-1	-	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	52	65	ns
		Full	-	-	75	ns
Turn-OFF Time, t_{OFF}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	40	50	ns
		Full	-	-	55	ns
Break-Before-Make Time Delay, t_D	V_S = ±5.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 3	Full	10	19	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	-	5	pC
NO OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	30	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 1MHz, V_{NO} or V_{NC} = 1V_{RMS}, See Figures 4 and 6	25	-	71	-	dB
Crosstalk, Note 8		25	-	-92	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	59	-	dB

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Electrical Specifications: ±5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	±2	-	±6	V
Positive Supply Current, I+	V_S = ±5.5V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.01	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.01	1	µA
		Full	-1	-	1	µA

NOTES:

5. V_{IN} = Input voltage to perform proper function.
6. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
7. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at 25^{o}C.
8. Flatness is defined as the delta between the maximum and minimum R_{ON} values over the specified voltage range.
9. Between any two switches.

Electrical Specifications: 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN (NOTE 5)	TYP	MAX (NOTE 5)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V, See Figure 5	25	-	30	40	Ω
		Full	-	-	50	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V	25	-	0.5	3	Ω
		Full	-	-	4	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 5.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V, Note 7	25	-	4.4	6	Ω
		Full	-	-	8	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V, Note 6	25	-0.2	-	0.2	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 1V, 4.5V Note 6	25	-0.4	-	0.4	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	2.4	1.5	-	V
Input Voltage Low, V_{INL}		Full	-	1.4	0.8	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{IN} = 0V or V+	Full	-1	-	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	64	80	ns
		Full	-	-	90	ns
Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	29	40	ns
		Full	-	-	45	ns
Break-Before-Make Time Delay, t_D	V+ = 5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 3	Full	15	39	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	1.2	2	pC
NO OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	30	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 1MHz, V_{NO} or V_{NC} = $1V_{RMS}$, See Figures 4 and 6	25	-	71	-	dB
Crosstalk, Note 8		25	-	-92	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	59	-	dB

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Electrical Specifications: 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN (NOTE 5)	TYP	MAX (NOTE 5)	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 5.5V, V- = 0V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.01	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.01	1	µA
		Full	-1	-	1	µA

Electrical Specifications: 3.3V Supply

Test Conditions: V+ = +3.0V to +3.6V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN (NOTE 5)	TYP	MAX (NOTE 5)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V, See Figure 5	25	-	51	60	Ω
		Full	-	-	70	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V	25	-	0.5	3	Ω
		Full	-	-	4	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 0.5V, 1.5V, Note 7	25	-	12	17	Ω
		Full	-	-	17	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.6V, V_{COM} = 1V, 3V, V_{NO} or V_{NC} = 3V, 1V, Note 6	25	-0.2	-	0.2	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.6V, V_{COM} = 1V, 3V, V_{NO} or V_{NC} = 1V, 3V, Note 6	25	-0.4	-	0.4	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	2.4	1.0	-	V
Input Voltage Low, V_{INL}		Full	-	0.9	0.8	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+	Full	-1	-	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	120	138	ns
		Full	-	-	160	ns
Turn-OFF Time, t_{OFF}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	50	60	ns
		Full	-	-	65	ns
Break-Before-Make Time Delay, t_D	V+ = 3.6V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 3	Full	30	60	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	1	2	pC
NO OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	30	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 1MHz, V_{NO} or V_{NC} = $1V_{RMS}$, See Figures 4 and 6	25	-	71	-	dB
Crosstalk, Note 8		25	-	-92	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	59	-	dB
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V- = 0V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.01	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.01	1	µA
		Full	-1	-	1	µA

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Electrical Specifications: 12V Supply

Test Conditions: V+ = +10.8V to +13.2V, V- = GND = 0V, V_{INH} = 3.0V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN (NOTE 6)	TYP	MAX (NOTE 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V, See Figure 5	25	-	14	20	Ω
		Full	-	-	30	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V	25	-	0.3	2	Ω
		Full	-	-	4	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 13.2V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V, 6V, 9V, Note 7	25	-	1.7	2	Ω
		Full	-	-	3	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 13V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 12V, 1V, Note 6	25	-0.2	-	0.2	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 13V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 1V, 12V Note 6	25	-0.4	-	0.4	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	3.0	2.8	-	V
Input Voltage Low, V_{INL}		Full	-	2.2	0.8	V
Input Current, I_{INH}, I_{INL}	V+ = 13.2V, V_{IN} = 0V or V+	Full	-1	-	1	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	40	50	ns
		Full	-	-	83	ns
Turn-OFF Time, t_{OFF}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 1	25	-	27	35	ns
		Full	-	-	40	ns
Break-Before-Make Time Delay, t_D	V+ = 13.2V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, See Figure 3	Full	5	20	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, See Figure 2	25	-	12	14	pC
NO OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	10	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, See Figure 7	25	-	30	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 1MHz, V_{NO} or V_{NC} = $1V_{RMS}$, See Figures 4 and 6	25	-	71	-	dB
Crosstalk, Note 8		25	-	-92	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	59	-	dB
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13V, V_{IN} = 0V or V+, Switch On or Off	25	-1	0.01	1	µA
		Full	-1	-	1	µA
Negative Supply Current, I-		25	-1	0.01	1	µA
		Full	-1	-	1	µA

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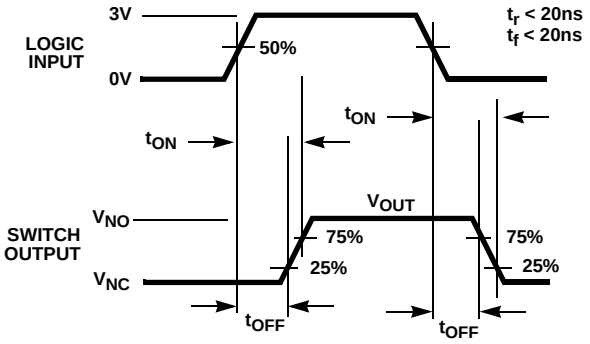
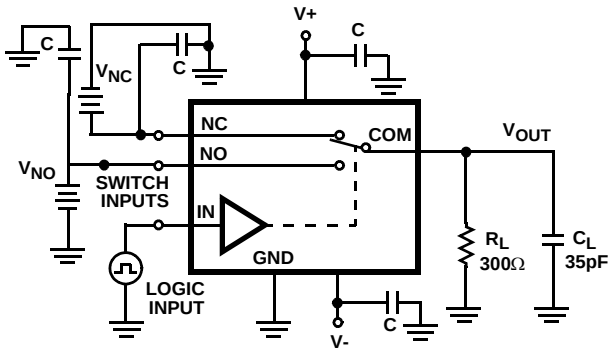
Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

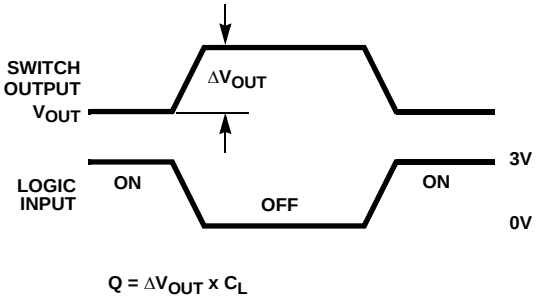


Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

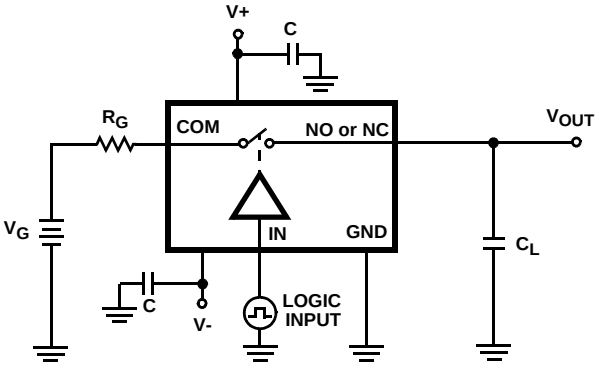
FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

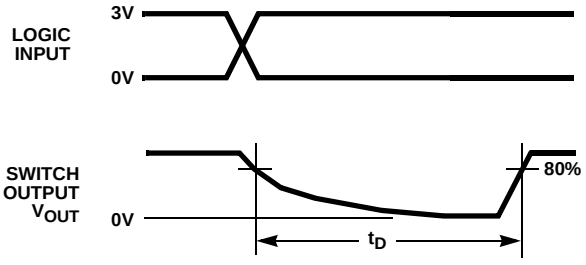
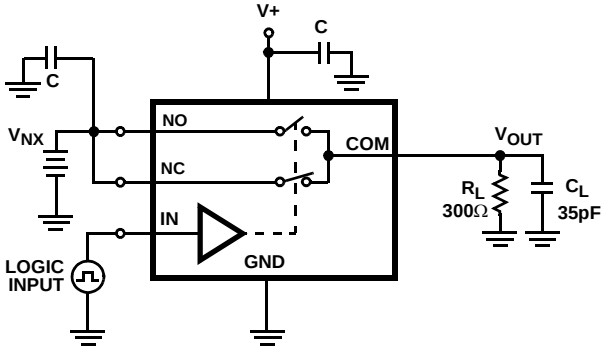


FIGURE 3A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME

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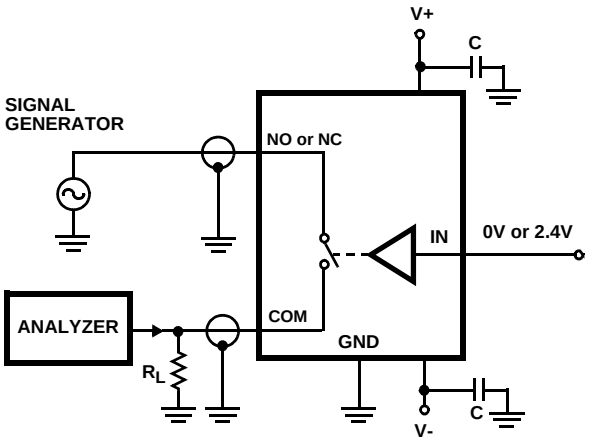
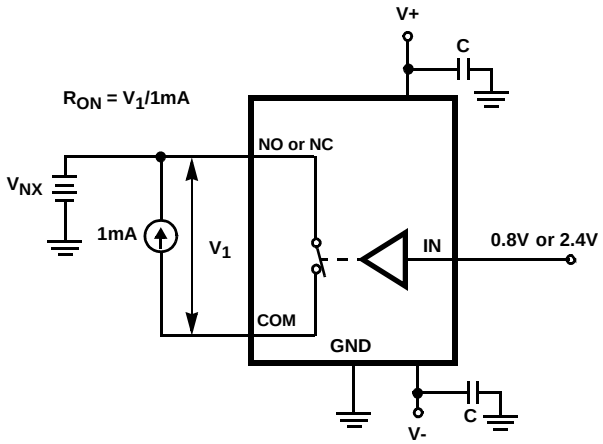
Test Circuits and Waveforms (Continued)



Repeat test for all switches.

FIGURE 4. OFF ISOLATION TEST CIRCUIT



Repeat test for all switches.

FIGURE 5. R_{ON} TEST CIRCUIT

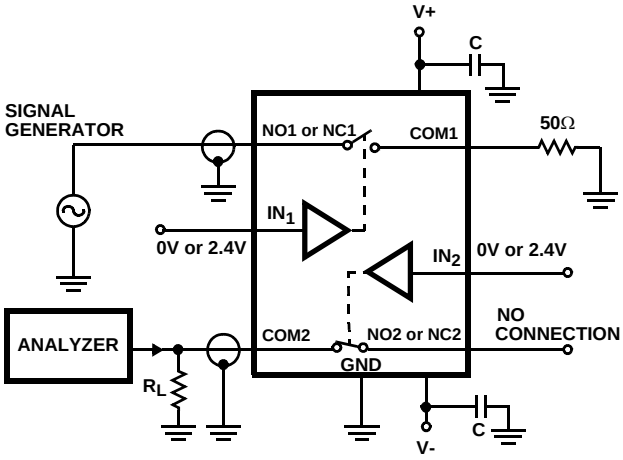


FIGURE 6. CROSSTALK TEST CIRCUIT

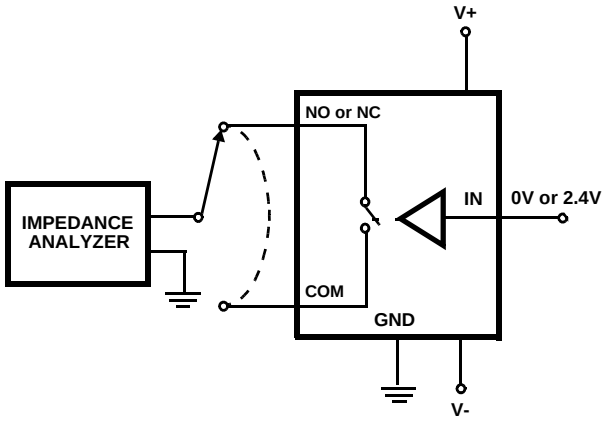


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43240 quad analog switches offer precise switching capability from a bipolar ±2V to ±6V or a single 2V to 12V supply with low on-resistance (18Ω) and high speed operation (t_{ON} = 52ns, t_{OFF} = 40ns). The devices are especially well suited for portable battery powered equipment thanks to the low operating supply voltage (2V), low power consumption (5µW), low leakage currents (5nA max). High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 8). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above V-.

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The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

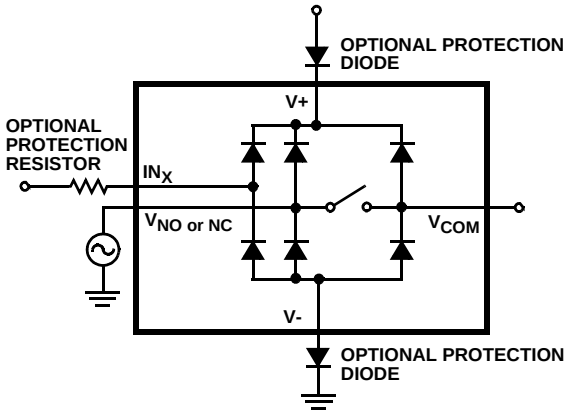

FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL43240 construction is typical of most CMOS analog switches, in that they have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V maximum supply voltage, the ISL43240 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies (±6V or 12V single supply), as well as room for overshoot and noise spikes.

This family of switches performs equally well when operated with bipolar or single voltage supplies. The minimum recommended supply voltage is 2V or ±2V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

Logic-Level Thresholds

V+ and GND power the internal logic stages, so V- has no affect on logic thresholds. This switch family is TTL compatible (0.8V and 2.4V) over a V+ supply range of 2.5V to 10V (see Figure 17). At 12V the V_{IH} level is about 2.8V. For best results with a 12V supply, use a logic family the provides a V_{OH} greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails (see Figure 18). Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation. The ISL43240 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example driving the device with 3V logic (0V to 3V) while operating with dual or single 5V supplies the device draws only 10µA of current (see Figure 18 for V_{IN} = 3V). Similiar devices of competitors can draw 8 times this amount of current.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 200MHz (see Figure 19). Figure 19 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An off switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off Isolation is the resistance to this feedthrough, while Crosstalk indicates the amount of feedthrough from one switch to another. Figure 20 details the high Off Isolation and Crosstalk rejection provided by this switch. At 10MHz, off isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

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Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified

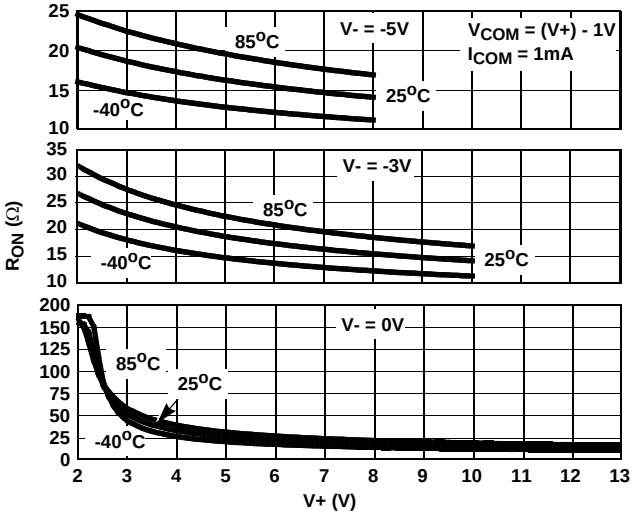

FIGURE 9. ON RESISTANCE vs POSITIVE SUPPLY VOLTAGE

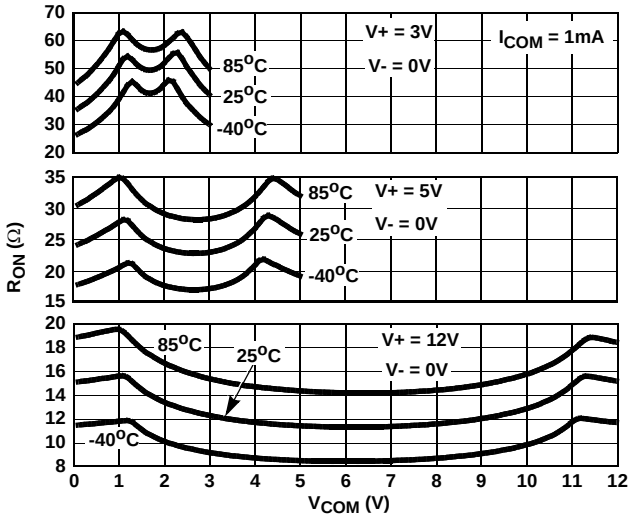

FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

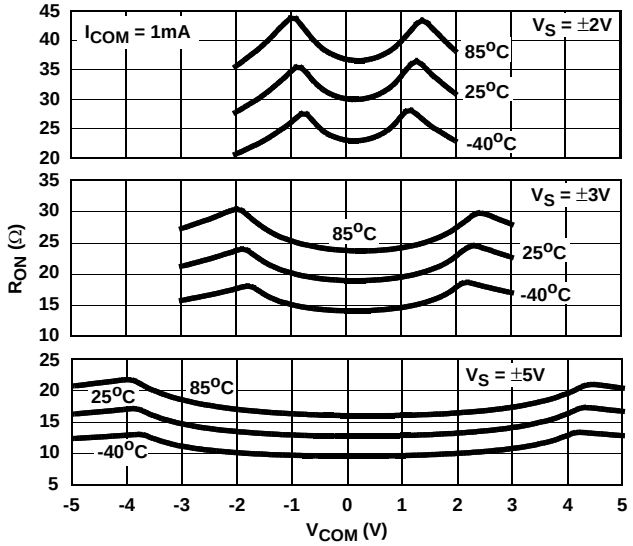

FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

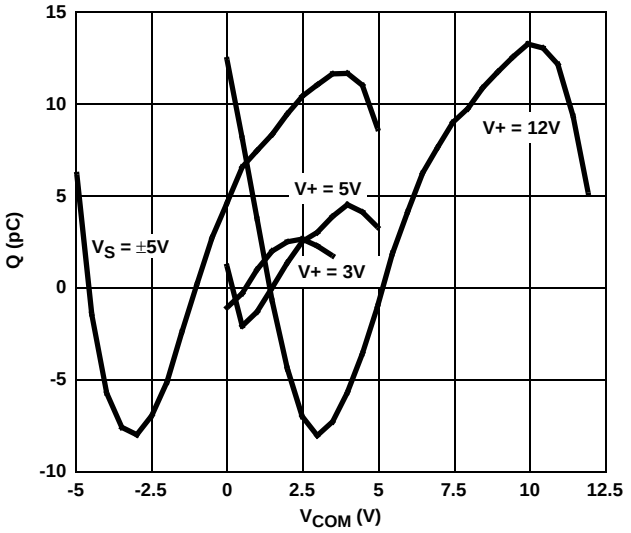

FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

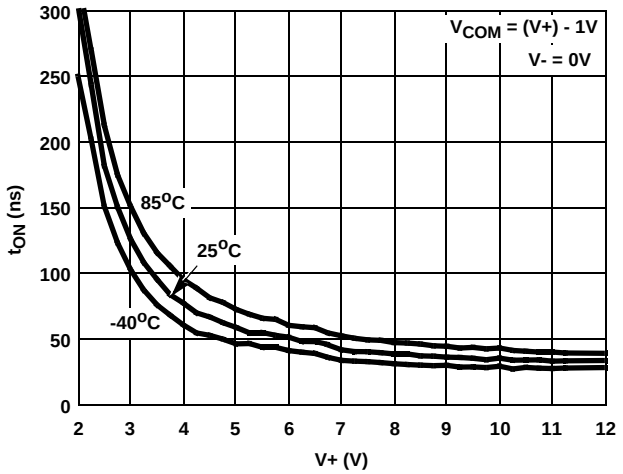

FIGURE 13. TURN - ON TIME vs POSITIVE SUPPLY VOLTAGE

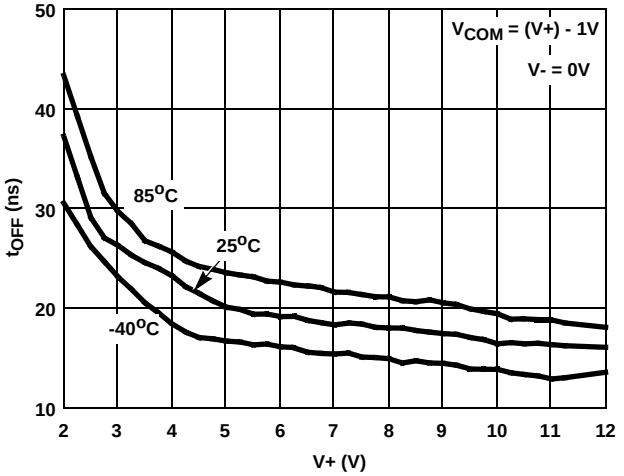

FIGURE 14. TURN - OFF TIME vs POSITIVE SUPPLY VOLTAGE

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Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

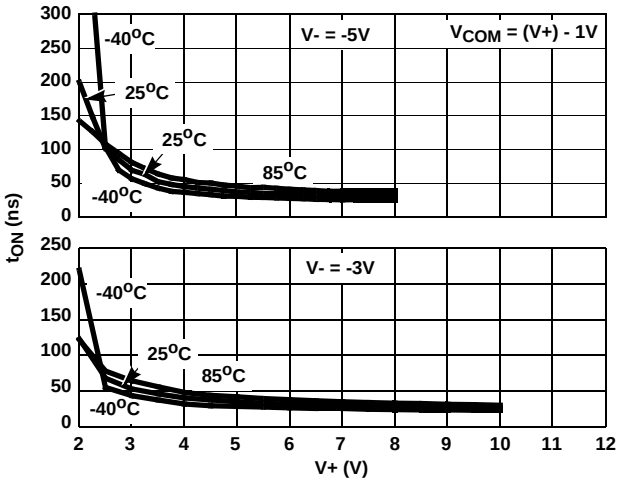

FIGURE 15. TURN - ON TIME vs POSITIVE SUPPLY VOLTAGE

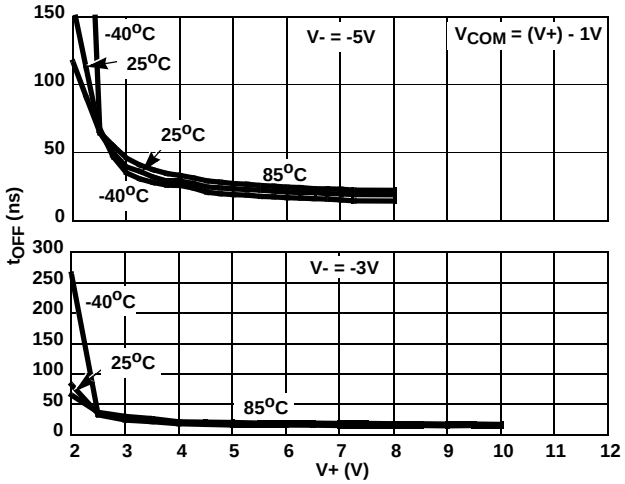

FIGURE 16. TURN - OFF TIME vs POSITIVE SUPPLY VOLTAGE

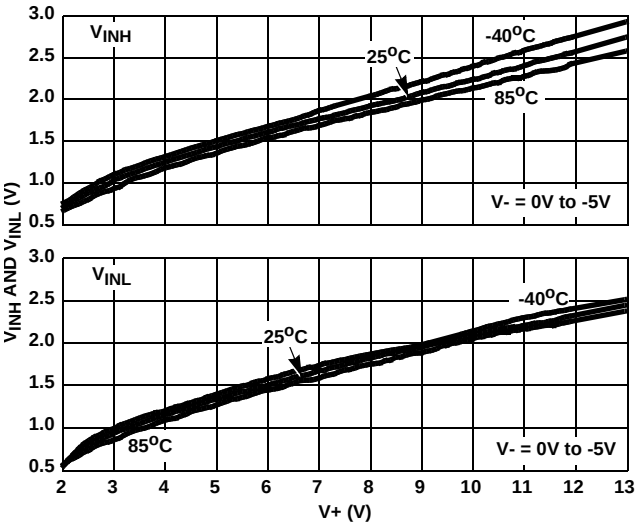

FIGURE 17. DIGITAL SWITCHING POINT vs POSITIVE SUPPLY VOLTAGE

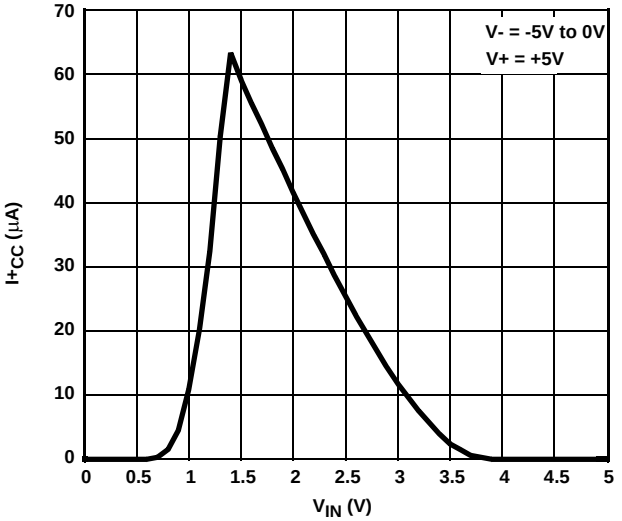

FIGURE 18. POSITIVE SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE

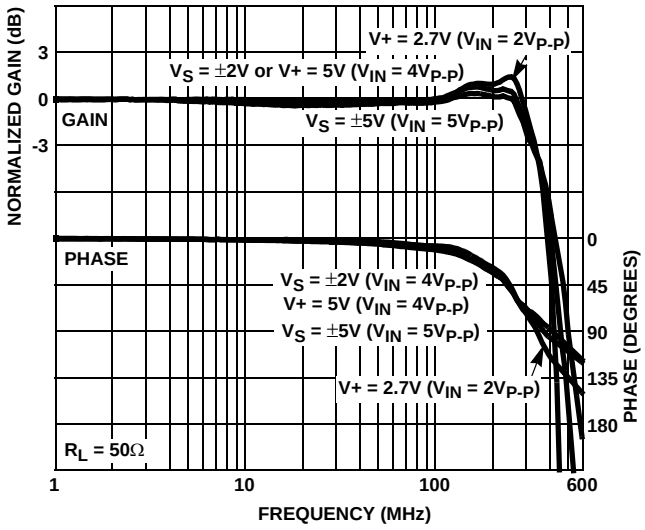

FIGURE 19. FREQUENCY RESPONSE

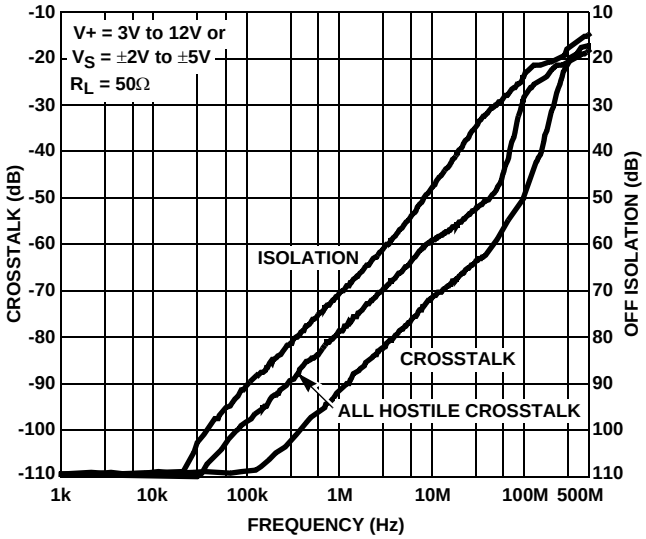

FIGURE 20. CROSSTALK AND OFF ISOLATION

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Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

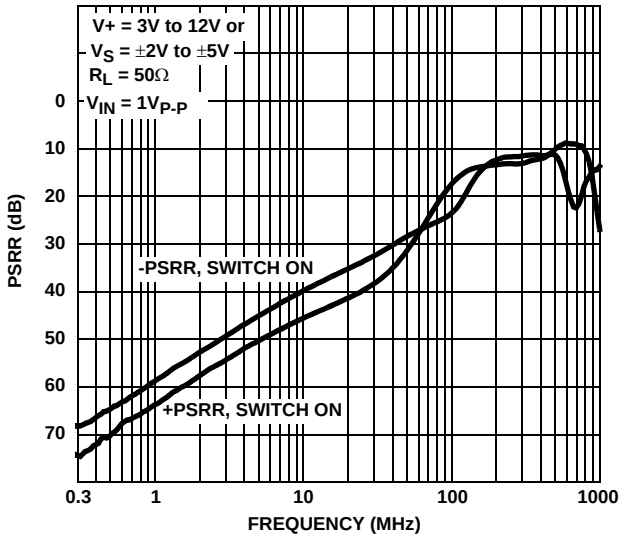

FIGURE 21. ±PSRR vs FREQUENCY

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

V-

TRANSISTOR COUNT:

ISL43240: 418

PROCESS:

Si Gate CMOS

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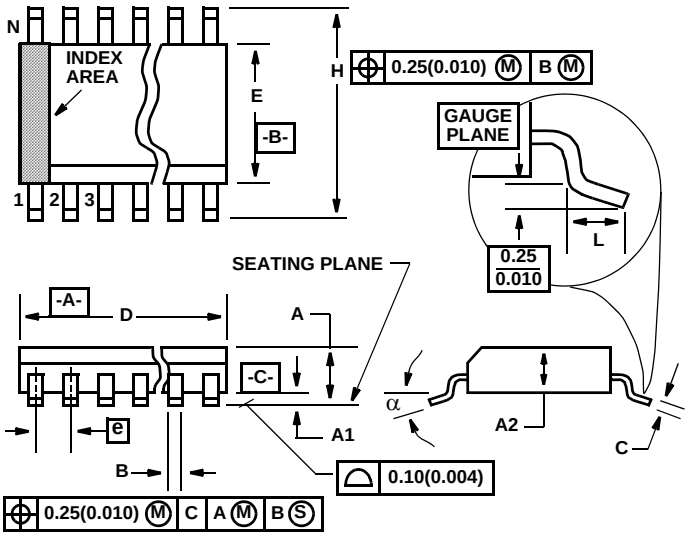
Shrink Small Outline Plastic Packages (SSOP)



M20.209 (JEDEC MO-150-AE ISSUE B)
20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.068	0.078	1.73	1.99	
A1	0.002	0.008’	0.05	0.21	
A2	0.066	0.070’	1.68	1.78	
B	0.010’	0.015	0.25	0.38	9
C	0.004	0.008	0.09	0.20’	
D	0.278	0.289	7.07	7.33	3
E	0.205	0.212	5.20’	5.38	4
e	0.026 BSC		0.65 BSC		
H	0.301	0.311	7.65	7.90’	
L	0.025	0.037	0.63	0.95	6
N	20		20		7
α	0 deg.	8 deg.	0 deg.	8 deg.	

Rev. 3 11/02

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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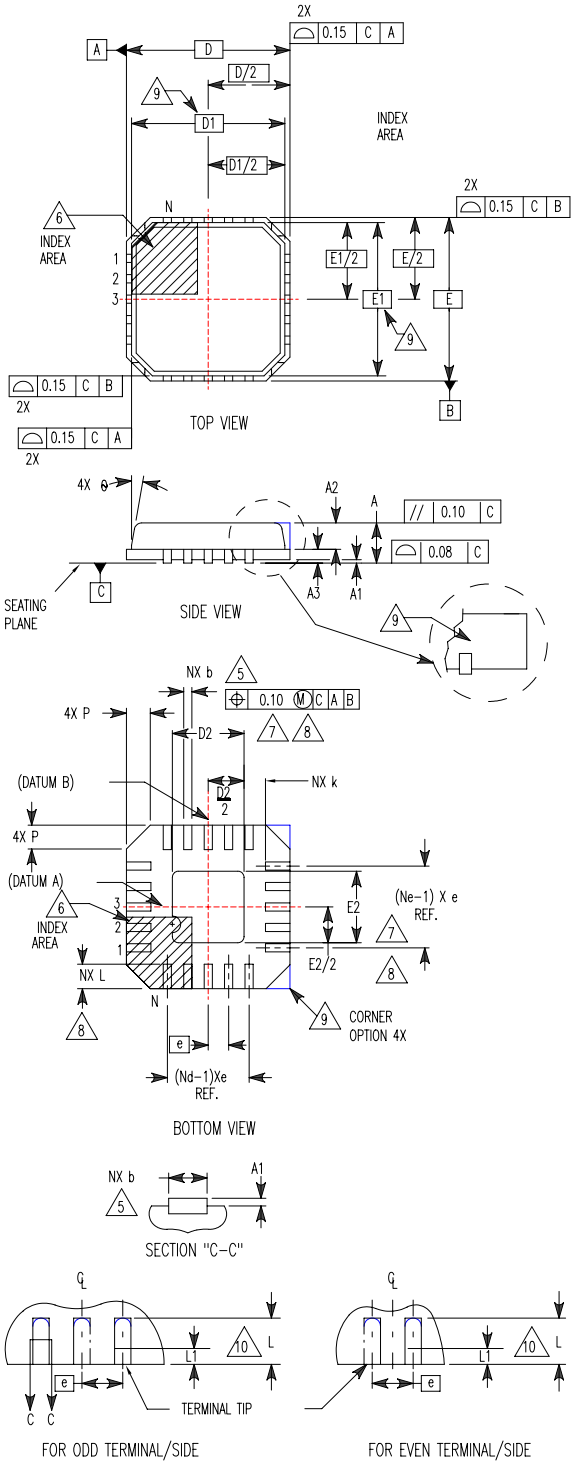
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.4x4

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VGGD-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		20		2
Nd		5		3
Ne	5	5		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

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